A GHz CMOS Frequency Synthesizer for Mobile Communication

by

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Abstract

This thesis presents an integrated solution for generating modulation frequencies in a GHz range, while providing a fine resolution by using a fractional-N approach. The synthesizer contains a phase-locked-loop that controls a four-stage ring oscillator to generate frequencies at around 700MHz. The four-stage ring oscillator provides two sets of quadrature signals to a mixer to demodulate any incoming RF at twice the oscillator's frequency. Design theories and issues are discussed in each chapter. For all building blocks, system-level and transistor-level simulations are verified and presented. A complete frequency synthesizer is fabricated in a 0.5um-CMOS process. The active area of the whole design is 1mm × 1.5mm and dissipates 32mW (simulated) at a supply voltage of 3.0 volt.

Acknowledgments

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Finally, I would like to record my unspoken debt to my girlfriend, my parents, and my sister who, at all times, shared my frustration and cared about me so that I am still in a good shape even though a few of my hair have already turned white. (But I believe they won't mind.)

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Introduction

1

The ever increasing demand for laptop computers and cellular phones in the last decade indicates a growing need for devices which facilitate mobility while allowing constant communication. In the future, analog cellular phones will be replaced by digital modems. This trend is motivated by the ability of digital cellular standards to accommodate more users, to provide better security, and to allow the transmission of digital data. Once the transition is complete, digital formats will enable laptop computers and cellular phones to merge, making the "mobile office" a reality.

Conventional RF (Radio Frequency) architectures with discrete external components, and expensive SAW (Surface Acoustic Wave) filters, are not attractive prospects for the wireless market. In the wireless market, the most important thing is the cost and then is the power consumption. The only reason power ranks second is because a cheaper battery can be used. The difficulty in developing an RF architecture which is suitable for a standard digital CMOS process goes beyond achieving high-speed circuits with low power supply voltages and low power dissipation. The real challenge exists in providing these benefits while still delivering what the market

demands: low cost.

1.1 Motivation: A Single-chip Digital Radio Receiver

One of the aims of our analog electronics group has been to develop high-speed circuits that will allow the integration of a complete digital radio receiver onto a single chip. A new architecture proposed in [1] goes beyond limitations of the direct-conversion architecture that has been gaining interest for single-chip designs. A non-zero quadrature IF reduces the image problem and eliminates concerns about self-EMI and $1/f$ noise. A complex bandpass filter embedded in a delta-sigma loop allows the A/D conversion to be performed directly on the pair of quadrature outputs from the mixer.

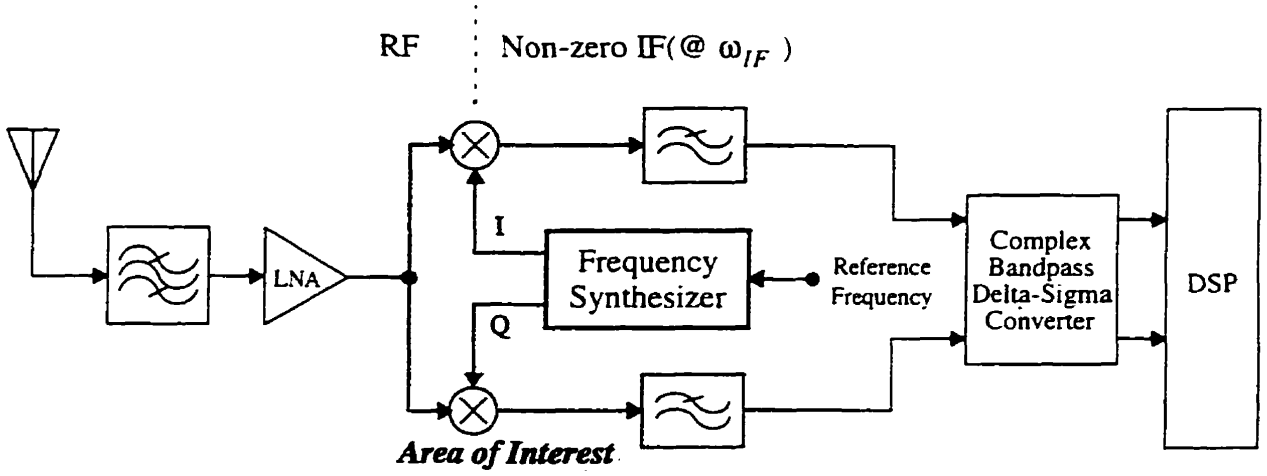


Figure 1.1 Architecture for the RF front-end

The purpose of this thesis is to provide the RF front-end (See Figure 1.1) with a frequency synthesizer which downconverts the incoming RF to the low-IF for the complex bandpass delta-sigma converter. The synthesizer applies the fractional-N method to generate frequencies with an accurate channel step-size which are non-integer multiples of the reference frequency.

1.2 Types of Frequency Synthesis

The frequency synthesizer generates a local oscillation (LO) signal used in the down-conversion of received signals. This signal must meet the frequency stability, precision, and frequency agility required by the architecture. Furthermore, the LO signal must have a spectrum which does not degrade the receiver performance and exceed the limits set by the other components of the receiver. The function of the frequency synthesizer is to translate the performance of a reference oscillator to frequencies that are useful to the users. Various methods are available to generate this carrier frequency. However, many of them are restrictive due to the modulation requirements of the system, the ability of the synthesizer to be integrated, as well as the necessity of limiting power dissipation. Many of these methods are summarized below. Other high-performance frequency synthesizers typically combine two or more of the following methods, exploiting the advantages of each.

Direct Analog Synthesis

In direct analog synthesis, the reference frequency is directly translated using analog techniques such as switching, frequency division, multiplication, filtering, and mixing. This form of synthesis offers very high purity at the cost of very high complexity. What follows is an explanation of some typical types of synthesis along with their advantages and disadvantages in terms of a wireless environment.

Frequency Switching

Frequency Switching (See Figure 1.2) is the most straight-forward form of frequency synthesis. It consists of a bank of crystals connected through a bank of switches to a crystal-controlled oscillator. While this type of synthesizer has good close-in phase noise purity and high stability of the

crystal reference is maintained [2], it has many disadvantages: for instance, the high cost of hardware, the limitations on the output frequency, and the difficulty in integrating such systems. As different reference crystals are required for each desired output frequency, the cost becomes excessive. Besides, the output frequency is limited to the maximum oscillating frequency of a crystal, but most of the crystal oscillators available in the market are usually under 200 MHz. Finally, with so many external crystals, complete integration becomes impossible.

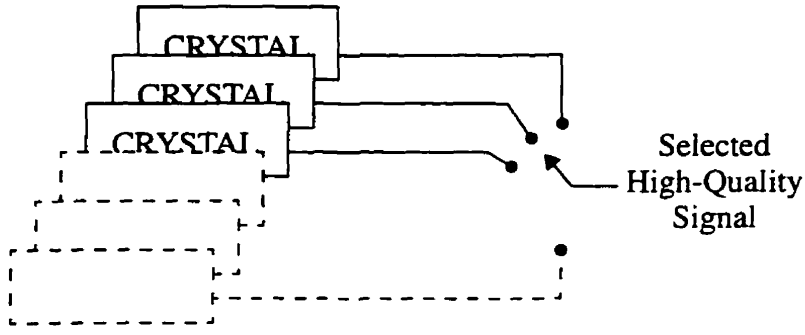


Figure 1.2 The use of multiple crystals to tune an RF system

Frequency Mixing

Frequency mixing utilizes a mixer to multiply two signals together, generating a signal that contains both the sum and the difference of the two input frequencies. Typically only one of these two frequencies is desired. This type of synthesizer has very good noise performance and the same stability as the reference oscillator. Frequency mixing is accomplished by using a nonlinear element such as a diode or a transistor and by exploiting the non-linearities to perform the mixing action. Unfortunately, the non-linearities tend to produce a signal that contains many spurious tones at various mixing products. The final signal will be a combination of many frequencies with the form: $nf_a \pm mf_b$

These spurious frequencies are the basic disadvantage of frequency mixing. Filtering can be used to eliminate these spurs, but can do so only at the price of a narrow frequency range. A

wide-band solution to reduce unwanted spurs is to use balanced mixers or quadrature mixers. Quadrature mixers can be easily integrated and can attenuate spurious frequencies from 20 to 50 dB.

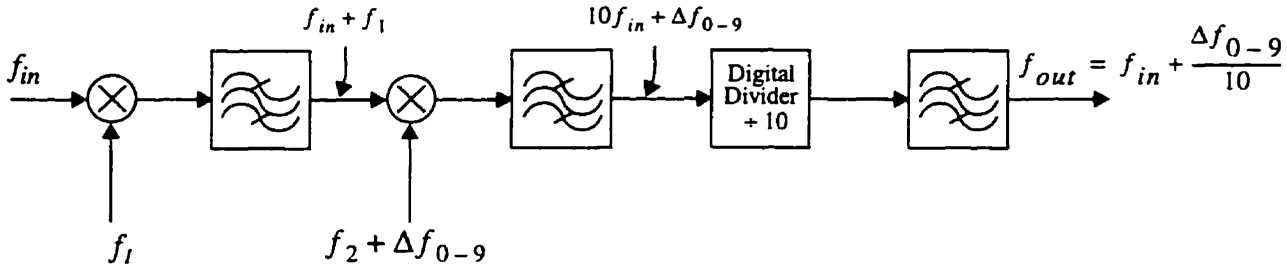


Figure 1.3 Frequency synthesis using frequency mixing method

Direct Digital Frequency Synthesis

A Direct-Digital Frequency Synthesizer (DDFS) proposed in [3] produces a smooth, sinusoid-like signal by combining a sine look-up table and a digital-to-analog converter (DAC). A stable source (such as a crystal reference) clocks a phase accumulator which provides the 'index' to the sine look-up table inside a Read-Only-Memory (ROM). The output of the look-up table goes to a DAC and is converted to a stepped sine wave. A typical block-diagram is shown below.

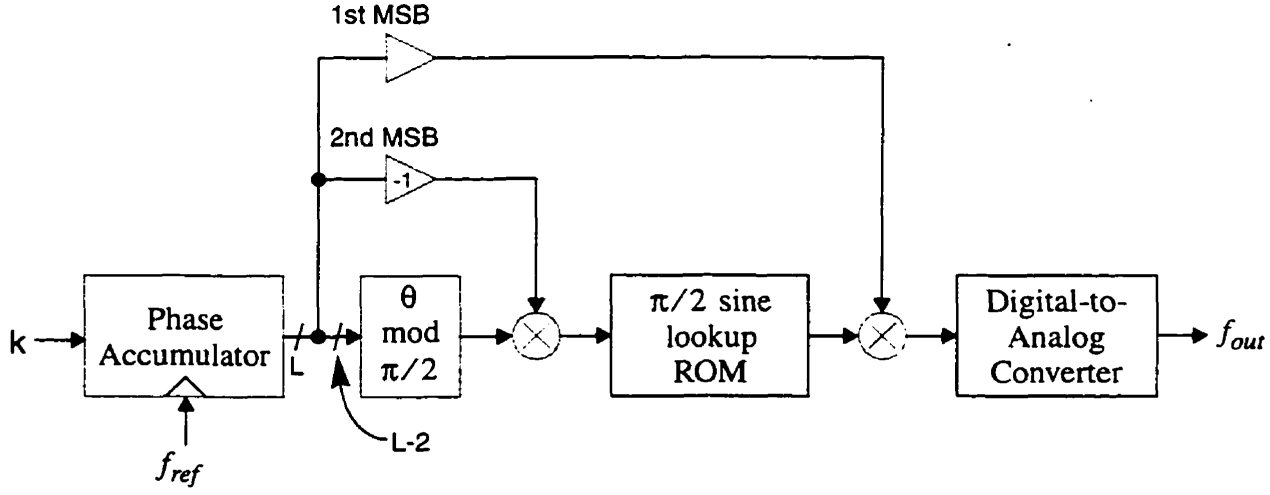


Figure 1.4 A Direct-Digital Frequency Synthesizer[3] which has exploited the $\sin(\theta)$ symmetries about π and $\pi/2$ for table compression

This architecture offers low phase jitter. Moreover, it can quickly switch output frequen-

cies and provide an output that is continuous. Some common techniques, being used for spurious suppression, include phase dithering and noise-shaping. However, the overall system is still very complex, and can only be used for relatively low frequencies with a reasonably low power dissipation.

Indirect Analog Synthesis

Indirect synthesis utilizes an oscillator which is controlled by a Phase-Locked-Loop (PLL) to generate its output frequency. This frequency can be an extracted clock from a data sequence or it can be a multiple of the reference clock. The PLL has often been used to track a slowly-varying signal to perform FM demodulation. It is also an attractive approach for frequency synthesis because it is relatively easy to design and integrate and requires less passive components and interface circuits.

General Phase Locked Loop

Frequency synthesizers that employ one or more PLLs may appear intimidating and difficult to understand. An intuitive understanding of a single-loop PLL operation can be explained by converting the PLL section to a general form given in Figure 1.5. The method of frequency translation is not specified and can be anything from a simple digital divider to a single sideband modulator that contains its own PLL. The PLL tunes the Voltage-Controlled Oscillator (VCO) until the phases and the frequencies of the signals applied to the Phase Detector (PD) are equal. Expressions are given below for the output of the frequency translation devices.

$$f_{ref} = F_r(f_{in}) \qquad f_{div} = F_d(f_{vco}) \tag{1.1}$$

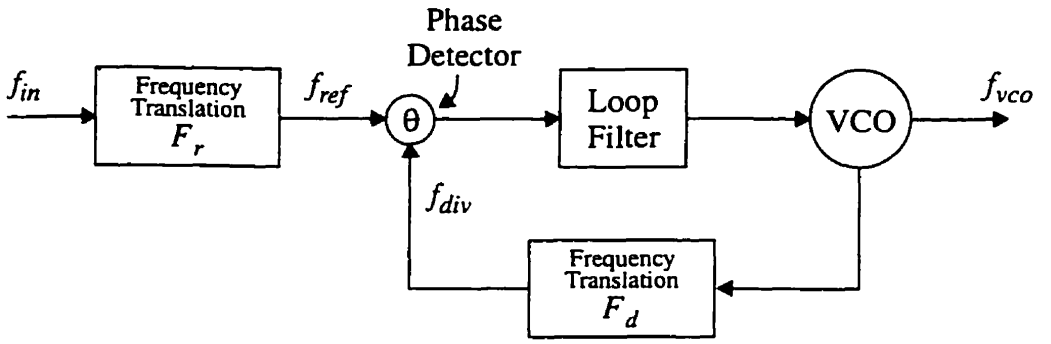


Figure 1.5 Block diagram of a phase-locked loop

Once the system is 'locked', the output frequency can be easily calculated by equating the signals at the input of the PD, resulting the expression in (1.2).

$$f_{ref} = f_{div} \text{ and hence } f_{vco} = F_d^{-1}(F_r(f_{in})) \qquad (1.2)$$

Another advantage of the PLL is the noise suppression it provides. The noise spectral components close to the average oscillation frequency of a VCO are suppressed when it is placed in a PLL. If the PD has low noise sidebands, the phase noise well within the bandwidth of the loop, ω_{pll} is given by:

$$\Phi_{vco}(f) = \Phi_{ref}(f) \cdot N \qquad f < \frac{\omega_{pll}}{2\pi} \qquad (1.3)$$

where N is the division ratio of the divider in the feedback path of the PLL, Φ_{vco} is the PSD of the VCO, and Φ_{ref} is the PSD of the reference oscillator.

The major disadvantage of the above frequency synthesis is the lengthy time it takes to switch the output frequency. The switching speed is usually at least ten times the period of f_{ref}. This limit arises from setting the PLL bandwidth to no wider than one tenth of the reference source. The filter cannot be widened because of the need to filter the reference source feed-through and to ensure that the loop is stable.

The PLL with an integer divider has a resolution equal to f_{ref}. For fine resolution, this implies a very low frequency. As the loop bandwidth cannot be larger than one tenth of f_{ref}, it leads to a very poor switching-speed performance ($t_{sw} > \frac{10}{f_{ref}}$). Furthermore, the loop will provide less noise suppression for the VCO. To achieve acceptable performance, a low-noise VCO is required. An indirect synthesizer similar to the PLL is the Frequency-Locked-Loop (FLL). In an FLL, a Frequency Detector (FD) is used to measure the difference in frequency between f_{ref} and f_{div}. The loop uses this information to tune the VCO until $f_{ref} = f_{div}$.

The FD usually requires extra components to extract the frequency information whereas the PD used in PLL is easy to be implemented by using merely digital circuits. Therefore, the PLL is much more popular in synthesizer applications than the FLL.

PLL for Frequency Synthesis

In a basic PLL, the frequency translation device is a frequency divider, typically implemented with a digital counter. In Figure 1.6, the reference frequency is divided by M while the output frequency is divided by N.

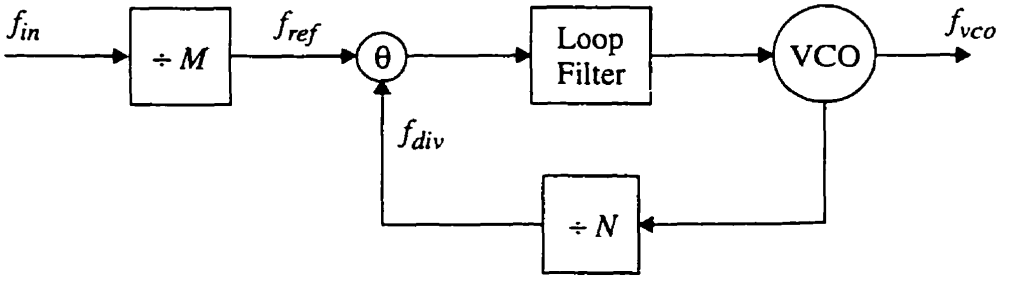


Figure 1.6 Basic phase-locked loop for frequency synthesis

The PLL forces the VCO to oscillate at a frequency where the two divided signals are equal. This relationship is given in (1.4).

$$f_{ref} = \frac{f_{in}}{M} \qquad f_{div} = \frac{f_{vco}}{N} \tag{1.4}$$

Solving for f_{vco} yields the standard expression for the synthesized signal:

$$f_{vco} = f_{in} \cdot \frac{N}{M} \tag{1.5}$$

This basic PLL provides many advantages in wireless applications. All the components are easily integrated and low power dissipation is often achieved. If the VCO is relatively quiet, good noise performance is feasible too. However, this loop still has a poor switching time.

Fractional-N Frequency Synthesis

The fractional-N technique modifies the classical indirect phase-locked loops to effectively permit the feedback divider to take a periodically changing division ratio and hence to give a non-integer ratio. For instance, if a fractional value of 1/8 is required, then the division ratio changes once (from N to $N+1$) every eighth cycle.

Figure 1.8 shows the architecture of a fractional-N synthesizer. An accumulator is a convenient device to control the division ratio because the number of occurrences of its carry-out equals the numerator of the fraction. For example, in Table 1, a 3-bit accumulator has 3 added to its output for each clock cycle, and consequently overflows on average three times every eight cycles, whenever its output would exceed the maximum of the accumulator.

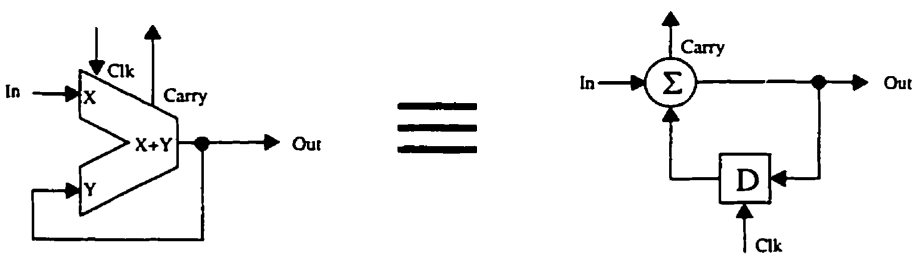


Figure 1.7 A typical implementation of an accumulator

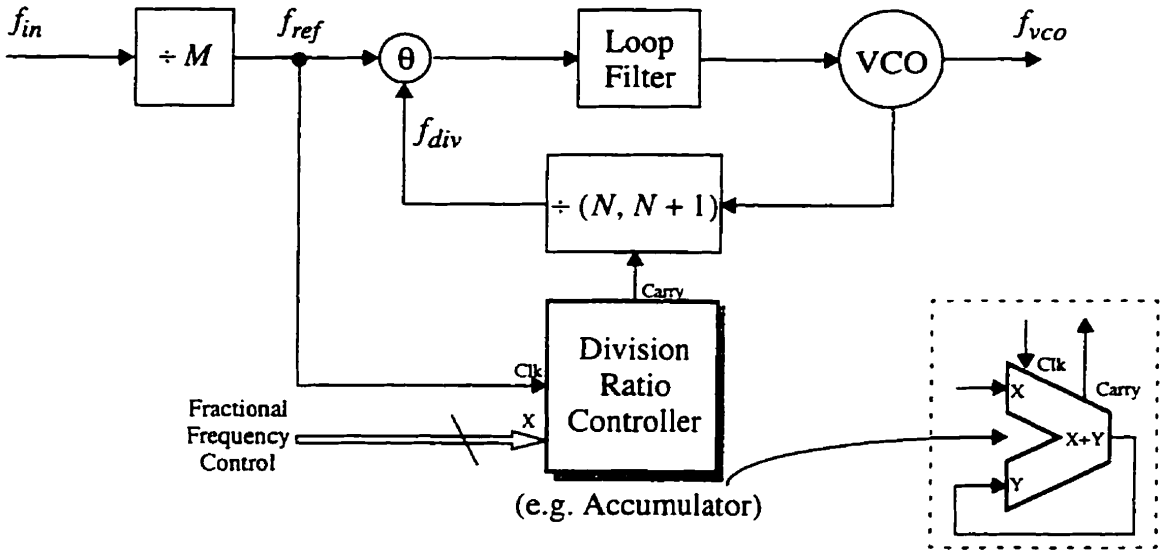


Figure 1.8 A basic fractional-N synthesizer

Accumulator content	Division Ratio
3	N
6	N
1(overflow)	N+1
4	N
7	N
2(overflow)	N+1
5	N
0(overflow)	N+1

Average division ratio = (8N+3)/8 = N+3/8

Table 1 Accumulator content for Figure 1.8

However there is a trade-off for the improvement in the frequency resolution. The manipulation of the division ratio generates phase perturbations, and hence spurious signals (or so-called beat note), which have to be eliminated in a useful synthesizer design. The nature of the phase perturbations is predictable and can be canceled out using an analogue correction system. For instance,

if the VCO output frequency is now changed from $N \cdot F_{ref}$ to $(N.g) \cdot F_{ref}$ while maintaining the feedback division ratio as N, the phase detector phase error takes on a sawtooth shape as given by [9]

$$\frac{\Delta\theta}{\Delta T} = \left(\frac{N + 0.g}{N}\right) F_{ref} \cdot T\left(\frac{2\pi}{T}\right) - F_{ref}\, T\left(\frac{2\pi}{T}\right) \tag{1.6}$$

This may be simplified to give

$$\frac{\Delta\theta}{\Delta T} = \left(\frac{2\pi\ F_{ref}\ 0.g}{N}\right) \bmod 2\pi \tag{1.7}$$

where $0.g$ denotes the fractional portion of the division ratio.

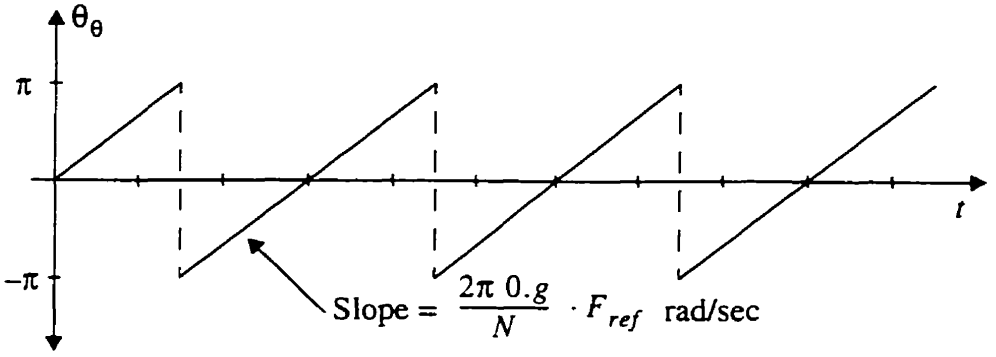


Figure 1.9 "Beat note" from the output of the phase detector

Many different solutions[9][10][11] which utilize various techniques, such as digiphase, to compensate the beat-note have been patented since as early as 1971.

However, there is a limit to the accuracy of the cancellation that can be achieved, and obtaining cancellation of better than 1% can be troublesome. In addition, the use of analogue components, i.e. ADCs, to correct for the beat note, greatly adds to complexity and power dissipation.

An ideal fractional-N system does not require any analogue components in order to get rid of these residual phase errors. Intuition suggests that this approach is not a practical possibility.

But a nearly complete digital solution has been devised and implemented in this thesis, showing the performance of a PLL can be virtually indistinguishable from that of the non-fractional loop operating at the same frequency ranges, and beyond.

A Comparison between DDS- and PLL-based Frequency Synthesizer

As for most of the modern sub-micron CMOS designs for DDS- and PLL-based frequency synthesizers, some of their tradeoffs on a mobile-communication standpoint are tabulated below.

Parameters	Phase-Locked Loop	Direct-Digital Synthesizer
Output Frequency Range	✓ ~ GHz	✗ < GHz
Switching Time	✗ $t_{sw} \propto \frac{1}{\omega_{loop}}$	✓ < 10 ns
Power Consumption	✓ 10 ~ 50 mW	✗ 2 ~ 20 W

It is obvious that the PLL-based frequency synthesis is a more appealing approach for the mobile communication in terms of its output frequency range and its power consumption than those of the DDS-based frequency synthesis. However, the switching time of the PLL is limited by its loop dynamics. Therefore, we shall discuss other methods to resolve this limitation in the next chapter.

1.3 Mixer Architecture

The linearity of an RF mixer usually is rather limited. The Gilbert topology is most commonly realized in bipolar technology. Its operation principle is based on a translinear configuration. Techniques like predistortion and emitter degeneration are necessary to obtain a reasonable lin-

earity. Imperfection in this kind of structure, combined with a limited matching, will render a third-order intercept point, IP3, which can only be slightly greater than 0 dBm[5]. In a CMOS technology, a double-balanced structure which cancels out the quadrature term of the MOS transistor was reported[6][7]. But these mixers only have a limited linearity which highly depends on matching, even more important is their limited frequency range.

In this thesis, part of effort has also been spent on designing the front-end RF mixer which gives a good linearity independent of mismatch and maintains the frequency range for the input signals.

1.4 References

[1] Steve Jantzi, Kenneth Martin, M.Snelgrove and Adel Sedra, "A Complex Bandpass ΔΣ Converter For Digital Radio," *ISSCC 1997, http://www.eecg.toronto.edu/~analog/PUBS/adel/www/ Complex_Bandpass_DS_Converter_for_Digital_Radio.ps*, University of Toronto, 1995

[2] William Gosling, ed., *Radio Receivers*, Peter Peregrins, London, 1986

[3] D. Sunderland *et al.*, "CMOS/SOS Frequency Synthesizer LSI circuit for Spread Spectrum communications," IEEE Journal on Solid-State Circuits, August 1984

[4] Bar-Giora Golderg and Henry Eisenson, "Frequency Synthesizer Strategies for Wireless," *MicroWave Journal*, June 1993, P.24-40

[5] H. Song and C.Kim, "A MOS four-quadrant analog multiplier using simple two-input squaring circuits with source followers," *IEEE J. Solid-State Circuits*, vol. 25, pp. 841-848, June 1990

[6] Peter Peregrinus, *Analogue IC design: the current-mode approach*, London, 1990

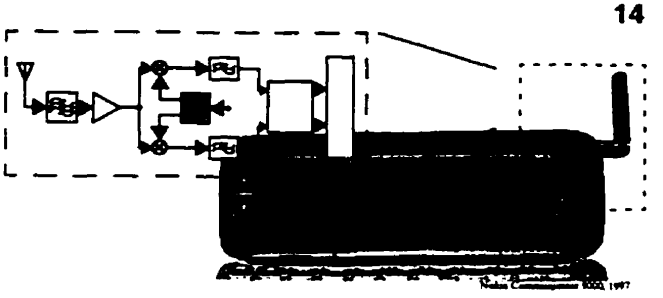
[7] D.Rabaey and J.Sevenhans, "The challenges for analog circuit design in mobile radio VLSI chips," in *Proc. AACD Workshop*, Leuven, Mar. 1993, Vol. 2, pp. 225-226

[8] A. Bruce Carlson, *Communication System*, 3rd. ed. McGraw-Hill, New York, 1986

[9] Dana Series 7000 Digiphase, Publication 980428 (manual), Dana Laboratories, 2401 Campus Drive, Irvine, CA 92664, 1973

[10] Egan, W.F., *Frequency Synthesis by Phase Lock*, John Wiley & Sons, New York, 1981

[11] Gillete, G.C., "Digiphase Principle," Frequency Technology, 1969



System Considerations

2

This chapter describes the system architecture, specifications of each building block, timing considerations and an analysis of jitter. Basic phase-locked-loops (PLLs) are generally well understood and so a detail analysis is not included. However, there are a number of books[13][14][15] which can be used for reference.

The quadrature receiver front-end is comprised of a dual-balanced mixer and a fractional-N frequency synthesizer. The main challenge lies in the design of the frequency synthesizer which is the most complicated and has to be immune from system interferences such as power supply noise, process variation and phase jitter. Our proposed type is an analog indirect version which is a modified PLL consisting of

- a voltage-controlled oscillator (VCO)
- a multi-modulus prescaler (PS)
- a phase modulator (PM)
- a frequency-phase detector (FPD) and
- a lowpass loop filter (LP).

2.1 Frequency Synthesizer

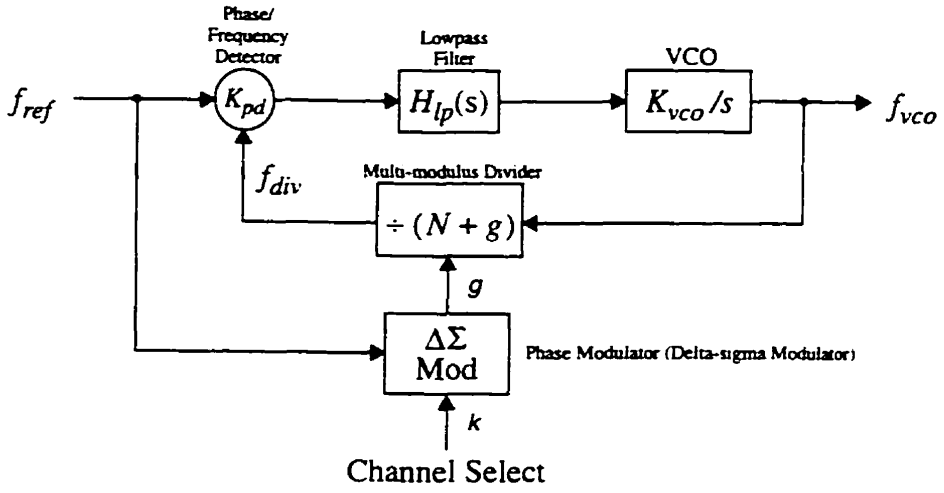


Figure 2.1 Proposed architecture for the fractional-N synthesizer

The above architecture of the frequency synthesizer has been studied extensively by a number of researchers[16][17] and is referred to as a "conventional delta-sigma fractional-N synthesizer". Its basic working principle is similar to that of the N/N+1 fractional-N design discussed in the previous chapter on page 9. However, a number of enhancements have been made in order to suppress the spurious noise output as well as to improve the feasibility of implementation in a CMOS process for RF applications. In the following sections, we shall discuss how the performance of this frequency synthesizer can be improved by:

1. Noise-shaping which further reduces the spurious phase noise

2. Frequency doubling which brings the output frequency higher and reduces the sloping sideband of the sinusoidal output (See Figure 2.5)

3. A high-speed phase selector embedded in the multi-modulus divider which eliminates extra logic in the prescaler, and makes it easier to interface with a multi-bit phase modulator in Figure 2.12

4. A precharge-type phase detector which provides a fine resolution for the phase difference.

Advanced Fractional-N Synthesis

For this kind of frequency synthesizer, the PLL still acts as a digitally-controlled frequency generator and as an analog reconstruction filter for the (digital) phase modulator. As shown in Figure 2.1, the phase modulator produces a bit stream, g, that contains the desired frequency control embedded in a stream of binary numbers. The average density of binary numbers controls the division ratio of the PLL and hence the output frequency of the synthesizer. The function of the phase modulator is to shape the noise spectrum of the quantization error, thereby reducing the spurious level in the passband of the PLL. Its effect can be shown by taking the Fourier transformation at the output of the phase detector. A typical result is shown in the following figure.

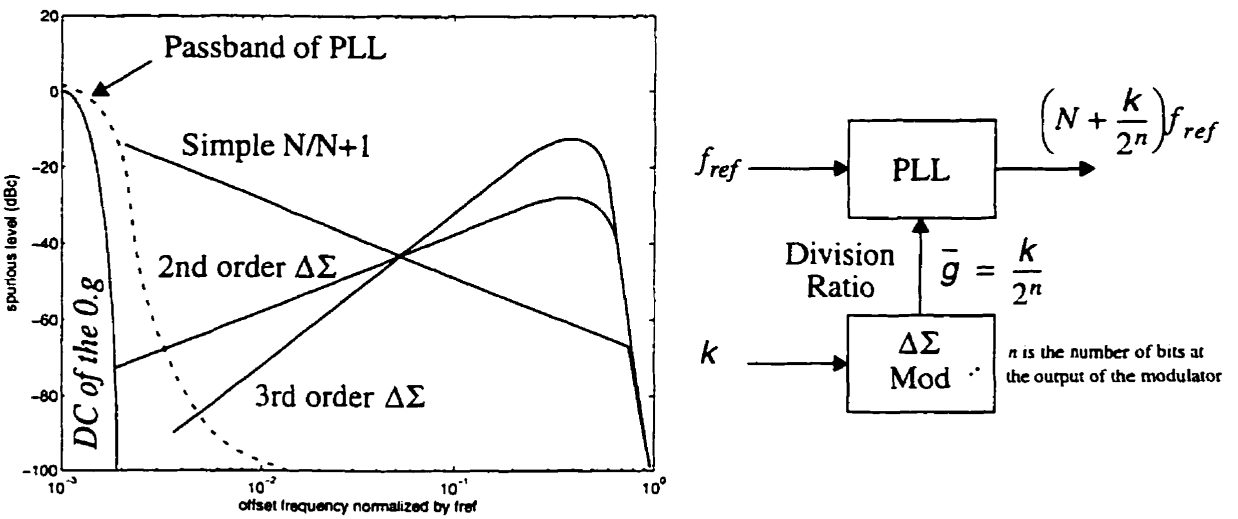


Figure 2.2 Spurious level with different orders of delta-sigma modulator

The spurious noise produced by the phase modulator can be substantially removed by the loop filter of the PLL. Simply speaking, the higher the order, the better suppression. A third-order modulator is enough however for most practical designs. A detailed analysis is discussed in the "Phase Modulator" section of this chapter.

2.2 Voltage-Controlled Oscillator

In this section, properties of the voltage-controlled oscillator (VCO) shall be discussed. The PLL shown in Figure 2.1 is used to synthesize a higher frequency by comparing the phase and the frequency of a reference source, typically a crystal oscillator, to those of the prescaler driven by the VCO. The loop corrects any phase and frequency deviation of the VCO caused by the noise and changes in operating conditions. However, these corrections can only be made up to the bandwidth of the loop. Frequency noise higher than the bandwidth remains un-attenuated. For this reason, the control loop acts as a highpass filter for noise generated by the VCO, but as a lowpass filter for noise input to the PLL. If there are any noise or changes in the operating conditions that are faster than the bandwidth of the loop, they will appear at the VCO output. Besides, any low-frequency noise in the input signal will feed through to the output, up to the bandwidth of the loop. These ideas can be more easily illustrated by writing loop equations with respect to different sources.

The close-loop transfer function, $H(s)$, from the f_{ref} to the PLL's output is given by

$$H(s) \equiv \frac{\Phi_{vco}(s)}{\Phi_{ref}(s)} = \frac{K_{pd}H_{lp}(s)\dfrac{K_{vco}}{s}}{1 + K_{pd}H_{lp}s\dfrac{K_{vco}}{sN}} = N\left(1 - \frac{1}{1 + K_{pd}H_{lp}(s)\dfrac{K_{vco}}{sN}}\right) \tag{2.1}$$

The noise transfer function, $H_{vn}(s)$, from the VCO to the PLL's output.

$$H_{vn}(s) \equiv \frac{\Phi_{vn}(s)}{\Phi_{vco}(s)} = \frac{1}{1 + K_{pd}H_{lp}(s)\dfrac{K_{vco}}{sN}} \tag{2.2}$$

The noise specifications for a local oscillator (LO) in communication applications are always very strict. An ideal LO has a spectrum of a pure carrier with no noise sidebands. How-

ever, every oscillator has noise that degrades the performance of the transceiver. The "close-in" noise degrades the Signal-to-Noise Ratio (SNR) at the output of the demodulator. The higher frequency sideband noise degrades the adjacent channel selectivity due to nonlinearities in the mixer. Noise at even-higher frequencies will limit the dynamic range (a measure of the ability to receive weak signals in the presence of strong signals at different frequencies) of the system.

When RF architectures are initially designed, the LO is assumed to be ideally pure, precise and agile. As the design progresses, the LO architecture can achieve the required precision and agility, but still it is assumed to be ideally pure. As the design advances further, the purity of the LO becomes an important issue because it can limit the SNR of the transmitted and received signals, and be a limiting factor in determining how wide the transmission bandwidths of two communication channels can be.

Noise in the receiver

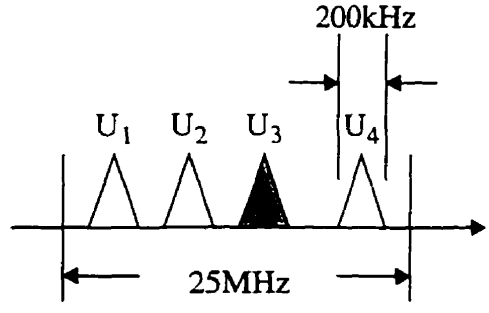


Figure 2.3 A downlink transmission spectrum in GSM (FDMA is used)

A well-designed LO used in a receiver should not limit the performance of the transceiver. Our proposed receiver (See Figure 1.1) requires that the received signal have an SNR of at least 30 dB[19] which is a reasonable value in many SSB systems. This requirement limits the amount of noise that can be tolerated in the LO. The problem of noise in the LO can be demonstrated by looking at a down-conversion example. A sample-channel spectrum is depicted in Figure 2.3.

Suppose it is desired to downconvert the signal transmitted by User 3. If User 3 is downconverted by an ideal sinewave, only User 3 will appear at the baseband. However, if the LO is not an ideal sinewave, any noise around the LO will also downconvert the channels of other users to the baseband. These other users will appear as noise to the detector and degrade the SNR of the received signal.

All oscillators have sideband noise, so it is important to determine the amount which is acceptable. An idealized power spectrum of an LO is given in Figure 2.4. It consists of an impulse at the desired frequency of operation and flat noise sidebands with a noise density given in dB/Hz below the carrier. The noise sidebands (B_{nSB}) beyond $\pm$ 25 MHz will not contribute noise because the received signal will be filtered in the baseband after it is demodulated. In an actual LO's power spectrum, the sideband noise will rise up from the noise floor close to the impulse (as indicated by the dotted region in Figure 2.4). These sloping sidebands or "near-in noise" shall initially be ignored in this analysis. However, they are very important because they determine the minimum channel spacing by degrading the received signal exactly like the flat sideband noise.

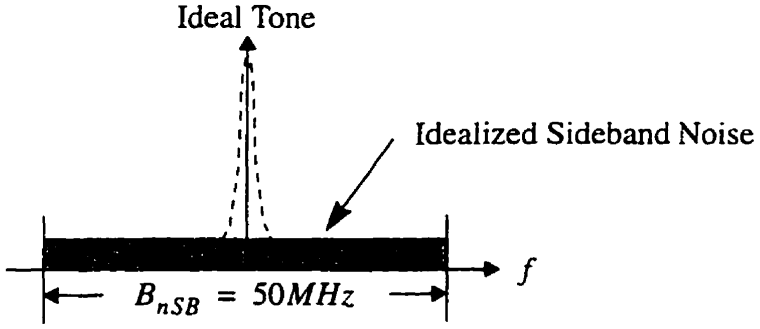


Figure 2.4 Idealized local oscillator power spectrum

In a fading channel, the transceiver architecture depends on diversity, not extra power, to improve the Signal-to-Noise-Ratio (SNR). We can assume that the average power of all users is usually constant. This assumption becomes more accurate as the number of users increases and is

a valid assumption for systems with approximately 50 users[19]. Additionally, the relative signal level of the desired user to the other users is highly variable and can differ by as much as 30 dB. This variability is accounted for by adding a 15 dB margin to the 15 dB SNR required for reliable transmission. These assumptions determine the mean noise level requirements.

The total noise power folded onto the received signal, P_{TN}, is the product of the sideband power spectral density (PSD), the user bandwidth, and the number of users.

$$P_{TN} = P_{SB} B_{user} N_{user} \tag{2.3}$$

If we divide both sides of equation (2.3) by the signal power, the left-hand side will become the reciprocal of the required SNR. The PSD of the sideband noise, P_{SB}, relative to the signal is now equal to $(SNR \cdot B_{user} \cdot N_{user})^{-1}$. By inserting 30 dB for the SNR, a user bandwidth of 200 kHz, and 50 users, the PSD of the sideband noise must be 100 dB/Hz below the carrier.

Effect of Near-in Noise

In the previous section, the local oscillator was assumed to have an impulse at the desired frequency and a flat noise floor limited to the transmission bandwidth. In reality, the noise floor is amplified by the oscillator and causes the flat-band noise to rise towards the carrier as below.

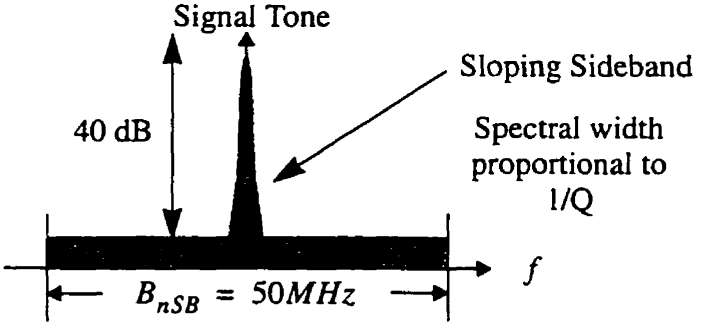


Figure 2.5 More realistic local oscillator power spectrum

Therefore it is named as the sloping sideband or the "near-in" noise. The sideband noise in the

LO is typically at a reasonably low level beyond 300 kHz (including the channel bandwidth and the guard-band). As a result, the sloping sideband noise within the user bandwidth will dominate the noise performance of the LO. The worst case occurs when the received signal has an unacceptable SNR level even without the presence of any other users. In order to prevent this, the SNR within the channel bandwidth must be at least 40dB. This completes the preliminary specifications of the local oscillator which are summarized in the following table.

Specifications	Value
Maximum Frequency	~900MHz
Required Turning Range	800±50 MHz
Flat-band Noise Floor	-100dB/Hz
In-band SNR (300kHz)	40dB

Table 2 Specifications of the voltage-controlled oscillator (VCO)

Effects of the Phase Jitter

The r.m.s. phase jitter is also another important parameter. It defines the instability of the generated signal relative to the reference signal. We measure it by recording the time delay from the zero crossing of the reference to that of the LO's output and calculating the r.m.s. value. Jitter is usually normalized to the period of the LO frequency and expressed as a percentage of the period or converted to degrees.

The output of an oscillator can be written as

$$V(t) = [V_o + \varepsilon(t)] \sin[2\pi f_o t + \phi(t)] \tag{2.4}$$

where the amplitude variation is represented by $\varepsilon(t)$, the nominal frequency is given by f_o, and $\phi(t)$ is a random process representing the phase noise. $\varepsilon(t)$ is assumed to be mean-zero and

only the phase noise contribution is considered.

Assume there is a deterministic sinusoidal variation in the phase, i.e. a sinusoidal phase modulation, where

$$\phi(t) = \Delta\theta \sin(\omega_m t) \quad \text{with} \quad |\Delta\theta| \ll \frac{\pi}{2} \tag{2.5}$$

Substituting (2.5) into (2.4) and expanding by means of the trigonometry,

$$V(t) = V_o \sin(2\pi f_0 t) + \frac{V_o \Delta\theta}{2}\{\sin[(2\pi f_0 + \omega_m)t] - \sin[(2\pi f_0 - \omega_m)t]\} \tag{2.6}$$

The resulting spectrum is shown in Figure 2.6. In arriving at this result, we have assumed that small angle assumption is applicable, i.e. $|\Delta\theta| \ll \frac{\pi}{2}$.. Otherwise, a more rigorous derivation in [20] must be followed. These extra tones, beside the central one, modulate the noise floor and increase the in-band noise.

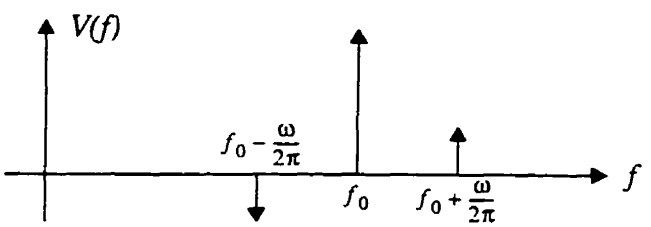


Figure 2.6 First-order spectrum for sinusoidal PM

Statistical Model

Now, if the phase and the amplitude are not deterministic, a statistical approach must be taken. We begin with a summary of derivations given in [21]. To simplify the calculations and be intuitive, we assume that the communication circuits require low-noise design, and the amplitude variations shall be small. Variations in amplitude are not as important as those in frequency because the PLL will drive a double-balanced mixer configured in an amplitude-insensitive Gilbert topology (except at the point where the switches in the mixer fully turn on and off).

Assume that the output noise of LO has a bandwidth B_o centered on f_o. If the noise is white with a spectral density of N_o, then the filtered noise is given by Φ_n as shown in Figure 2.7.

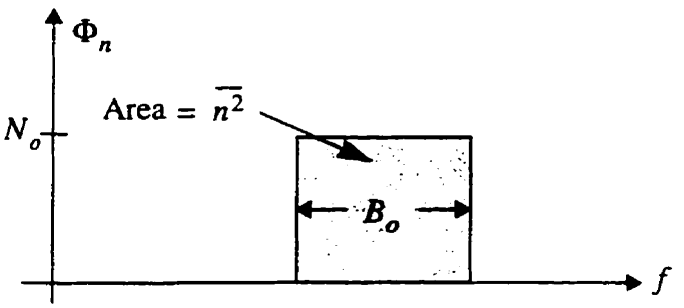


Figure 2.7 Power spectral density of output noise components

The total noise power given by the integral of the noise density, can be written as the product of the noise density and the noise equivalent bandwidth, B_o.

$$\overline{n^2} = N_o B_o \tag{2.7}$$

The noise can be broken up into quadrature components as follows:

$$\vec{n} = \vec{n_x} + \vec{n_y} \qquad n_x = x \sin\omega_o t \qquad n_y = y \cos\omega_o t \tag{2.8}$$

where x and y are independent random variables that change as a function of time.

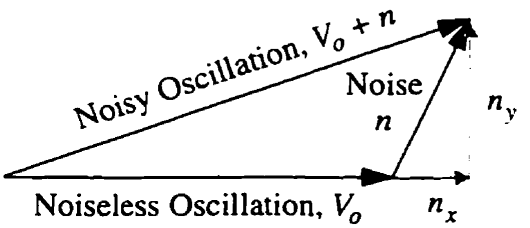


Figure 2.8 Quadrature noise added to a noiseless oscillation

The quadrature noise sources are shown in Figure 2.8. In a mean-square sense, the total noise is

$$\begin{aligned} \overline{n^2} &= \overline{n_x^2} + 2\overline{n_x} \cdot \overline{n_y} + \overline{n_y^2} \\ &= \overline{n_x^2} + \overline{n_y^2} \qquad (\overline{n_x} \cdot \overline{n_y} = 0) \end{aligned} \tag{2.9}$$

When the *sin* and *cos* functions are established in (2.8), the phase reference is arbitrary

and thus $\overline{n_x^2} = \overline{n_y^2}$. Using the equalities in (2.7) and (2.9), the total power for each component is

$$\overline{n_x^2} = \overline{n_y^2} = \frac{\overline{n^2}}{2} = \frac{N_o B_o}{2} \tag{2.10}$$

Since each quadrature component occupies the same bandwidth as the original filter spectrum does, the density of each is simply $N_o/2$. The power of the random time functions x and y can be evaluated by equating the power of the quadrature components with the mean-square value of the time functions.

$$\overline{n_x^2} = \overline{(x\sin\omega_o t)^2} = \overline{x^2(\sin\omega_o t)^2} = \frac{\overline{x^2}}{2} \tag{2.11}$$

$$\overline{n_y^2} = \overline{(x\cos\omega_o t)^2} = \overline{y^2(\cos\omega_o t)^2} = \frac{\overline{y^2}}{2} \tag{2.12}$$

Since the noise power of a single quadrature component, given by (2.10), is $N_o B_o/2$, the power of the random time functions is given by $\overline{x^2} = \overline{y^2} = \overline{n^2} = N_o B_o$.

By considering the original expression of the ideal LO with additive noise, the random time functions (2.8) are now substituted for n.

$$\begin{aligned} V + n &= V_o\sin\omega_o t + x\sin\omega_o t + y\cos\omega_o t \\ &= (V_o + x)\sin\omega_o t + y\cos\omega_o t \end{aligned} \tag{2.13}$$

For small angle variations due to y, (2.13) can be approximated by:

$$V + n \approx (V_o + x)\sin(\omega_o t + \theta_o) \tag{2.14}$$

where θ_o is given by, $\theta_o = \text{atan}\left(\frac{y}{V_o + x}\right) \approx \text{atan}\left(\frac{y}{V_o}\right) \approx \frac{y}{V_o}$ (2.15)

As we compare (2.14) and (2.15) with (2.4), the noise expressed as n_x results in amplitude modulation of the LO while n_y results in angle modulation of the LO. Because the r.m.s. of y equals

N_oB_o, the phase-induced noise is

$$\overline{\theta_o^2} = \frac{\overline{y^2}}{V_o^2} = \frac{N_oB_o}{V_o^2} = \frac{\overline{n^2}}{V_o^2} = \frac{1}{SNR} \ (rad^2) \tag{2.16}$$

By examining (2.16), the output jitter of the LO given in radians is the inverse of the Signal-to-Noise ratio (SNR) which is equal to the integral of the noise spectrum normalized to the squared amplitude of the output signal. This equation is very convenient to compare the performance of different oscillations when a PSD is not easily available. For an SNR = 40dB, the maximum r.m.s θ_o allowed is $\frac{180}{\pi}\sqrt{\frac{1}{SNR}} = \frac{180}{\pi}\sqrt{\frac{1}{10^2}} = 5.73$ degrees.

Accumulative Jitter inside the PLL

Timing jitter in a ring-oscillator PLL not only depends on the interaction of noise in the oscillator, but also on the dynamics of the PLL. In the VCO, each timing error determines the starting point of the next oscillation cycle which, in turns, creates a permanent phase shift in the overall output. If the VCO is configured in a PLL, however, the phase difference between the reference clock, f_{ref}, and the prescaler's output is detected and compensated by the dynamics of the loop. The phase detector will then sense the shift and initiate an error signal to change the frequency of the VCO in a such way that moves the phase of the output to minimize their difference.

Since the amount of phase adjustment is usually small, the phase error cannot be corrected in one clock cycle but is reduced gradually over several cycles. The phase error may accumulate up over several hundred cycles, depending on the bandwidth of the loop filter.

In order to estimate the accumulated r.m.s. jitter, we assume that the PLL has a sequential

phase detector, which can be represented by a simple discrete-time model as shown below.

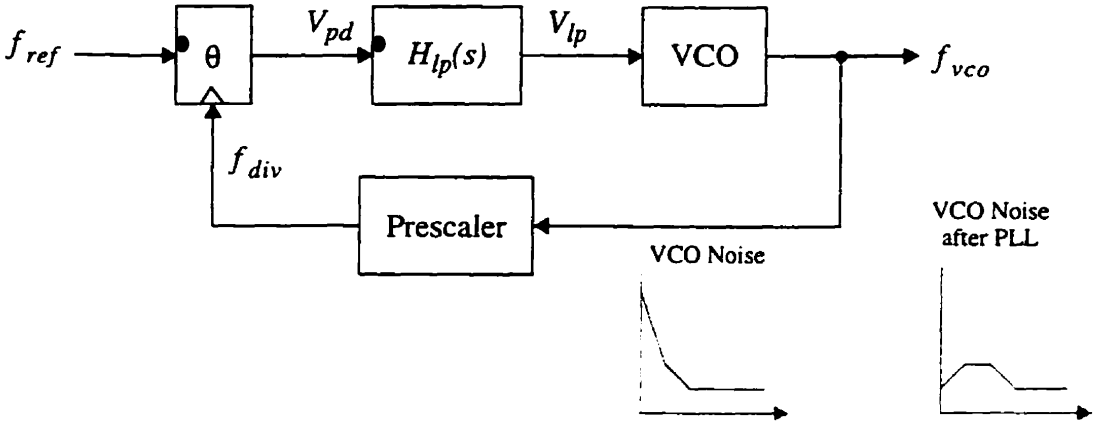


Figure 2.9 A simplified discrete model of the PLL with phase noise injection

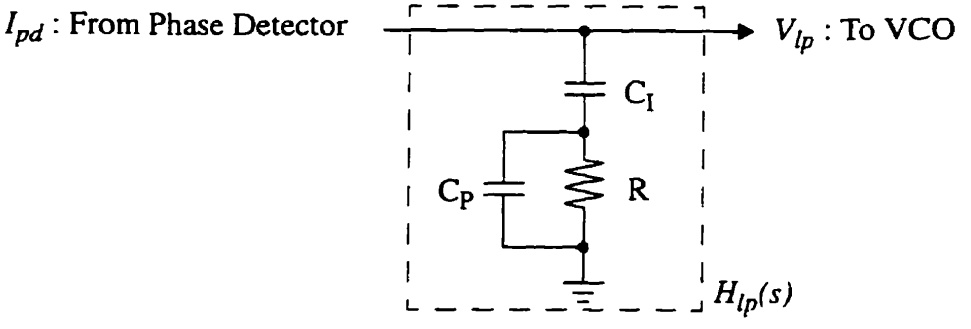


Figure 2.10 A second order lead-lag filter used as the loop filter

In most PLL designs, a second-order loop filter is used and its transfer function is given by,

$$H_{lp}(s) = \frac{a(s+n_1)}{s(s+p_1)} \tag{2.17}$$

where the DC gain of the filter, $a = \frac{1}{C_p}$, a zero, $n_1 = \frac{1}{C_I R}$, and a pole, $p_1 = \frac{C_I + C_P}{C_I C_P R}$. In most cases, the capacitor C_P does not affect the bandwidth of a PLL and can be neglected for simplicity. In this case, $H_{lp}(s)$ is reduced to $\frac{a(s+n_1)}{s}$ where $a = R$ and $n_1 = 1/RC_I$. Before we derive the z-domain transfer functions, let us assume that the sampling frequency, $1/T$, which is several times of the VCO's maximum frequency, i.e. $1/T \gg f_{vco}$, is much greater than the pole fre-

quency of the loop filter, i.e. $n_1 T \ll 1$. Applying the Forward-Euler transformation[1] (i.e. $s = \frac{z-1}{T}$) and the condition, $n_1 T \ll 1$, to (2.2), we obtain the transfer function for the phase jitter as,

$$H_{vn}(z) = \frac{(1-z^{-1})}{1-(1-\varepsilon)z^{-1}} = \frac{\Phi_{vn}(z)}{\Phi_{vco}(z)} \tag{2.18}$$

where $\varepsilon = K_{pd}K_{vco}aT/N$ and $\varepsilon \ll 1$.

The phase jitter from the VCO can be modeled as a sequence of unit step phase jumps with random magnitude. A single phase jump at time kT can be represented [22] in z-domain by,

$$\Phi_n(z) = \frac{2\pi}{T}\frac{\Delta\tau_k}{1-z^{-1}} \tag{2.19}$$

The magnitude of each error step is Δt_k . And hence the output jitter is,

$$\Phi_{on}(z) = H_{vn}(z)\Phi_n(z) = \frac{2\pi\Delta\tau_k}{T(1-(1-\varepsilon)z^{-1})} \tag{2.20}$$

For all events up to time MT, the sum of output phase shifts is represented by,

$$\sum\Phi_{on_i}(nT) = \sum_{k=-\infty}^{M}\frac{2\pi\Delta\tau_k}{T}(1-\varepsilon)^{M-k} \tag{2.21}$$

To find the r.m.s. output jitter, the expectation of its squared value can be calculated as [22],

$$E[\Phi_{on}^2(nt)] = \left(\frac{2\pi}{T}\right)^2\frac{\overline{\Delta\tau^2}}{\varepsilon(2-\varepsilon)} \approx \left(\frac{2\pi}{T}\right)^2\left(\frac{\overline{\Delta\tau^2}}{2\varepsilon}\right) \tag{2.22}$$

provided that $\Delta\tau_k$ and $\Delta\tau_l$ are not correlated when $k \neq l$.

1. Forward-Euler Transformation maps the j ω-axis to a shifted z-plane, which is often used in modeling highly oversampled systems, such as PLLs.

The r.m.s. accumulated phase jitter is, $\sqrt{E[\Phi_{on}^2(nt)]} = \sqrt{\frac{\Delta\tau^2}{2\varepsilon}\frac{2\pi}{T}} = \sqrt{\frac{1}{2\varepsilon}}\sqrt{\overline{\theta_o^2}} = \alpha\sqrt{\overline{\theta_o^2}}$ where $\sqrt{\overline{\theta_o^2}}$ can be obtained from (2.16), and $\alpha = \sqrt{\frac{N}{2K_{pd}K_{vco}aT}}$ is defined as the accumulation factor.

In conclusion, the r.m.s. timing jitter in a PLL is α times larger than the intrinsic jitter in the VCO. The accumulation factor α is inversely proportional to the square-root of $K_{pd}K_{vco}aT$ and in this case shows little dependency on C_1 and C_P. Therefore, as long as $C_P \ll C_1$ and stability requirements are met [23], the jitter accumulation factor can be lowered by increasing the bandwidth of the loop, $\omega_L \approx K_{pd}K_{vco}a$. This result is a guideline for use during the design of the loop filter.

2.3 Prescaler in the Multi-Modulus Divider

The term "prescaler" refers to a non-programmable divider with a high operating frequency. The challenge in designing a prescaler is to minimize the power consumption of the programmable divider while allowing the use of higher VCO frequencies. High-speed prescalers are often constructed in a fast logic family like Bipolar ECL but seldom in CMOS.

The prescaler is the feedback element that forces the VCO output to be a multiple of the reference frequency. Just as in any negative-feedback system with enough forward-path gain, the transfer function reduces to the inverse of the feedback element. In the case of the PLL, this forces the input frequency to be scaled up by the division ratio of the prescaler which may or may not be a constant integer. For the case of the fractional-N frequency synthesis, it is not.

Problems arise if the maximum operating frequency of the VCO is faster than that of the prescaler. For instant, if the VCO begins to oscillate at a frequency beyond the range of the pres-

caler, the output of the prescaler will either be a constant or possibly the natural frequency of the divider, which are both slower than the reference frequency. The loop will respond by forcing the VCO to oscillate faster until the output of the loop filter becomes saturated and the VCO is trapped at its highest output frequency. As the prescaler must operate at a frequency higher than that of the VCO, this circuit is not trivial. The speed of the prescaler is the ultimate limiting factor in the design of most frequency synthesizers.

Conventional Dual-Modulus Divider

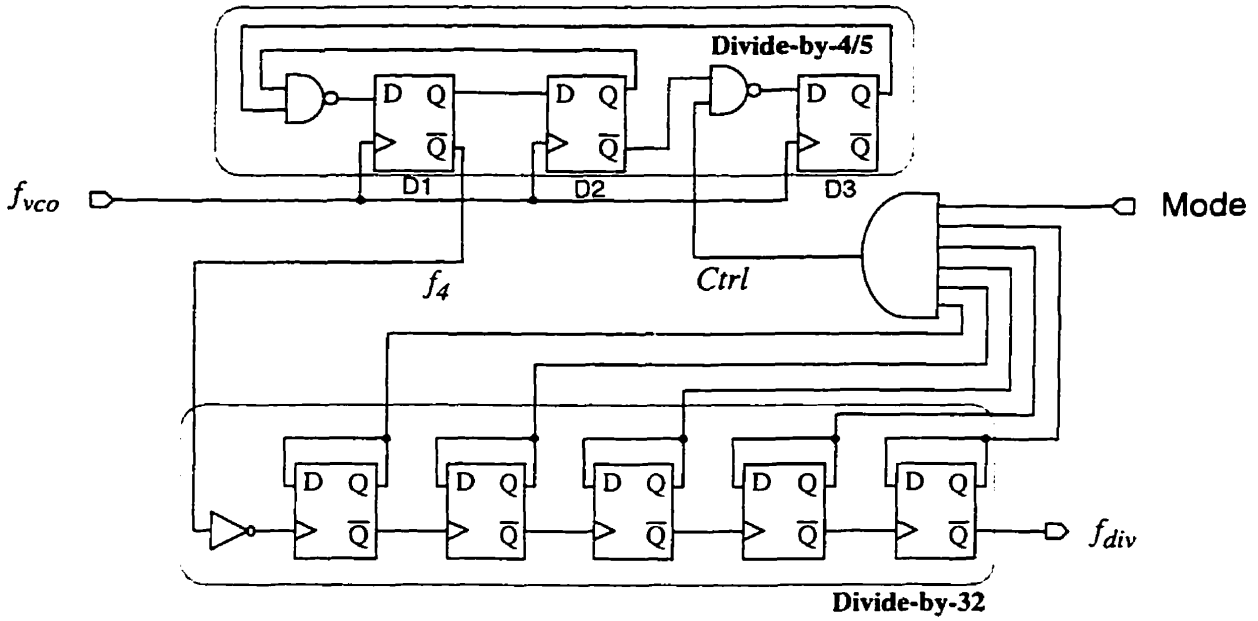


Figure 2.11 A traditional dual-modulus(128/129) divider

A common high-speed dual-modulus divider [24] consists of a synchronous divide-by-4/5 and an asynchronous divide-by-32 circuit as shown in Figure 2.11. The synchronous divider is the only part which always operates at the maximum frequency. If the *Ctrl* is low, the intermediate frequency f_4 generated by the two D-flip-flops(D1, D2) will equal one-fourth of the input frequency, f_{vco}. The asynchronous dividers at the bottom will divide the f_4 by 32 so that the output frequency, f_{div}, equals 1/128 of the f_{vco}. On the other hand, Divide-by-129 is accomplished by setting the

mode input high. As a result, whenever the asynchronous dividers reach a count of 127, the synchronous divider goes through an extra delay, D3, resulting in an additional count. So the last count will be a divide-by-5 and the total division ratio will be 129.

The main drawbacks of this kind of prescaler design are its speed and power consumption. The NAND gate inside the critical path of the synchronous divider can never be eliminated completely. Another serious problem is the synchronous divider which includes three fully functional D flip-flips. They consume large amount of power for their high frequency inputs. As a result, this kind of dual-modulus prescaler always have a slower operating speed than that of a complete asynchronous divider.

Full-Speed Prescaler

A dual-modulus prescaler proposed in [25] is shown in Figure 2.12. It consists of two high-speed divide-by-2 circuits, a phase-selector, and six low-speed divide-by-2 building blocks. The two right-most dividers are optimized for the high-speed divide-by-2 operation. The dual-modulus operation is based on the fact that a 90-degree phase shift of a divided-by-4 signal is equal to one clock cycle of the input signal. A delay of a complete input-clock cycle can be controlled. In other words, a division ratio can now be changed from N to N+1. We can extend this idea to generate division ratios of N+2, and even N-1.

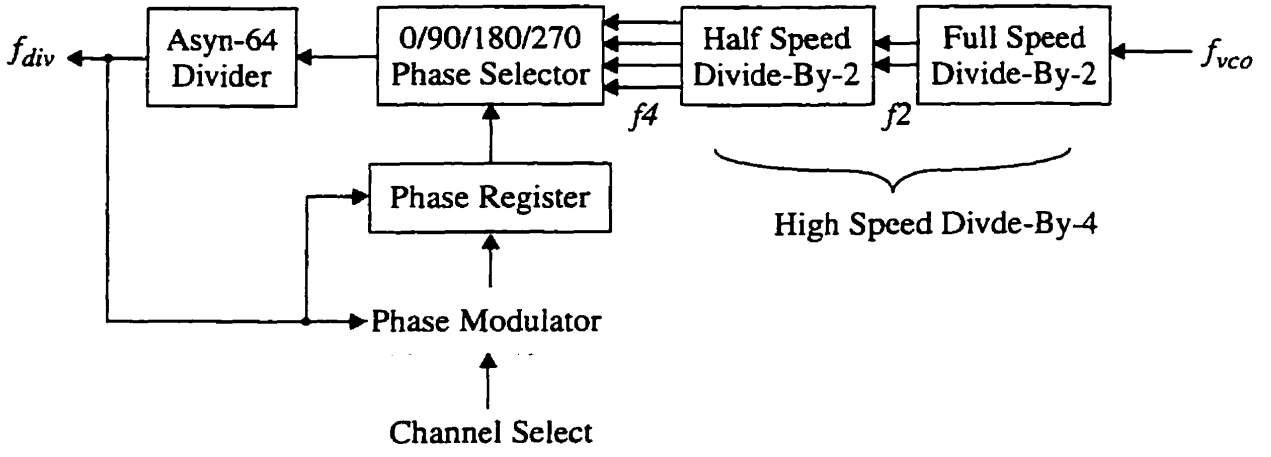


Figure 2.12 Full-speed multi-modulus (255/256/257/258) prescaler

High-Speed Divide-by-2 Divider

As this divider has to operate at the highest possible speed, a fast structure must be used. Some of the proposed structures make use of the CMOS dynamic D-flip-flops[26] or the level-triggered latches[27]. However, they operate with a 5V power supply, and their speed decreases drastically at a lower voltage.

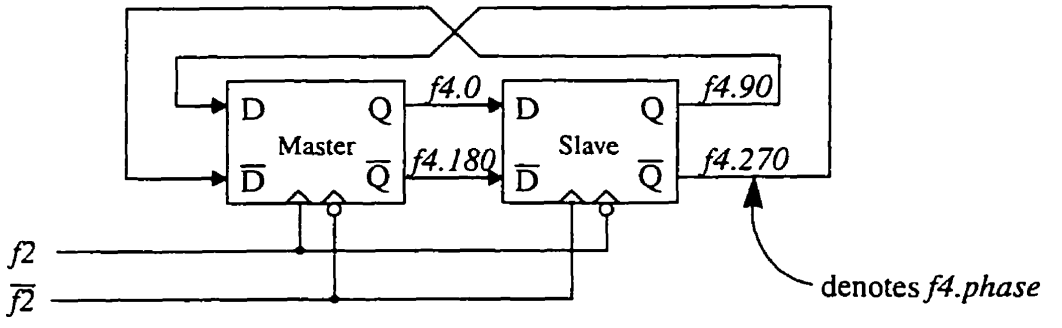


Figure 2.13 Half-speed master-slave divide-by-2 (The full-speed divider is the same as the above except only the 0 and 180 outputs are used)

We make use of two D flip-flops configured in a master-slave style to implement the divide-by-2 as shown above. In order to run at the maximum speed, a differential signal, f_{vco}, is fed to the first full-speed divide-by-2 (See Figure 2.12). The second divide-by-2 reduces the frequency down to one-fourth of the original frequency. Since they are running at frequencies of f_{vco}

and f_{vco} / 2, they have to be fast and simple. Because we only need the divide-by-2 operation, a fully functional flip-flop is not required. A simple latch and hold is sufficient for this application. This circuit will be discussed in detail in the next chapter.

Phase Selector

The principle of emulating different division ratios is best illustrated by the timing diagram as shown in Figure 2.14.

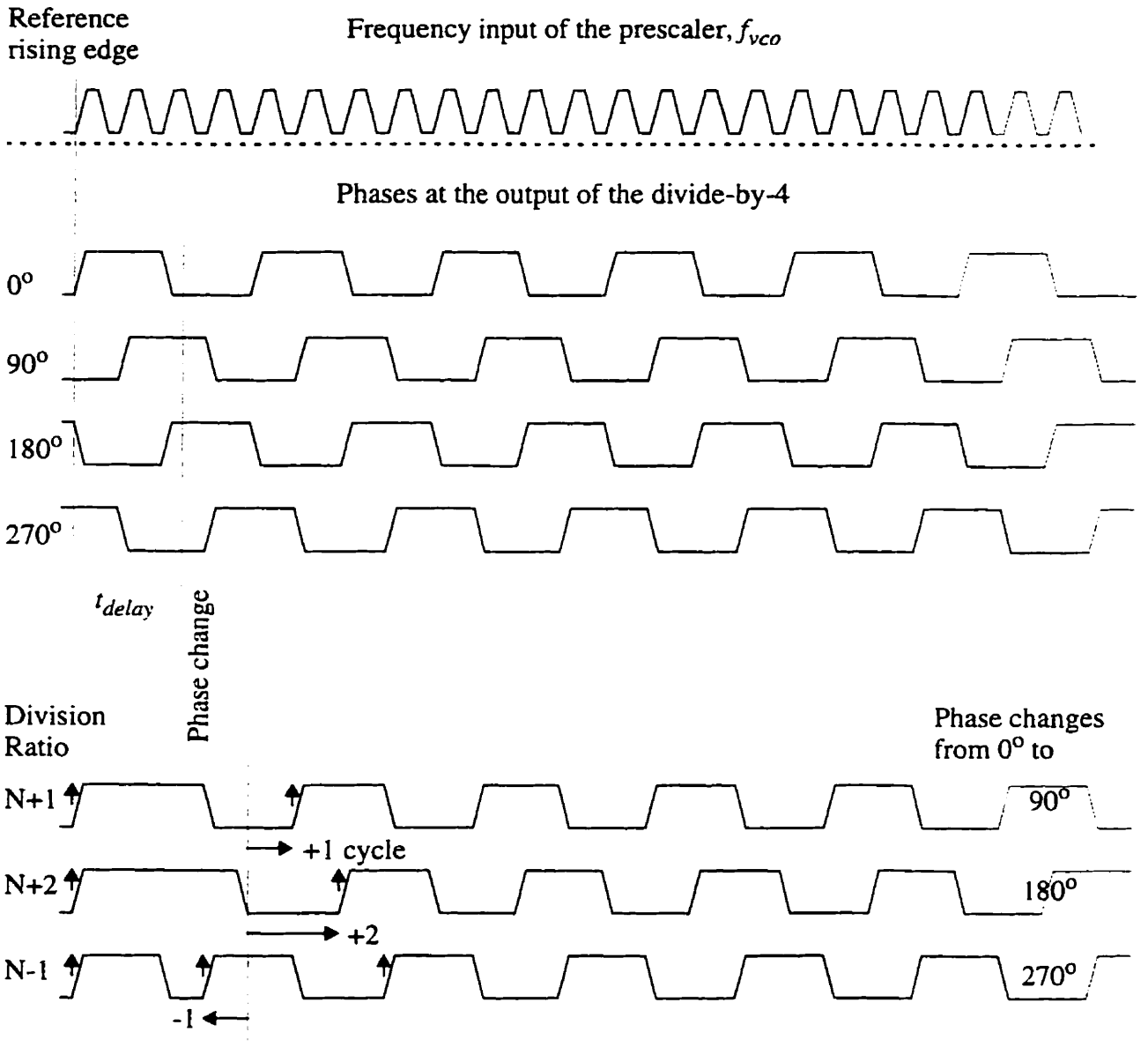


Figure 2.14 Phase selection principle

If the phase selector stays in one of the phases, the overall division ratio will be $2 \times 2 \times 64 = 256$. A divide-by-(256 + n) operation is made possible by delaying or advancing one of the rising edges within a complete 256-division cycle. The time of delaying or advancing is controlled by the phase modulator. The beauty of the circuit is its simplicity to emulate the required division ratio. However, we have assumed several properties which are critical when we design the dividers.

Design guidelines to be taken:

1) The time delay, t_{delay}, from the reference rising edge to the phase change has to be constant.

2) The output waveform of the full speed and half speed dividers has to be symmetrical, i.e. 50% duty cycle.

3) The functional speed of the asynchronous-64 divider is no greater than 1/2 of the input frequency, f_{vco}. Of course, it must also be able to toggle faster than 1/3 of the f_{vco}, mainly for the *N-1* division.

Owing to guideline 3, we design the asynchronous-64 divider to be a series of six fully functional flip-flops whose maximum speed, f_{max}, must be set and verified by Spice simulation to ensure $1.1 \times f_{vco}/3 < f_{max} < f_{vco}/2$. A margin of 10% has been taken into account.

Low-Speed Asynchronous Frequency Divider

The low speed divide-by-64 divider consists of a chain of six simple D-latch flip-flops (DFFs). By connecting the inverted output of each DFF to its input, the DFF acts as a simple divide-by-2 circuit. It is cascadable and requires the least amount of circuitry. Therefore it can operate at the highest speed while consuming a reasonable amount of power. The maximum operating speed is about one-half of the f_{vco}, so a standard and asynchronously resetable flip-flop can be used.

2.4 Phase Modulator

The phase modulator is the core of the fractional-N synthesis. It generates the fractional division ratio, $0.g$, by distributing a series of integer outputs whose average over time equals the desired fractional value. The simplest type has been discussed in the previous chapter. However, in order to achieve a better spurious performance, more advanced concepts based on the oversampling delta-sigma techniques need to be applied.

First-Order Modulator

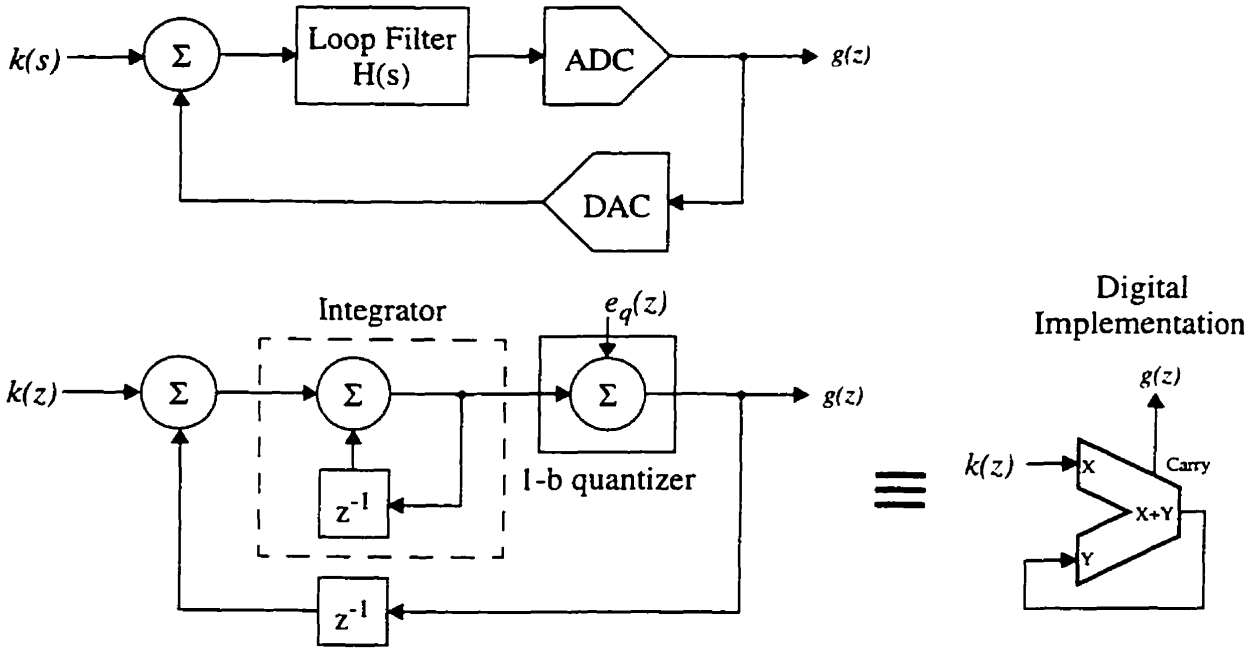


Figure 2.15 A typical 1-bit delta-sigma modulator and its discrete-time model

If the analog-to-digital converter (ADC) and digital-to-analog converter (DAC) are assumed to be perfect, the only error introduced by these components will be the quantization noise. It is uniformly-distributed and has a variance (σ^2) of $LSB^2/12$, where LSB is the least significant bit. If the loop gain is high, the output voltage, $g(z)$, will track the input voltage, $k(z)$, for

all frequencies within the close-loop 3dB bandwidth. The quantization is also suppressed over the same frequency range. The sampling rate F_s is usually much greater than the close-loop bandwidth used.

If the channel select in Figure 2.1 is analogous to the input voltage in Figure 2.15 and the division ratio control (e.g. the output of the phase modulator) is analogous to the output of the quantizer, the delta-sigma techniques can be applied directly to achieve the spurious rejection needed in the fractional-N synthesis. Since the channel select has already been given in a digital form, k, the ADC and DAC are not required. The integrator can also be implemented digitally as an accumulator. The 1-bit quantizer output is actually the carry-out (or overflow) of the accumulator. Based on Figure 2.15, the system transfer function in z-domain is given as,

$$g(z) = \frac{\frac{1}{(1-z^{-1})}}{1+\frac{z^{-1}}{1-z^{-1}}}k(z) + \frac{e_q(z)}{1+\frac{z^{-1}}{1-z^{-1}}} = k(z) + (1-z^{-1})e_q(z) \qquad (2.23)$$

which represents a first-order digital highpass for the quantization error sequence. Any high frequency content present in the error sequence are then reduced by the loop filter of the PLL.

Third-Order Modulator

In order to improve the spurious suppression, we choose a third-order delta-sigma modulator architecture to implement our phase modulator. It is constructed from a cascade of three first-order modulator (1-1-1) as discussed in the previous section. This architecture was first proposed in [29] and is shown in Figure 2.16. In fact, the earliest form of the multi-stage modulator is based on adding coefficients from different rows of the Pascal triangle (Coefficients of polynomials drawn inside a triangle) to the basic N/N+1 pattern[30][31]. The average division ratio inside the pattern does not change because the coefficients of the Pascal triangle in a singe row are

always zero-mean and symmetric. Yet, the spurious noise components are noise-shaped as if a delta-sigma modulator.

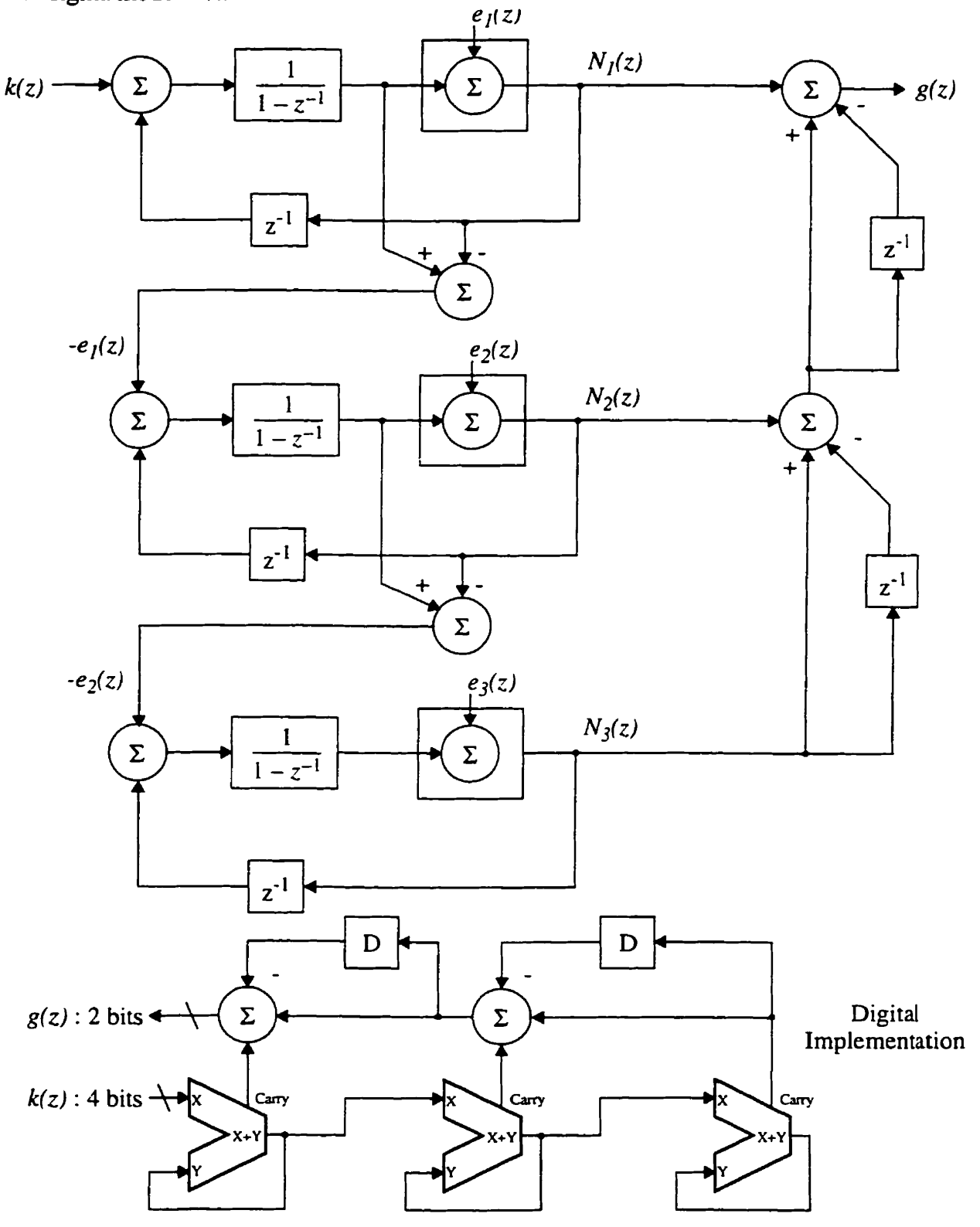


Figure 2.16 System diagram for a (1-1-1) modulator which feeds forward the error

Similar to the first-order modulator, the quantization noise of $e_n(z)$, n=1,2,3, is assumed to have a uniform distribution with $\sigma_{e_n}^2 = 1/12$. The system transfer function of the third-order modulator can be derived as follows:

For each first-order modulator ,

$$N_1(z) = \frac{\frac{1}{1-z^{-1}}}{1+\frac{z^{-1}}{1-z^{-1}}}k(z) + \frac{e_1(z)}{1+\frac{z^{-1}}{1-z^{-1}}}$$

$$= k(z) + (1-z^{-1})e_1(z)$$

$$N_2(z) = -e_1(z) + (1-z^{-1})e_2(z)$$

$$N_3(z) = -e_2(z) + (1-z^{-1})e_3(z)$$

The fractional division ratio of a 1-1-1 third-order modulator is,

$$\begin{aligned} g(z) &= N_1(z) + (1-z^{-1})N_2(z) + (1-z^{-1})^2 N_3(z) \\ &= k(z) + (1-z^{-1})^3 e_3(z) \end{aligned} \tag{2.24}$$

As the division ratio is applied to the PLL, the oscillation frequency of the VCO is,

$$f_{vco} = (N.g)f_{ref} = (N.k) \times f_{ref} + (1-z^{-1})^3 e_3(z) \times f_{ref} \tag{2.25}$$

where N is the integer division ratio of the prescaler.

The first term of (2.25) is the desired frequency, while the second term represents the frequency noise due to the modulator. We can examine the phase noise performance by calculating the Power Spectral Density (PSD) due to the second term of (2.25). First of all, we define the frequency noise as $f(z)$ and its PSD is given by,

$$\begin{aligned} S_f(z) &= |(1-z^{-1})^3|^2 \times \sigma_{e_3}^2 \times f_{ref} \\ &= |1-z^{-1}|^6 \ \frac{f_{ref}}{12} \end{aligned} \tag{2.26}$$

Applying the frequency to phase relationship, $\Phi(t) = 2\pi\int f(t)dt$, and a simple rectangular integration in the z-domain yields,

$$\Phi(z) = 2\pi\frac{f(z)}{1-z^{-1}}\frac{1}{f_{ref}} \tag{2.27}$$

The PSD of the phase noise is,

$$\begin{aligned} S_{\Phi}(z) &= \left(\frac{2\pi}{f_{ref}}\right)^2\left|\frac{(1-z^{-1})^3}{1-z^{-1}}\right|^2\frac{f_{ref}}{12} \\ &= \frac{(2\pi)^2}{12\,f_{ref}}|1-z^{-1}|^4 \end{aligned} \tag{2.28}$$

Furthermore, we can generalize the above equation for an n-th order modulator,

$$S_{\Phi}(z) = \frac{(2\pi)^2}{12\,f_{ref}}|1-z^{-1}|^{2(n-1)} \tag{2.29}$$

The PSD in the frequency domain is,

$$\begin{aligned} S_{\Phi}(f) &= \frac{(2\pi)^2}{12\,f_{ref}}\left|1-e^{-j2\pi\frac{f}{f_{ref}}}\right|^{2(n-1)} \\ &= \frac{(2\pi)^2}{12\,f_{ref}}\left(2\sin\left(\frac{\pi f}{f_{ref}}\right)\right)^{2(n-1)} \end{aligned} \tag{2.30}$$

Usually the subreference frequency[1], f, is small compared with f_{ref}. The above equation can be further simplified as below. Its plot has been shown previously at the beginning of this chapter in Figure 2.2.

$$S_{\Phi}(f) = \frac{(2\pi)^2}{12\,f_{ref}}\times\left[2\pi\frac{f}{f_{ref}}\right]^{2(n-1)} \tag{2.31}$$

The equation (2.31) shows that the rising slope of the phase noise from a second-order modulator

1. Subreference frequency is the frequency around the carrier reference.

is 20dB/decade, and that from a third-order modulator is 40dB/decade. Therefore, the noise is attenuated to negligible levels close to the carrier. However, further from the carrier, the noise is not attenuated and must be filtered prior to the VCO by the loop filter.

Interfacing with the phase selector

As the phase modulator can only provide the information of the fractional frequency control, $g(z)$, we still need to design a phase register to shift the phase properly, as shown below.

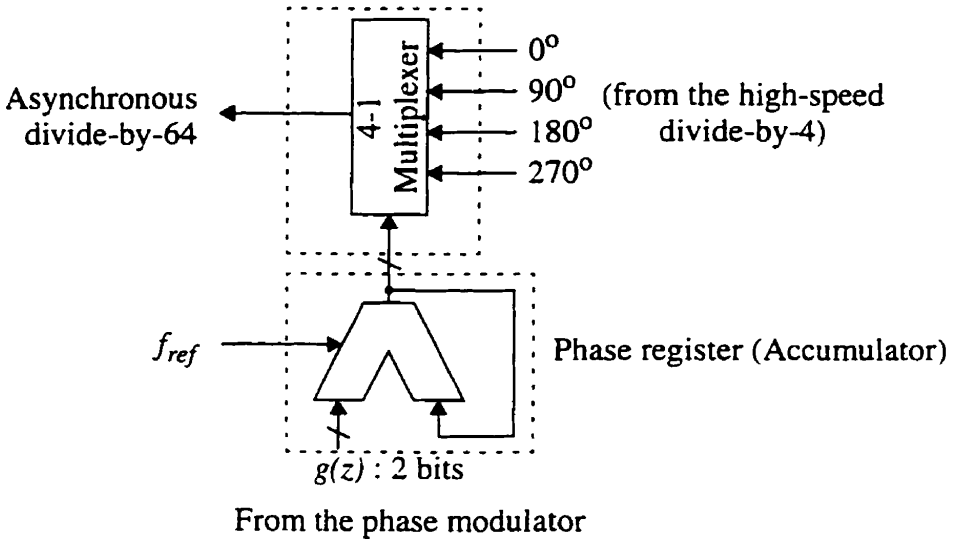


Figure 2.17 Interfacing the phase selector with the phase register

The phase degree is cyclic. The required phase shift is always given by adding the previous degree to the current one and then taking the modulus of 360°. Furthermore, the phase shift can only occur during the rising edge of f_{ref}. All of the above operations are implemented by a simple accumulator. The corresponding phase shifts in binary form are shown in the following table.

Phase Shifts	Division Ratios	Binary Controls, $g(z)$
0	N	00
90	N+1	01
180	N+2	10
270	N-1	11

2.5 Phase/Frequency Detector and Charge Pump

Phase Detectors (PD) are also referred as Phase Comparators. It is not a device that "senses phase", but rather it compares the phases of two signals and ideally provides a signal that is linearly related to the phase difference. There are many types of PDs to choose from in the design of a frequency synthesizer. A summary of two typical choices is given below.

Four-Quadrant Multipliers

This type of PD provides a signal that is proportional to the phase difference between two signals by multiplying the two input signals together. This type of PD is sometimes referred as a linear phase detector. The PD properties of a multiplier can be seen through the following trigonometric identity.

$$V_i \sin(\Phi_i) V_o \cos(\Phi_o) = 0.5 V_i V_o [\sin(\Phi_i - \Phi_o) + \sin(\Phi_i + \Phi_0)] \quad (2.32)$$

For small differences in phase, the first sine function on the right-hand side can be approximated as $\Phi_i - \Phi_o$ which is proportional to the phase difference with the gain defined to be $0.5 V_i V_o$. The second sin(.) function results in a signal at twice the frequency of the input signal and is typically removed by a simple lowpass filter. The output of this PD is a sine-wave with multiple zero phase values, half with a positive slope and the other half with a negative slope. This is shown in Figure 2.18. This property allows the user to neglect the relative polarity of the input signals in a multiplier PD because positive feedback will always force the loop away from the unstable operating point and towards stability.

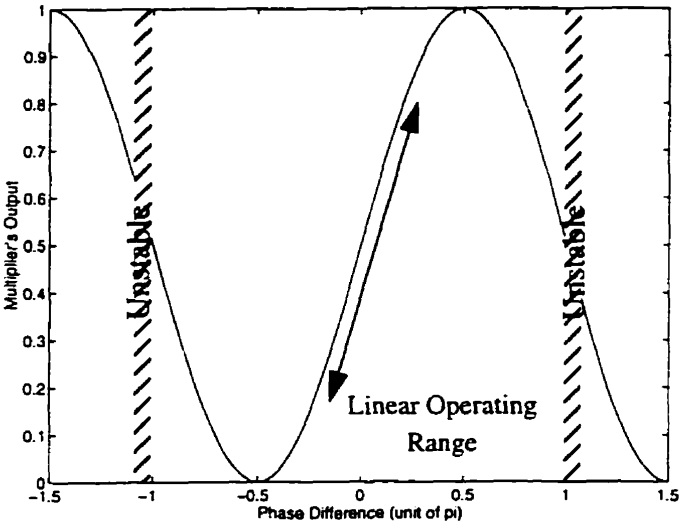


Figure 2.18 Multiplier phase detector transfer function

Except for special applications like low-noise tracking filters, the linear phase comparator is not the best choice for a PD because the gain of PD changes with the amplitude of the input signal. Equation (2.32) shows that the output signal amplitude is directly proportional to the input signal levels due to the multiplying function. If the amplitude of either signal varies due to changes in temperature or power-supply voltage, the PD gain will vary as well. These changes will alter the loop characteristics and may cause the loop to become unstable.

It might seem that this PD has an advantage by providing a continuous phase-error signal through a complete cycle, however, if the VCO signal passes through any type of digital circuit such as a prescaler, the signal will be "squared up" and there will only be the phase information at zero crossings. Furthermore, if the divider does not provide a 50% duty cycle, then the phase information will be valid only at the rising edge.

Sequential Phase/Frequency Detector and Charge Pump

A three-state phase/frequency detector (PFD) is a very robust circuit. Not only does it provide a linear input range covering 4π radians, it also provides frequency information to the loop. A typ-

ical arrangement is shown in the figure below.

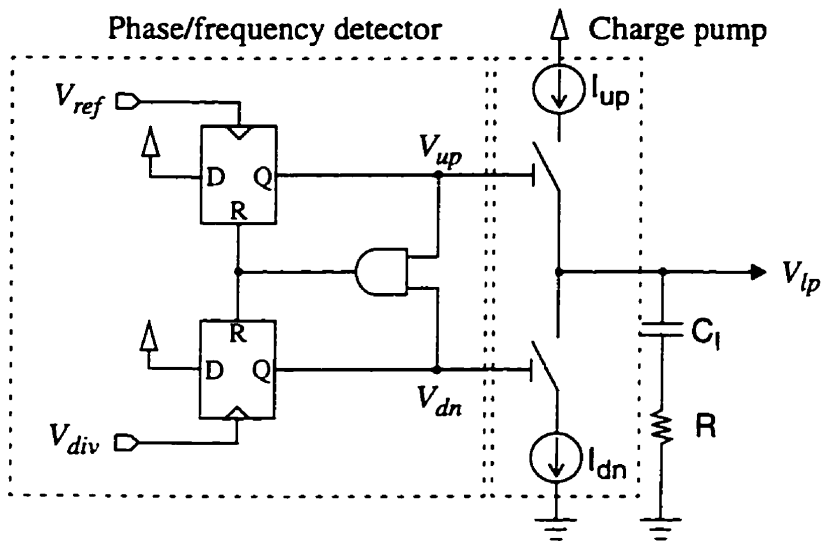


Figure 2.19 Three-state phase/frequency detector and charge pump circuit

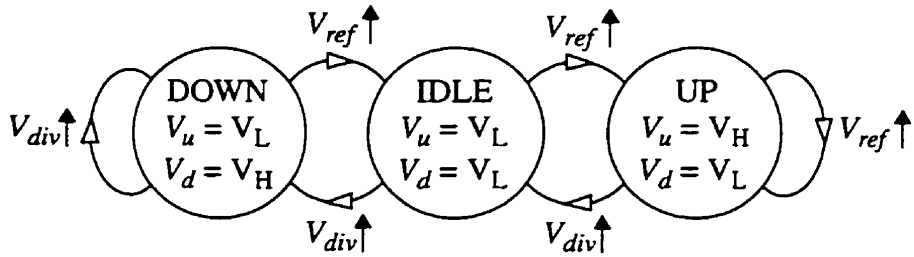


Figure 2.20 State diagram for the phase/frequency detector

As the name implies, the phase-detection operation of the above PFD can be described with a three-state machine as shown in Figure 2.20. The rising edges of the input signals cause the circuit to move from one state to the next. For example, if the state machine is initially in the idle-state, the outputs of the PFD shall be both low. The frequency of the VCO is not changed. If the VCO decreases in frequency, the rising edge from the reference, V_{ref}, will arrive, more often, before the rising edge from the prescaler, V_{div}. In case the rising edge from the V_{ref} is first seen, the state machine moves to the up-state. This turns on the charge pump I_{dn} to pump the current out from the capacitor, C_l. The control voltage, V_{vco}, is then decreased, which, in turns, slows down the VCO. This completes the phase correction for a positive error. For a negative error,

the phase correction occurs in a similar procedure but the roles of V_{ref} and V_{div} are reversed.

The gain curve of the PD is shown in Figure 2.21. It is linear from $-2\pi N$ to $+2\pi N$ and repeats itself every $4\pi N$ where N is the division ratio of the prescaler. The gain is easily calculated to be, $K_d = \frac{V_H - V_L}{2\pi N}$. At high frequencies, the range of this PD is reduced from $\pm 2\pi N$, but the gain remains constant[28].

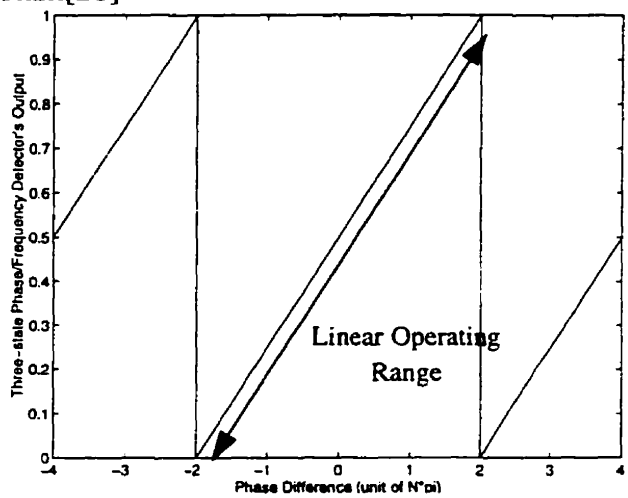
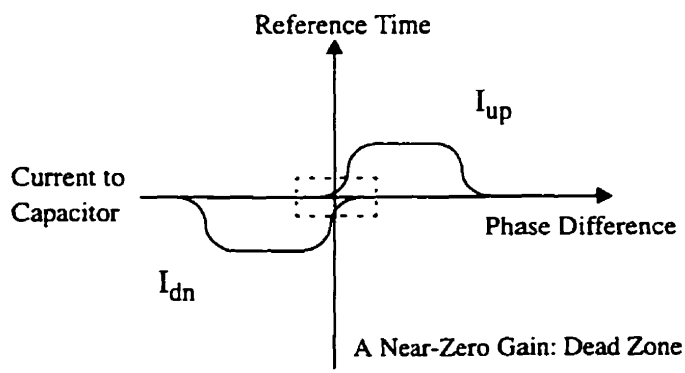


Figure 2.21 Gain curve of the three-state PFD

This circuit is not without its disadvantages. Of primary concern in this type of phase detector is the crossover distortion, and the changes in gain that can occur near zero phase difference. This is the so-called "dead zone"[33]. Since a PLL forces the oscillator to operate in this zero-phase region, the loop gain can also be reduced (possibly to zero or even crossing over and changing the negative feedback to positive feedback). The result is that the VCO output can wander around this dead zone without sending any error signal to the loop and therefore increases phase noise.



A secondary concern is the limit of the maximum operating speed which is dominated by the reset operation of the DFFs. Even the simplest type of the conventional PFD[12][32] has to contain nine gates as shown in Figure 2.22. For example, if V_{div} has already been high and a positive-going edge of V_{ref} arrives, the output of the NOR5 will go low, which forces the output of the four-input NOR1, *RST*, to become high. This *RST* signal propagates through NOR2, NOR4, NOR1 and returns to the output of NOR1 again. The critical path includes these four gate delays for resetting. The maximum operation frequency is limited by approximately twice the self-termination time of the *RST* pulse[32] which is about eight gate delays.

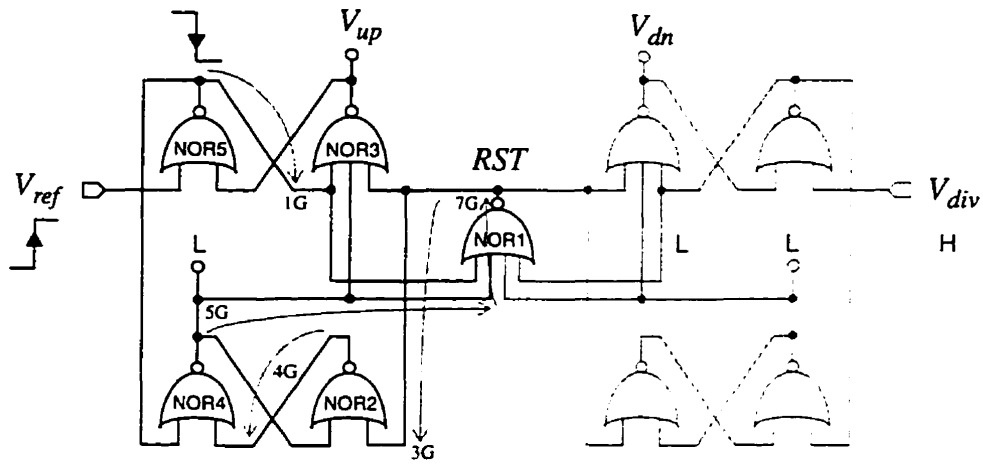


Figure 2.22 The three-state sequential phase detector based on NOR gates

Precharge-Type Phase/Frequency Detector[34]

Instead of storing the state of the phase information into a static register, this type of PFD stores the state at a precharged node. The advantage of this circuit is its high resolution for detecting the phase difference. For a high-speed fractional-N frequency synthesizer, precision in detecting a phase difference is important. Recall that the divided frequency is sent from the prescaler and the division ratio can vary from *N-1* to *N+2*. The PFD is required to distinguish a change of division ratio from *N* to *N+1*, which occurs in only one f_{vco} cycle, or 1.25 ns in our design.

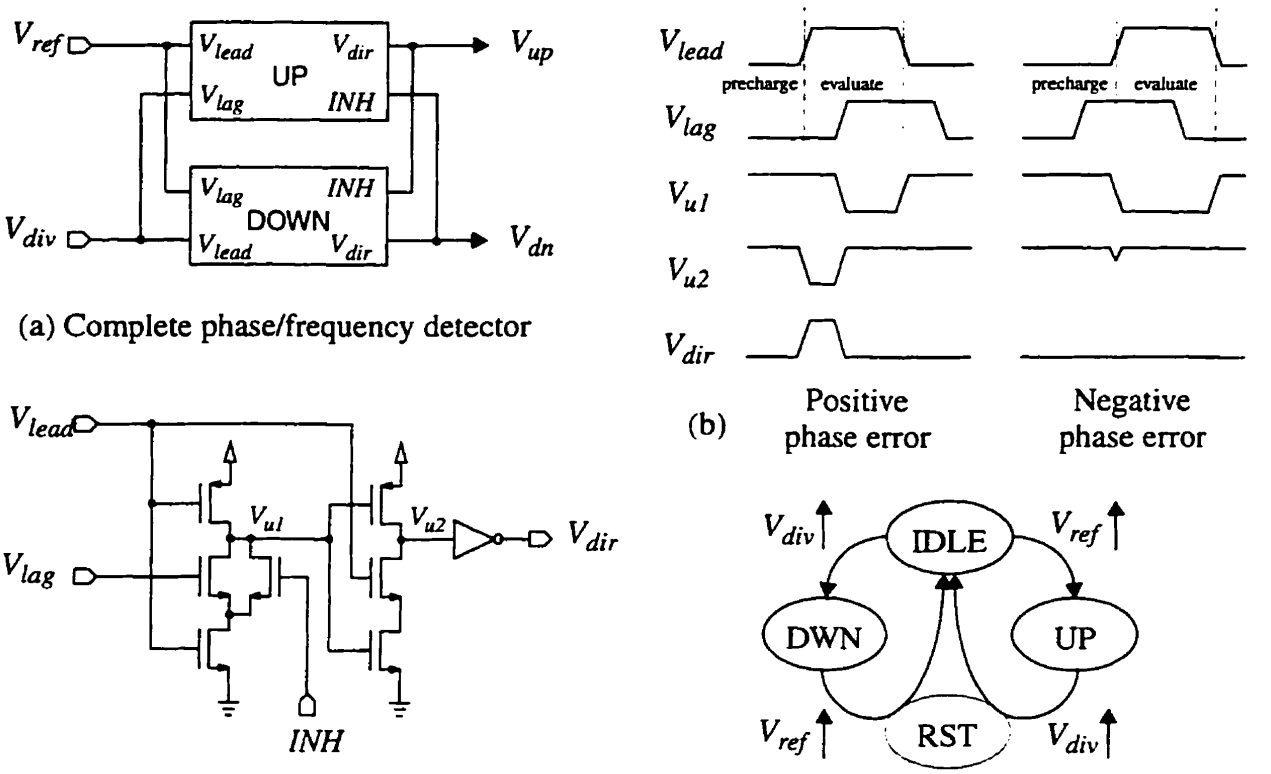


Figure 2.23 Phase detection by the precharge-type phase/frequency detector

The complete PFD consists of two half PFDs cross-coupled together as depicted in Figure 2.23(a) and (c). Each half PFD is implemented using True-Single-Phase Clocking (TSPC) logic which precharges and evaluates the phase difference between the two input clocks. It maintains a state diagram, Figure 2.23(d), similar to that of the three-state PFD. However, the number of transistors needed is only one third of those needed by the three-state PFD.

Let us first look at the UP block and the timing diagram of a positive phase error shown in Figure 2.23(a) and (b) respectively. The node V_{u1} is precharged while the V_{ref} stays low. If the V_{div} signal does not rise within the precharge period, V_{u1} remains high, which causes V_{u2} to follow V_{ref} and transit to low. Therefore an UP signal is generated in V_{up}. After the rising edge of V_{div},

V_{u1} is discharged, which deactivates the V_{up} signal. The pulse width of the V_{up} signal is thus proportional to the phase difference between V_{ref} and V_{div}. For the case of a negative phase error, V_{u1} is also precharged while V_{ref} stays low. V_{div} then rises before V_{ref}. V_{u1} is discharged immediately at the rising edge of the V_{ref}. This transient drives the V_{u2} back to high. So, no UP signal can be generated in this case.

The inhibit input, *INH*, is used to reduce the gate skew and to detect the frequency difference. Assume that there is no *INH* pin. There will be small pulses in V_{up} and V_{dn} even if the two clock inputs are in-phase. The *INH* immediately discharges the node V_{u1} of the same block (e.g. UP Block) after the precharge period when the V_{dir} of another block (e.g. DOWN Block) becomes active (i.e. high). This helps V_{dir} settle faster. The frequency detection is accomplished by the same principle. The timing diagram for frequency acquisition is shown below, for the case when V_{ref} is at a much higher frequency than V_{div}.

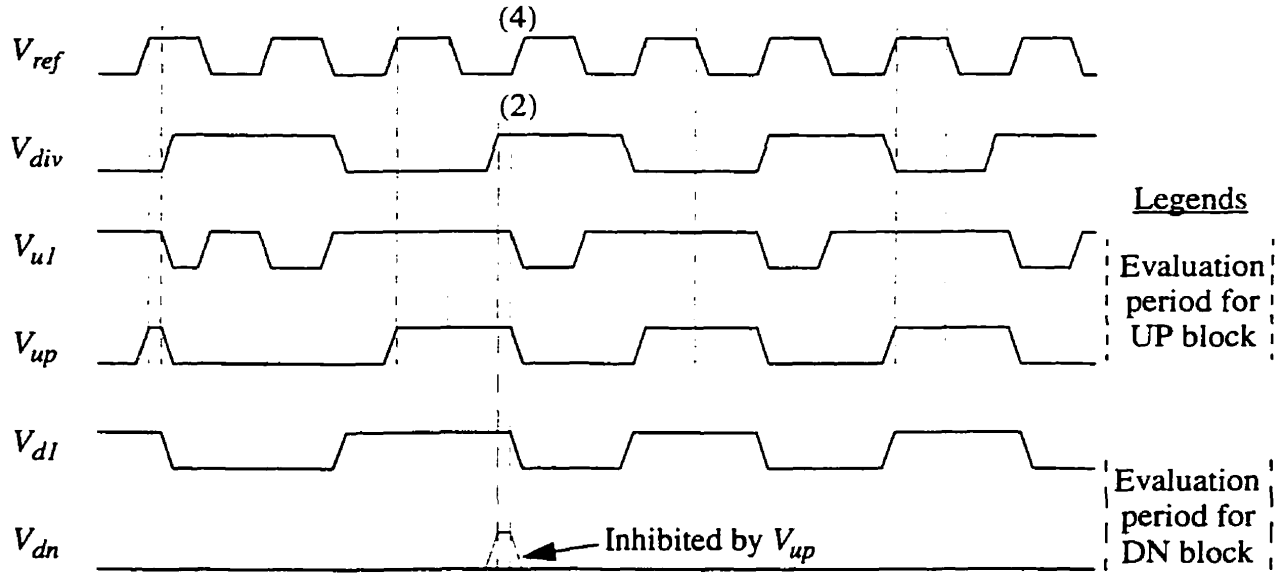


Figure 2.24 Waveforms of the precharge-type PFD during the frequency acquisition

Referring to the above diagram, we see that although the second V_{div} pulse arrives earlier than the fourth V_{ref} pulse, the false DOWN signal is inhibited by the preceding V_{up} signal because of the

cross-coupled connection shown in Figure 2.23(c).

2.6 Loop Filter

This is probably the simplest building block in the frequency synthesizer. However, it provides the designer many choices to control the dynamics of the PLL and different performance characteristics, for example, the spurious level, the lock-in time and the overshoot, can be obtained. Generally speaking, the narrower the loop bandwidth, the lower the spurious level but the longer the lock-in time.

A second-order loop filter is required for locking a linear input. The calculations of the appropriate pole location and the values of the circuit elements can be found in [12]. Some of important equations are shown again for clarity.

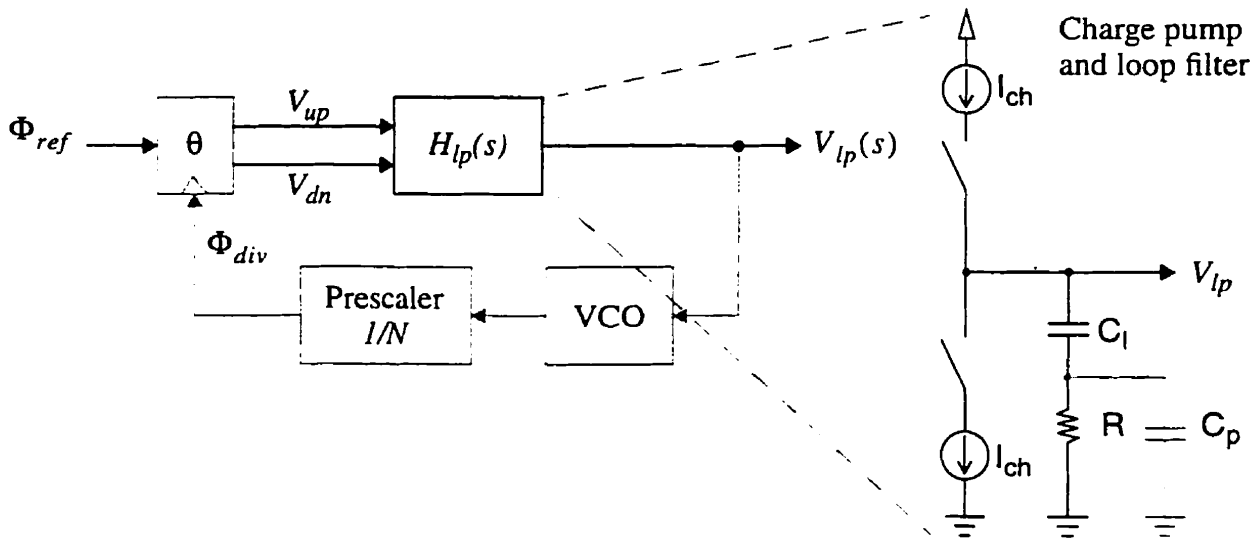


Figure 2.25 The output of the loop filter as the transfer function

The transfer function of the loop is

$$\frac{V_{lp}(s)}{\Phi_{ref}(s)} = \frac{sK_{pd}H_{lp}(s)}{s + K_{pd}K_{vco}H_{lp}(s)/N} \tag{2.33}$$

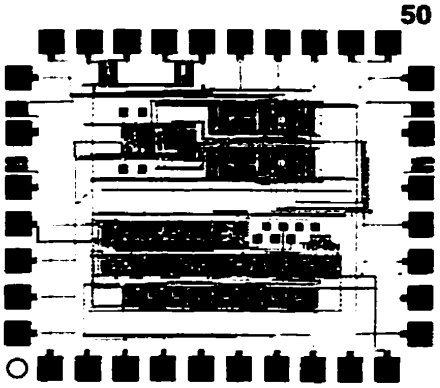
$$= \frac{N}{K_{vco}} \frac{s(1+sRC_l)}{1 + sRC_l + \dfrac{s^2NC_l}{K_{pd}K_{vco}}}$$

By setting the quadratic term and the linear term in the denominator of (2.33) equal to $1/\omega_o^2$ and $1/\omega_o Q$, respectively, the bandwidth of the PLL is $\omega_o = \frac{1}{\tau_{pll}} = \sqrt{\frac{K_{pd}K_{vco}}{NC_I}}$ and the Q-factor is $Q = \frac{1}{RC_I\omega_o} = \frac{1}{R}\sqrt{\frac{2\pi N}{C_I I_{ch} K_{vco}}}$. Nonetheless, the capacitor C_P is neglected in the transfer function, whose size is about 1/10 of C_I. It is not included for changing the dynamic of the PLL but serves as a de-glitching capacitor when either one of the current sources in the charge pump, I_{up} and I_{dn}, first switches on. The Q-factor will inevitably be enhanced by this additional C_P. We can take this into account by setting a lower value for Q, typically down 20%, and then calculate the size of C_I from ω_o as well as the value of R from Q. The size of C_p is chosen at 1/10 of the size of C_I.

2.7 References

[12] Ken Martin and David Johns, *Analog Integrated Circuit Design*, Wiley, 1996
[13] William F. Egan, *Frequency Synthesis by Phase Lock*, Wiley, 1981
[14] Roland E. Best, *Phase locked Loop Theory, Design and Applications*, Prentice Hall, 1994, 2nd Edition
[15] Jack Smith, *Modern Communication Circuits*, McGraw Hill, 1986
[16] T.A.D Riley, M.A. Copeland and T.A Kwasniewski, "Delta-Sigma Modulation in Fractional-N Frequency Synthesis", *IEEE Journal of Sold State Circuits*, Vol. 28, No. 5, May 1993, pp. 553-559
[17] Brian Miller, "Technique Enhances the Performance of PLL Synthesizers", *Microwaves and RF*, Jan. 1993, pp 59-65.
[18] Vadim Manassewitsch, "Frequency Synthesizers Theory and Design", *Wiley Interscience*, 1987, 2nd Edition
[19] E.H. Walker, "Penetration of Radio Signals into Building in the Cellular Radio Environment," *Bell System Technical Journal*, Vol. 62, No. 9, Part I, November 1983, pp. 2719-2734
[20] Lindsey, W.C., M.K. Simon, *Telecommunication Systems Engineering*, Prentice Hall, Engleword Cliffs, NJ, 1973
[21] A. Blanchard, *Phase-Locked Loops: Application to Coherent Receiver Design*, Wiley: New York, 1965

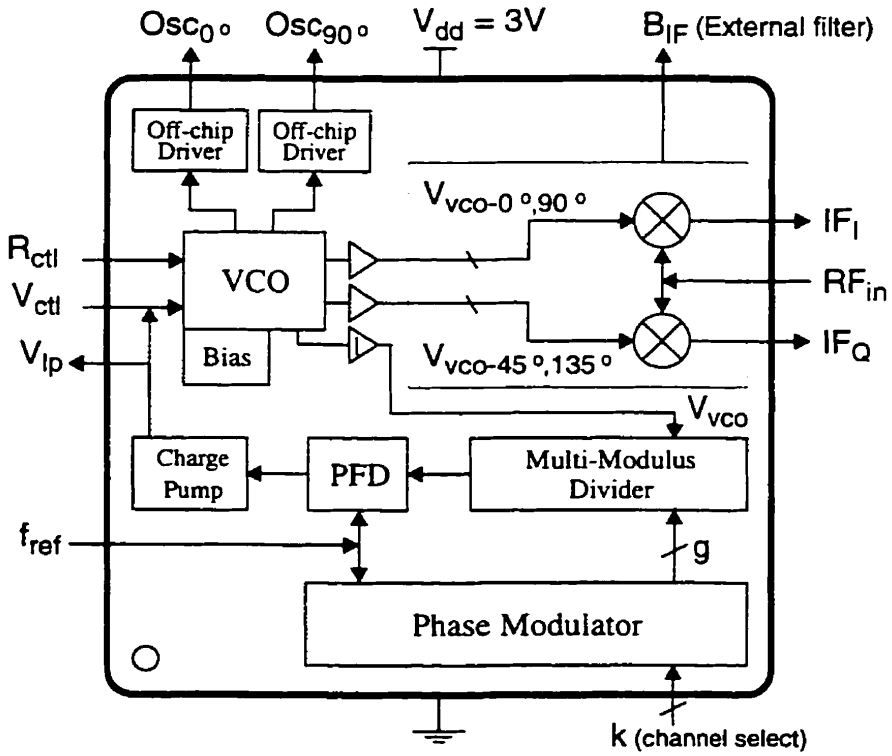
[22] Todd C. Weigandt, Beomsup Kim, Paul R. Gray, "Timing Jitter Analysis for High Frequency, Low-Power CMOS Ring-Oscillator Design", *ISCAS*, June 1994
[23] Floyd M. Gardner, "Charge-Pump Phase-Locked Loops", *IEEE Transactions on Communications*, vol. COM-28, no. 1, Nov. 1980
[24] R. Rogenmoser, Q. Huang, and F.Piazza, "1.57 GHz asynchronous and 1.4 GHz dual modulus 1.2 um CMOS prescalers," in *Proc. IEEE 1994 Custom Integrated Circuits Conf.*, May 1994, pp. 16.3.1-4
[25] Jan. Craninckx and Michiel S.J. Steyaert, "1.75 GHz/3V Dual-Modulus Divide-by-128/129 Prescaler in 0.7 um CMOS", in *IEEE Journal of Solid State Circuits*, July 1996, pp 890-897
[26] R. Rogenmoser, N.Felber, Q. Huang, and W. Fichtner, "A 1.16 GHz dual modulus 1.2 um CMOS prescaler," in *Proc. IEEE 1993 Custom Integrated Circuits Conf.*, San Diego, May 1993, pp. 27.6.1-4
[27] N. Foroudi and T. A. Kwasniewski, "CMOS high-speed dual-modulus frequency dividers for RF frequency synthesis," in *IEEE Journal Solid State Circuits*, vol. 30, pp. 93-100, Feb 1995
[28] Dan H. Wolaver, *Phase Locked Loop Circuit Design*, Prentice Hall, New Jersey, 1991
[29] Y.Matsuya, K. Uchimura, A. Iwata, T. Kobayashi, M.Ishikawa, and T. Yoshitome, "A 16-bit oversampling A-to-D conversion technology using triple-integration noise shaping," *IEEE J. Solid State Circuits*, vol. 22, pp. 921-929, Dec. 1987
[30] H. Adachi, H. Kosugi, T. Uwano, and K. Nakabe, "High-speed frequency switching synthesizer using fractional-N phase-locked loop," *Electronics and Communications in Japan*, Part 2, Vol. 77, No. 4, 1994
[31] D. Owen, and J. Wells, "Fractional-N Synthesis System," *GEC Review*, Vol. 11, No.1, 1996
[32] Soyuer M. and Myer, R. G., "Frequency Limitations of a Conventional Phase-Frequency Detector," *IEEE J. Solid State Circuits*, vol. 25, no. 4, pp. 1019-1022, Aug 1990.
[33] A.Hill and J.Surber, "The PLL Dead-Zone and How to avoid it," *RF Design*, pp.131-134, March 1992
[34] H.Kondoh, H. Notani, T. Yoshimura, H. Shibata, and Y. Matsuda, "A 1.5V 250MHz to 3.0V 622MHz Operation CMOS Phase-locked Loop with Precharge Type Phase Frequency Detecotr," *IEICE Trans. Electronics*, Vol E78C, No. 4, April 1995



Circuit Design

3

This chapter describes the circuits inside all the building blocks of the frequency synthesizer and the down-conversion mixer. First of all, the system block diagram is shown in Figure 3.1.



Pins	Descriptions
B_{IF}	IF external filter
f_{ref}	Reference frequency
$IF_{I,Q}$	I,Q-IF outputs
k	4-bit channel select
Osc_{0^o}	0°-VCO output
Osc_{90^o}	90°-VCO output
V_{lp}	Loop filter
V_{vco}	VCO input
RF_{in}	RF input
R_{vco}	VCO tuning resistor

Figure 3.1 A system block diagram of the frequency synthesizer and the mixer

This system is a mixed-signal design. The analog part of it consists of a wide-swing constant-transconductance bias circuit, a voltage-controlled oscillator (VCO), and a fully-differential mixer. The digital part consists of a multi-modulus divider, a phase modulator, a phase detector, and a charge pump. In order to balance the integration and the testability, some of the low-frequency components are connected externally and different sections can be evaluated independently.

The two off-chip drivers at the top-left corners in Figure 3.1 are 0°- and 90°-outputs of the VCO, $Osc_{0°,90°}$, which are primarily designed for testing purposes. Another pair of 0°- and 90°-outputs of the VCO, $V_{vco\text{-}0°,90°}$, are multiplied together to provide a doubled frequency to the in-phase arm of the mixer. A third pair of the VCO outputs, $V_{vco\text{-}45°,135°}$, are also multiplied similarly for the quadrature-phase arm of the mixer. The demodulated signal from the incoming RF can be obtained from the IF_I and IF_Q pins. All afore-mentioned signals are fully differential.

An output of the VCO, V_{vco}, passes through a high-speed latch which is the buffer marked with an "I"-sign inside. Positive feedback in the latch regenerates the sinusoidal shape of V_{vco} into a full-scale digital signal before the signal is fed into the multi-modulus divider. The output of the multi-modulus divider is then delivered to the digital phase/frequency detector (PFD). The PFD drives the charge pump and delivers the error signal to the VCO.

A note about naming conventions for the transistors:

A transistor is always in the form of M_{number}. All properties of the transistor are then named with the corresponding "number". For example, the threshold voltage of the transistor M_1 is called V_{th1} and the gate-to-source voltage of this is called V_{gs1}. The effective gate voltage, V_{eff1}, is equal to $V_{gs1} - V_{th1}$. This naming scheme will be applied implicitly throughout the following sections.

3.1 Wide-Swing Constant-Transconductance Bias Circuit

The bias circuit, which is shown in Figure 3.2, has incorporated a wide-swing cascode current mirrors [35] into a constant-transconductance cell [36]. The cascode current-mirrors provide a high output-impedance without severely limiting the signal swing. The use of the constant-transconductance cell maintains the transconductance of the analog circuit to match with the conductance of the bias resistor, $R_b = R_1 + R_2$, and is ideally insensitive to the power-supply, process and temperature variations.

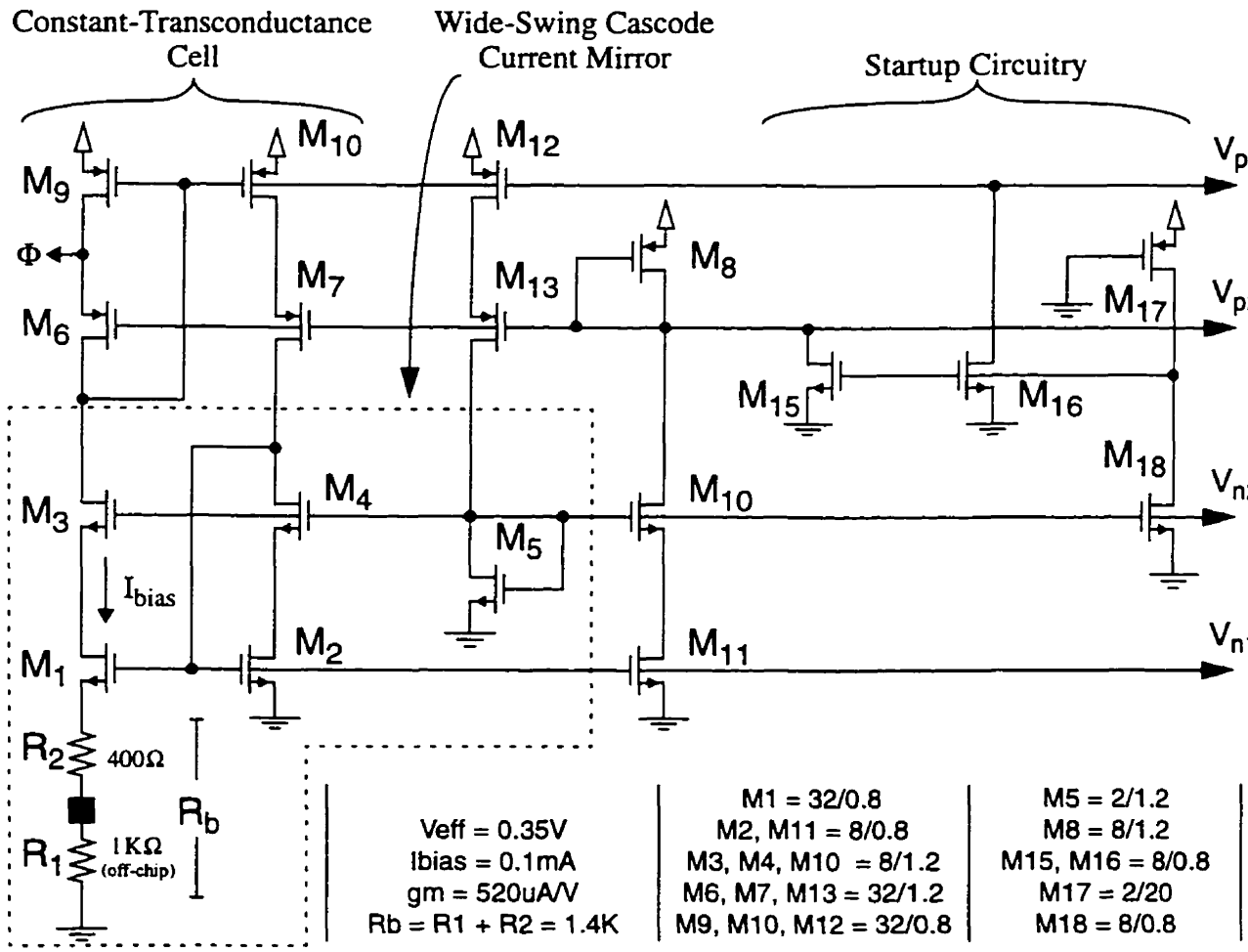


Figure 3.2 Wide-swing constant-transconductance bias circuit

Basically, there are three important building blocks in the bias circuit.

1. The constant-transconductance cell contains two cascode current mirrors which are connected rail-to-rail, and uses positive feedback to stabilize the current generated by the bias resistor.
2. The circuitry enclosed by the dotted lines is the n-MOS side of the wide-swing cascode current mirror. The p-MOS side, M_6-M_{10} is similar to that of the n-MOS but is flipped upside down and scaled according to the mobility ratio. Wide-swing cascode current mirrors are important to a low-voltage design when a high gain and a wide swing are essential. The allowable signal-swing is from $V_{ss} + 2 * V_{eff}$ to $V_{dd} - 2 * V_{eff}$ [37]. For example, if $V_{dd} = 3V$, $V_{ss} = 0V$,and $V_{eff} = 0.35V$, we shall have a maximum signal swing of $3 - 4 \times 0.35 = 1.6V$.
3. There are two stable states in the bias circuitry. One is the normal bias condition while the other one is that no current exists in all branches. The startup circuitry injects current into the constant-transconductance cell by pulling the bias lines, V_{p1} and V_{p2}, down to V_{ss} when the circuit starts functioning. After the bias currents have been established, the inverter, M_{17} and M_{18}, switches off M_{15} and M_{16} and completes the startup process. The on-resistance of M_{17} is chosen to be high (i.e. smaller W/L) so as to reduce the idle DC current.

The size of the bias resistor, R_b, can be found by applying the Kirchoff's-voltage-law (KVL) around the loop created by M_1, M_2 and R_b.

$$V_{gs2} = V_{gs1} + I_{bias}R_b$$

To a first-order approximation, assuming that the threshold voltages, V_{th1} and V_{th2}, are equal, we can calculate R_b as,

$$\sqrt{\frac{2I_{bias}}{\mu_n C_{ox}(W/L)_2}} = \sqrt{\frac{2I_{bias}}{\mu_n C_{ox}(W/L)_1}} + I_{bias}R_b$$

$$R_b = \frac{2}{\sqrt{2\mu_n C_{ox}(W/L)_2 I_{bias}}}\left(1 - \sqrt{\frac{(W/L)_2}{(W/L)_1}}\right)$$

$$R_b = \frac{2}{g_{m2}}\left(1 - \sqrt{\frac{(W/L)_2}{(W/L)_1}}\right)$$

$$= \frac{1}{g_{m2}} \qquad \text{if } \frac{(W/L)_2}{(W/L)_1} = \frac{1}{4} \qquad (3.1)$$

If the body effect of M_1 is included, i.e. $V_{gs1} = V_{eff1} + V_{th} + \Delta V_{th}$, we shall need a smaller bias resistor because,

$$R_b = \frac{1}{g_{m2}} - \frac{\Delta V_{th}}{I_{bias}}$$

$$= \frac{1}{g_{m2}} - \frac{\gamma}{I_{bias}}(\sqrt{2\Phi_f + V_{sb1}} - \sqrt{2\Phi_f})$$

$$= \frac{1}{g_{m2}}\left(1 - \frac{2\gamma}{V_{eff}} \cdot \sqrt{2\Phi_f}\left(\sqrt{1 + \frac{V_{sb1}}{2\Phi}} - 1\right)\right) \qquad g_{m2} = \frac{2I_{bias}}{V_{eff}}$$

$$\cong \frac{1}{g_{m2}}\left(1 - \frac{\gamma}{2\sqrt{2\Phi_f}}\right) \qquad V_{sb1} = I_{bias}R_b = I_{bias}/g_{m2} \qquad (3.2)$$

We revise the size of the R_b by substituting[1] $\gamma = 0.6V^{1/2}$ and $2\Phi_f = 0.7V$ into (3.2). The second term, $\gamma/(2\sqrt{2\Phi_f})$, in the bracket is found to be 0.36 and thus the new value of R_b is 1.3K. The Hspice simulation shows that R_b should be 1.4K.

Apart from the body effect, the mobility degradation will also come into effect when the temperature rises. This affects the gate-effective voltage and hence the signal swing. Detailed discussions can be found in [37].

The circuit was designed using a V_{eff} of 0.35V. The chosen V_{eff} is a bit higher than typical in order to give an improved noise rejection for the voltage-controlled oscillator[38].

1. All nominal parameters are extracted from the level-3 model of the HP 0.5um process.

Bias Current versus Power-Supply Voltage

To demonstrate the stability, the bias circuitry from the extracted layout was simulated using Hspice. In Figure 3.3, the bias current is plotted against the power-supply voltage.

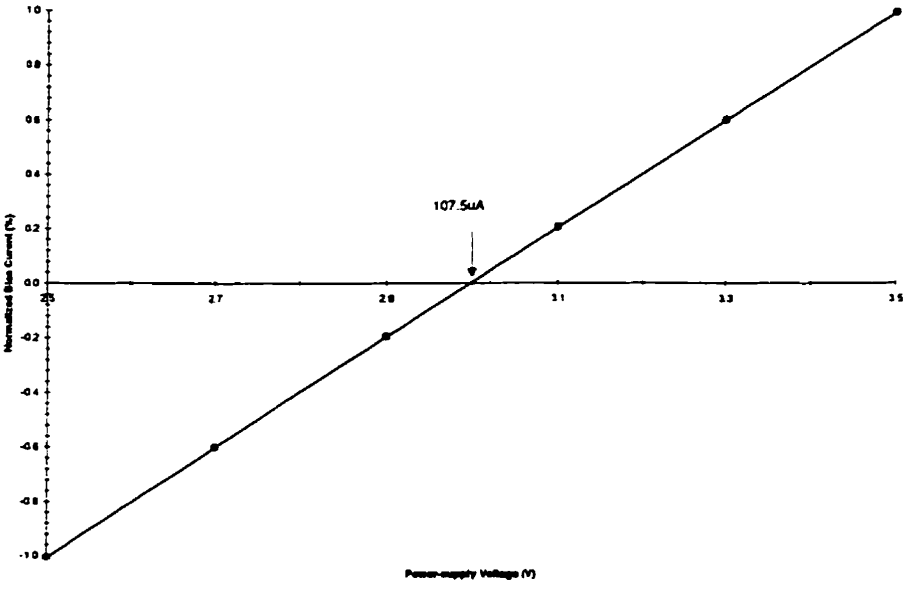


Figure 3.3 Bias current from the wide-swing constant-transconductance bias versus the power-supply voltage

3.2 Four-Stage Ring Voltage-Controlled Oscillator

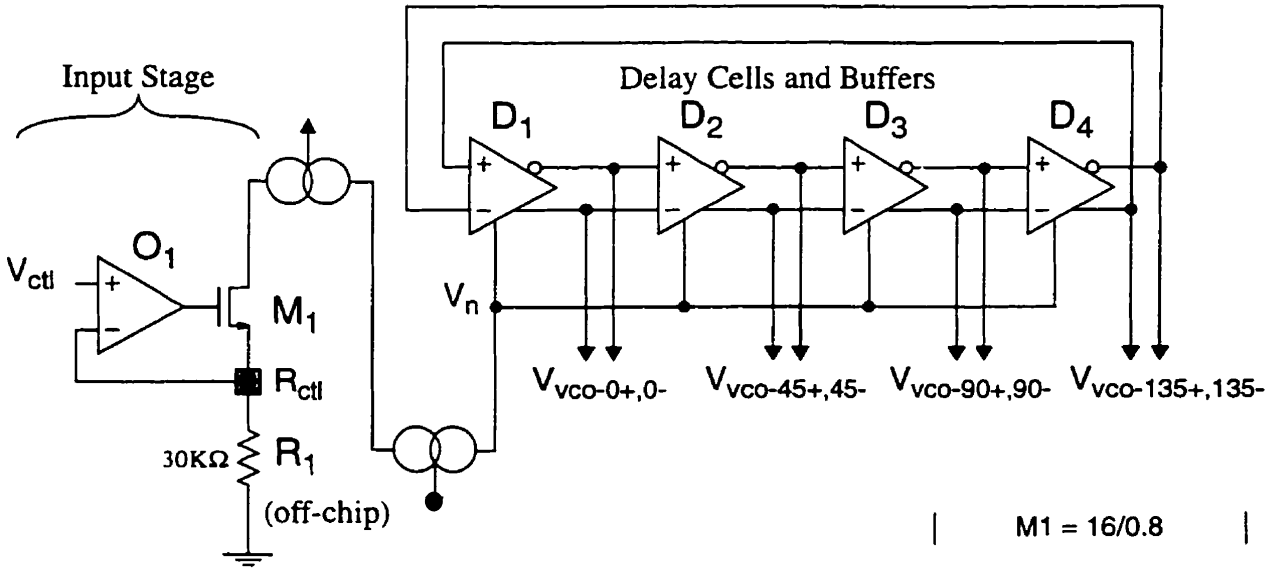


Figure 3.4 Voltage-controlled oscillator

A block diagram of the voltage-controlled oscillator (VCO) is shown in Figure 3.4. The high-gain opamp, O_1, in the VCO converts the input voltage, V_{ctl} (from the charge pump), into current which is given by $I_{R1} = V_{ctl} / R_1$. The current is then mirrored by a wide-swing current mirror. Four delay cells are connected as a ring oscillator. Each delay cell provides a delay of 45° for a total delay of 180°. The additional 180° phase shift comes from a cross connection between D_4 and D_1. The use of an even number of delay cells is advantageous because quadraturely-shifted versions of any output signal are available. As we shall see in the mixer design, one of the applications is to multiply two of the quadrature signals and obtain a doubled frequency[39] because $\sin(2\omega) = 2\sin(\omega)\cos(\omega)$. The effect of the power-supply noise on the oscillation frequency can be minimized by means of a fully-differential design and, thereby, reduces the phase jitter.

Single-Ended Folded-Cascode Opamp (O_1)

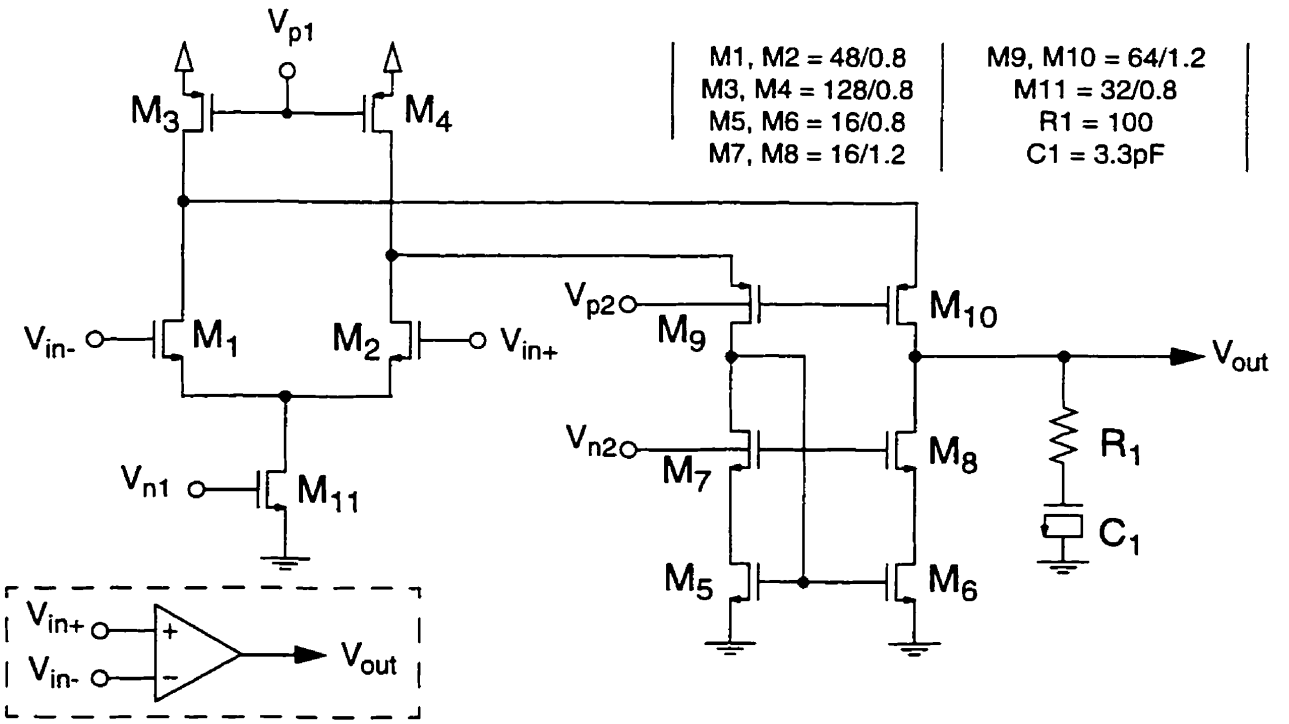


Figure 3.5 Single-ended folded-cascode opamp

The input stage of the VCO contains an NMOS transistor driven by a single-ended folded-cascode opamp, O_1, which is shown in the Figure 3.5. The folded-cascode structure is well-known for its high speed and high gain. In addition, by using the wide-swing current bias, the output signal swing is not limited seriously. Some of the design equations related to the opamp are summarized[37][40] as follows.

- Voltage Gain

$$\begin{aligned} \text{Low-frequency gain: } A_v &= g_{m1} r_{out} \\ &= g_{m1}\{[(g_{m8}+g_{mb8})r_{ds8}r_{ds6}] \parallel [g_{m10}r_{ds10}(r_{ds4} \parallel r_{ds2})]\} \\ &\cong g_{m1}g_{m10}\frac{(r_{ds4} \parallel r_{ds2})r_{o10}}{2} \\ &= 2\text{m} \times 930\text{u} \times \frac{11.4\text{K}(210\text{K})}{2} \\ &= 67\text{dB} \end{aligned} \tag{3.3}$$

$$\begin{aligned} \text{Mid- and high-frequency gain: } A_v &= g_{m1}\left(r_{out} \parallel \left(R_1 + \frac{1}{sC_1}\right)\right) \\ &\cong \frac{g_{m1}(1+sR_1C_1)}{sC_1} \end{aligned} \tag{3.4}$$

Notice that there is a zero, $1/R_1C_1$, due to the lead-compensation resistor, R_1. A reasonable value of the zero frequency is about 1.2 times[41] the unity-gain frequency, g_{m1}/C_1.

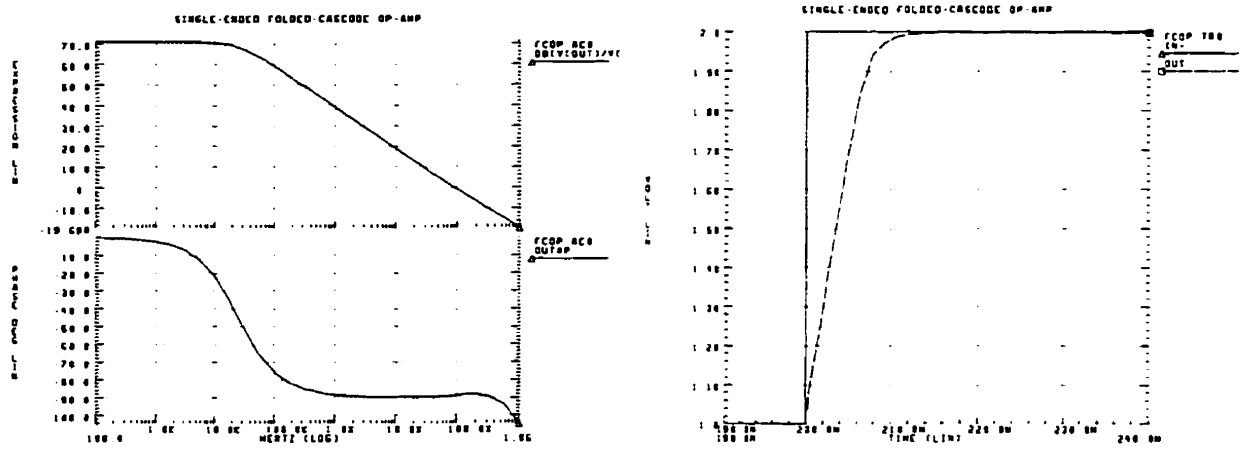
- Unity-gain frequency and Slew Rate

$$\begin{aligned} \omega_t &= \frac{g_{m1}}{C_1} & SR_v &= \frac{I_{D6}}{C_1} \\ &= \frac{2m}{3.3p} & &= \frac{412u}{3.3p} \\ &= 100\text{ MHz} & &= 125\text{ V/us} \end{aligned} \tag{3.5}$$

- Output Swing $V_{pp} = (V_{ss} + (V_{eff6} + V_{eff8}), V_{DD} - (V_{eff4} + V_{eff10}))$
  $= (0.7\text{ V}, 2.3\text{ V})$

The Hspice simulation results are shown in the figures below. From Figure 3.6(a), the

low-frequency gain is found to be 70dB. The phase margin is 90° at the unity frequency of 100MHz. In Figure 3.6(b), the slew-rate is shown to be 117V/us.



(a) (b)

Figure 3.6 Simulation results of the single-ended folded-cascode opamp (a) Frequency response (b) Step response

Delay Cells and Buffers (D_1, D_2, D_3, D_4)

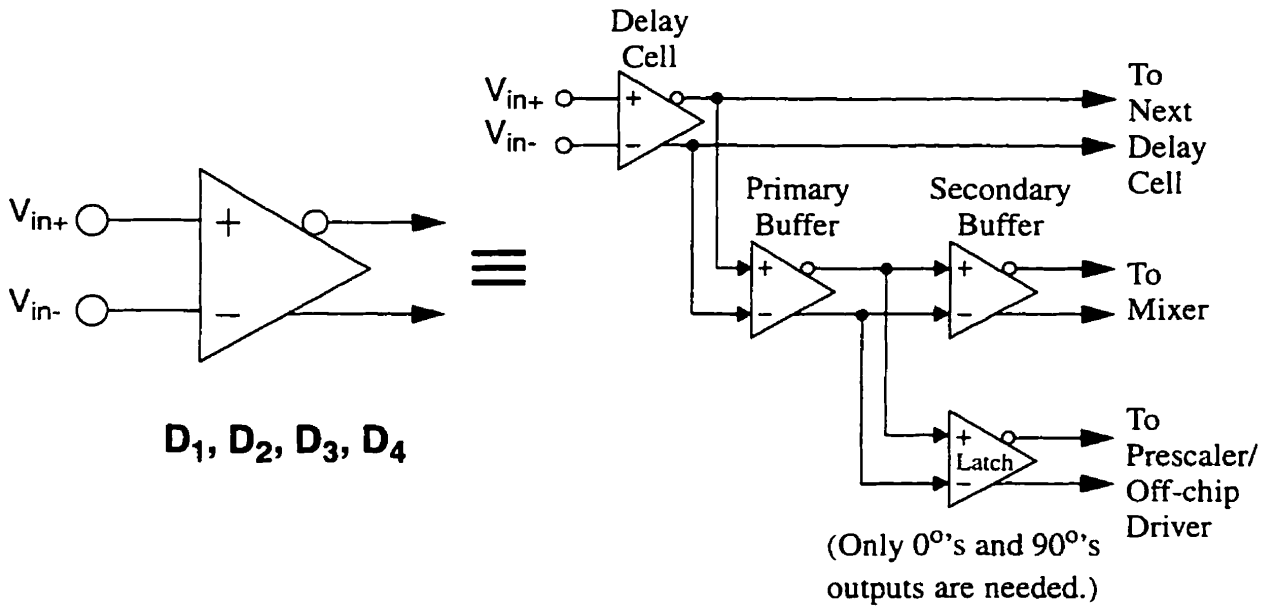


Figure 3.7 Schematic of a delay cell and it buffers

A delay unit which consists of a delay cell and three buffers is shown in Figure 3.7. Given a high oscillation frequency near the GHz range, the driving capability of a single CMOS delay cell is often very low. A series of buffers is necessary to provide enough gain for driving output signals.

Delay Cell

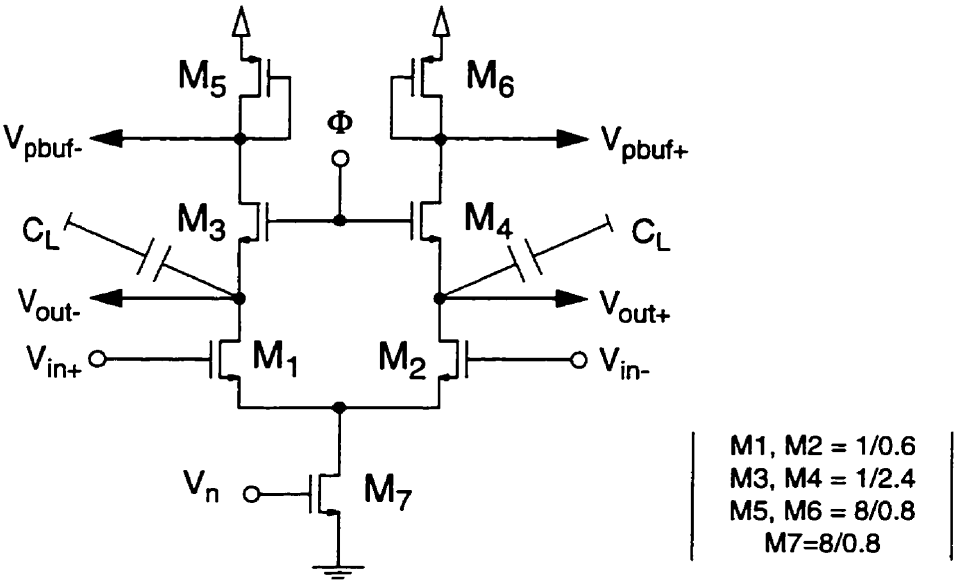


Figure 3.8 Differential delay cell

The delay cell is a differential pair with an NMOS load on top of a common-gate current driver, M3 and M4, as shown in Figure 3.8. The bias current, I_{D7}, is set by the input stage via the current mirrors and the V_n terminal. The common-gate driver provides the differential pair, M1 and M2, with low-impedance nodes to charge and to discharge their output nodes rapidly and hence to achieve a higher oscillation frequency. In addition, it acts as a current driver for the primary buffer. The bias voltage, Φ , is tapped from the drain of M9 in the bias circuit as shown in Figure 3.3 to ensure that M3 and M4 are always in their saturation mode. A pair of diode loads, M5 and M6, converts the current into voltage and drives the buffer stages.

The first step in designing a ring oscillator is to ensure that each delay cell has a gain greater than 1 at its pole frequency because the ring oscillator needs to have enough gain to start the oscillation. The DC gain, a_v, from V_{in} to V_{out} is approximately g_{m1} / g_{m3}. Since the 45° of phase shift occurs at the dominant pole with a gain of $a_v / \sqrt{2}$, the DC gain has to be greater than

$\sqrt{2}$. Thus, a proper ratio of W_1 and W_3 is given by

$$a_v = \sqrt{\frac{W_1}{L_1}\frac{L_3}{W_3}} > \sqrt{2} \quad \Rightarrow \quad \frac{W_1}{L_1}\frac{L_3}{W_3} > 2 \tag{3.6}$$

The second step is to determine the oscillation frequency. The period of oscillation cannot be easily represented in a complete expression. However, a simplified expression can be obtained by examining the phase delay of each delay cell. We model the transfer function of a single delay cell as a first-order system which is given as,

$$\frac{V_{out}(s)}{V_{in}(s)} \cong g_{m1}\left(\frac{1}{g_{m3}} \parallel \frac{1}{sC_L}\right) = \frac{g_{m1}}{g_{m3}}\left(\frac{1}{1 + s(C_L/g_{m3})}\right) \tag{3.7}$$

The position of the pole location depends on the load capacitance at the nodes, $V_{out+/-}$, and the impedance looking into the sources of common-gate amplifier. Since each delay cell contributes 45°, or $\pi/4$ radians of the phase lag, the oscillation frequency, f_o, which produces the desired phase-lag, can be estimated as,

$$\begin{aligned} -\angle\frac{V_{out}(s)}{V_{in}(s)} = \text{atan}(2\pi f_o \tau) = \pi/4 \quad \Rightarrow \quad f_o &= \frac{\tan(\pi/4)}{2\pi\tau} = \frac{1}{2\pi\tau} = \frac{g_{m3}}{2\pi C_L} \\ &= \frac{1}{2\pi}\frac{g_{m3}}{(C_{d1} + C_{s3} + C_{g1})} \\ &= \frac{1}{2\pi}\left(\frac{40u}{9.8f}\right) \\ &\cong 650\text{MHz} \quad @ \quad V_{ctl} = 0.75\text{V} \end{aligned} \tag{3.8}$$

In fact, the above estimation has not predicted the amplitude of the oscillation, nor the asymmetry of the output signal. A more accurate model may predict the delay as a combination of the time it takes for the load device to pull up the output node, including the effect of changing the transconductance, and the time required to charge and to discharge the output nodes, $V_{out+/-}$ [38]. An analysis of a simpler case has been done by [41]. The result obtained from (3.8) is valid

as long as the slew-rate limiting has not occurred. If the slew-rate limiting, $SR_v = I_{D7}/C_L$, had occurred and we assumed a full logic level was 3V, the oscillation frequency would have been $f_o = \frac{1}{\tau_o} = \frac{1}{(V_{pp}/SR_v)} = \frac{I_{D7}}{V_{pp}C_L} = \frac{40u}{3(10f)} = 1.33\text{GHz}$. Therefore, it confirms that the slew-rate limiting does not occur prior to the dominant-pole frequency.

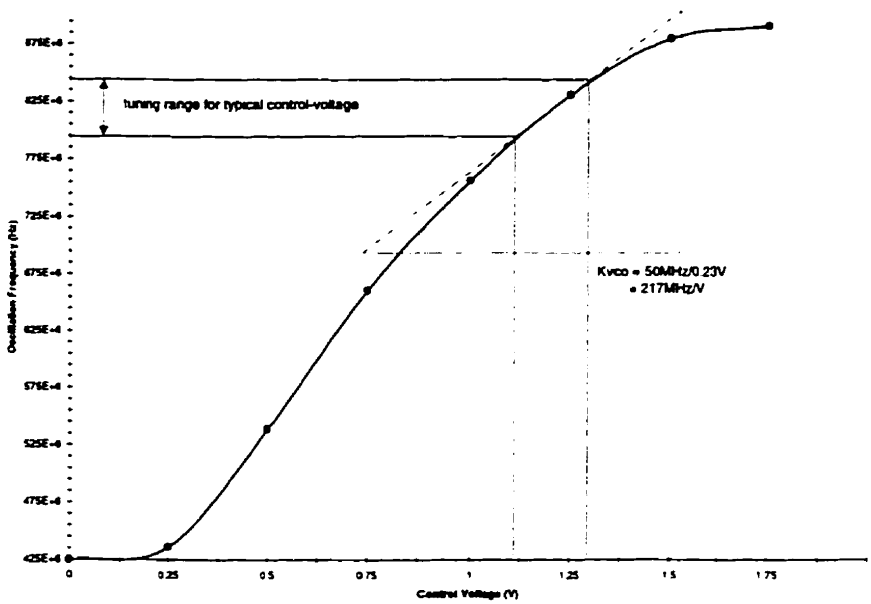


Figure 3.9 Gain curve of the VCO

The frequency of oscillation, simulated from the extracted layout, is plotted against the control voltage, as shown in Figure 3.9. The center frequency can be changed from 425MHz to 890MHz with a 465MHz tuning range. In our design, with a reference frequency to the PLL, f_{ref} = 3.2MHz, and a division ratio of the multi-modulus divider, int(N) = 256, the targeted tuning range is around 820 ±25 MHz.

Primary buffer and secondary buffer to the mixer

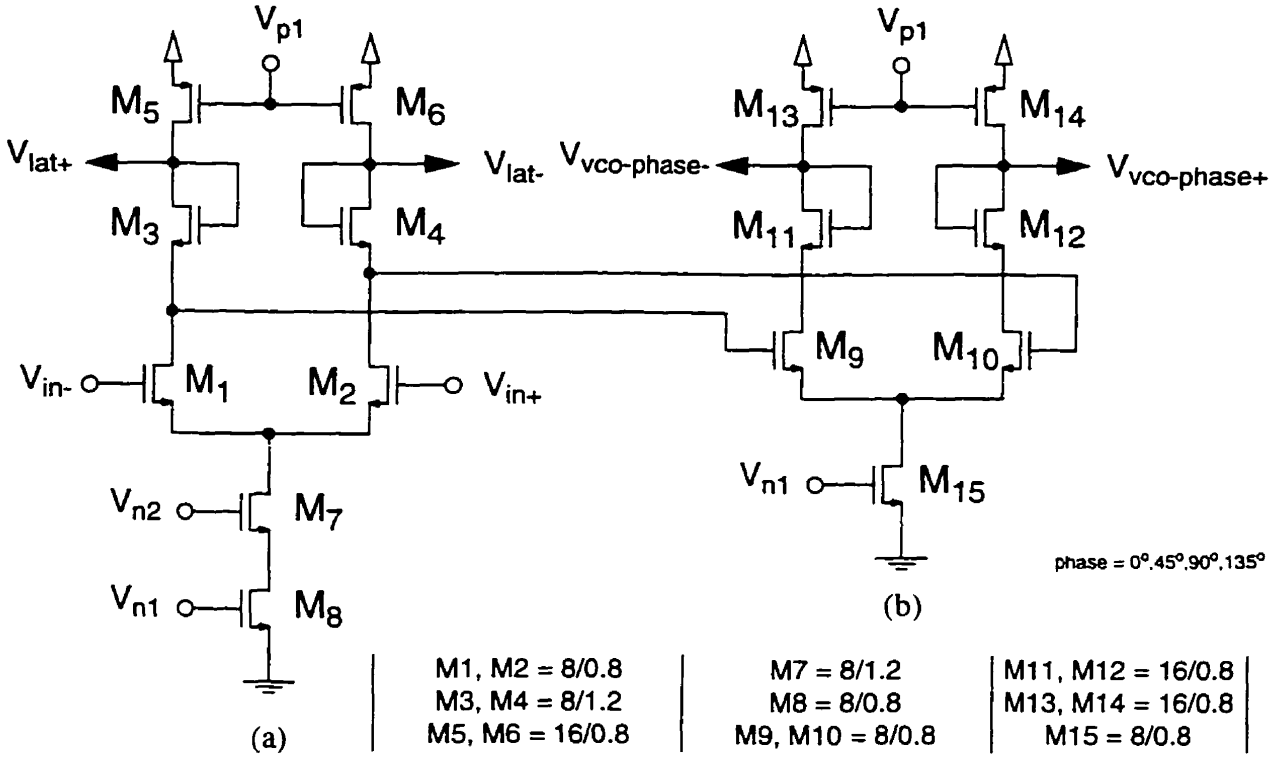


Figure 3.10 (a) Primary buffer and (b) Secondary buffer to the mixer

The primary and the secondary buffer contain similar level-shifts and gain stages, as shown in Figure 3.10(a) and (b) respectively. The primary buffer isolates the feed-through from the output stage back to the ring oscillator. Signals from the ring oscillator, $V_{in+,-}$, are amplified as they pass through differential pairs in the primary and secondary buffers, and are then level-shifted to drive the switching transistors in the mixer via $V_{vco\text{-}phase+/-}$. Another pair of level-shifted outputs from the primary buffer, $V_{lat+/-}$, is connected to a latch which is shown in Figure 3.11(a). The latch utilizes positive feedback to convert the oscillation waveform into a full logic level for the input of the prescaler. As shown in Figure 3.11(b), a 50-ohm output buffer is a high-current driver for off-chip probing. It can provide up to 6mA, peak-to-peak, to an external termination resistor which can be a discrete one, or the termination resistor inside the oscilloscope.

Secondary buffer to the prescaler and off-chip driver

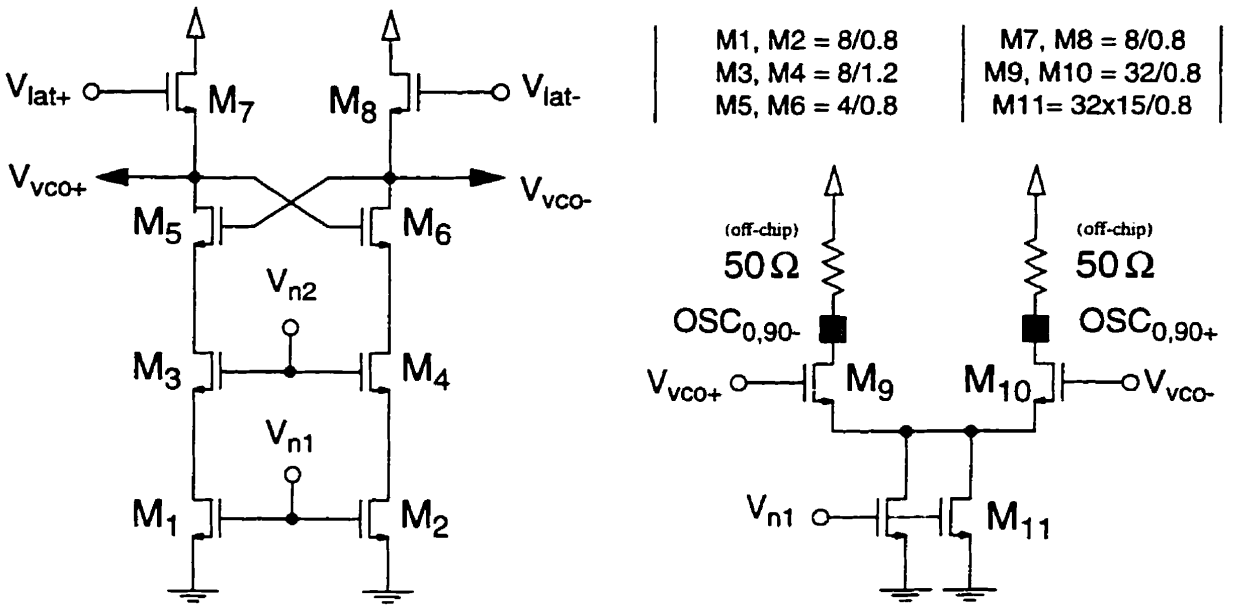


Figure 3.11 (a) Latch to the prescaler and (b) 50-ohm off-chip driver

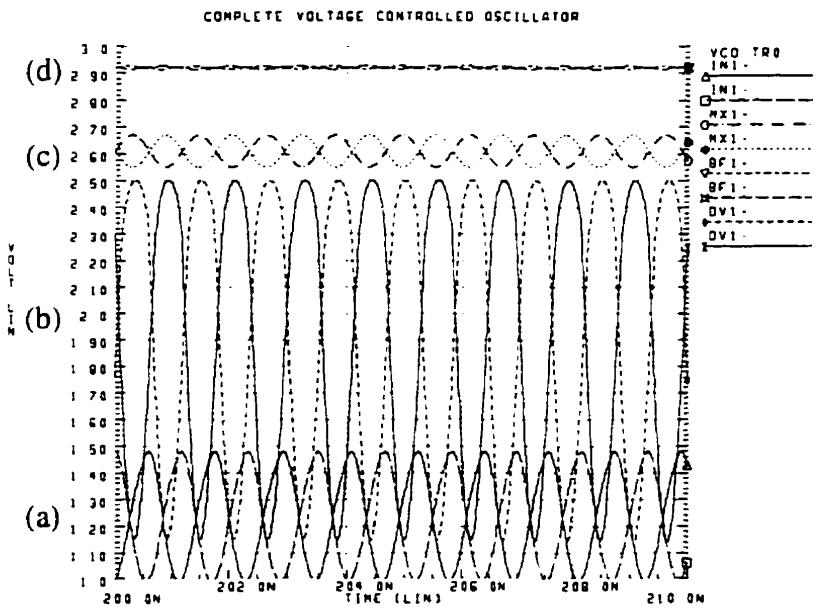


Figure 3.12 Waveforms of different outputs: (a) $V_{out+,-}$ (b) $V_{vco-0+,-}$ (c) $V_{lat+,-}$ and (d) $Osc_{0+/-}$

Figure 3.12 shows the simulated waveforms from different outputs of the VCO oscillating at 800MHz with an input voltage, V_{ctl}, of 1.5V. Each output node of the off-chip driver is assumed to have a 2pF capacitor (only for Hspice simulations) that emulates the capacitive load of the package pin.

3.3 Down-Conversion Mixer[43]

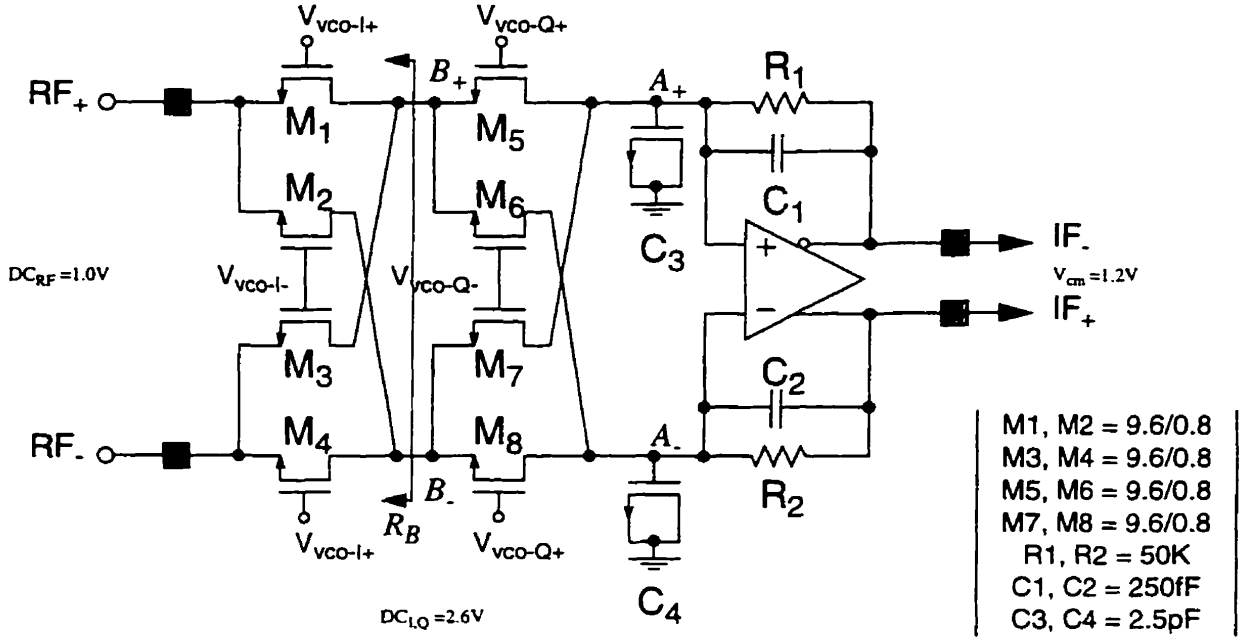


Figure 3.13 Circuit topology of a fully-differential down-conversion mixer

As shown in Figure 3.13, a mixer exhibiting a high linearity is realized by using the linear voltage-to-current relationship of a MOS transistor in its triode region. The multiplier in front of the opamp modulates the incoming $RF_{+/-}$. The use of a double-balanced structure cancels out the common-mode DC biasing signals and the nonlinearity of the switching transistors, M1-M8, due to the dependency of g_{ds} on V_{ds}. The highest-frequency node is $A_{+/-}$. Fortunately, this mixer is a down-conversion type. The opamp together with the feedback network immediately converts the current into a voltage and produces a low-frequency output signal, $IF_{+/-}$. However, to ensure that no high-frequency current on the virtual ground is leaked into the output voltage, two large capacitors, C_3 and C_4, are added. The feedback resistors, R_1 and R_2, are 50K-ohm and realize a high conversion gain.

The DC bias level of the RF and LO must be chosen to bias the switching transistors in

their triode region at all times. Otherwise, there will be distortion if the transistors are turned off during the mixing period. This can be avoided by setting their smallest-possible gate voltages at least a V_{th} higher than the largest-possible source level. For example, at M1, $V_{VCO\text{-}I,DC} - V_{VCO\text{-}I,AC} > V_{RF,DC} + V_{RF,AC} + V_{th1}$. We have chosen $V_{RF,DC}$ = 1.0V, $V_{RF,AC}$ = 160mV, $V_{VCO\text{-}I,DC}$ and $V_{VCO\text{-}Q,DC}$ = 2.6V through simulations. To understand the working principle, we start with the current equations going through each switching transistor, as given by

$$I_{DS,1} = \beta \cdot \left(V_{vco\text{-}I+} - V_{RF,DC} - V_{th} - \frac{V_{RF+} - V_{RF,DC}}{2}\right) \cdot (V_{RF+} - V_{RF,DC})$$

$$I_{DS,2} = \beta \cdot \left(V_{vco\text{-}I-} - V_{RF,DC} - V_{th} - \frac{V_{RF-} - V_{RF,DC}}{2}\right) \cdot (V_{RF-} - V_{RF,DC})$$

$$I_{DS,3} = \beta \cdot \left(V_{vco\text{-}I+} - V_{RF,DC} - V_{th} - \frac{V_{RF+} - V_{RF,DC}}{2}\right) \cdot (V_{RF-} - V_{RF,DC})$$

$$I_{DS,4} = \beta \cdot \left(V_{vco\text{-}I-} - V_{RF,DC} - V_{th} - \frac{V_{RF+} - V_{RF,DC}}{2}\right) \cdot (V_{RF+} - V_{RF,DC})$$

$$\begin{aligned} V_{B+} - V_{B-} &= R_B \cdot [(I_{DS,1} - I_{DS,4}) - (I_{DS,3} - I_{DS,2})] \\ &= \beta R_B \cdot (V_{vco\text{-}I+} - V_{vco\text{-}I-}) \cdot (V_{RF+} - V_{RF-}) \end{aligned}$$

The currents going through the Q-input transistors are similar to those of the I-input transistors. Thus, the IF-output is given by

$$\begin{aligned} V_{IF+} - V_{IF-} &= R_f \cdot [(I_{DS,5} - I_{DS,6}) - (I_{DS,8} - I_{DS,7})] \\ &= \beta R_f \cdot (V_{vco\text{-}Q+} - V_{vco\text{-}Q-}) \cdot (V_{B+} - V_{B-}) \\ &= \beta R_f \cdot (V_{vco\text{-}Q+} - V_{vco\text{-}Q-}) \cdot \beta \cdot R_{in} \cdot (V_{vco\text{-}I+} - V_{vco\text{-}I-}) \cdot (V_{RF+} - V_{RF-}) \\ &= (\beta^2 R_f R_B)(V_{vco\text{-}Q+} - V_{vco\text{-}Q-})(V_{vco\text{-}I+} - V_{vco\text{-}I-})(V_{RF+} - V_{RF-}) \\ &= (\beta^2 R_f R_B)(\sin\omega_{vco}t)(\cos\omega_{vco}t)(V_{RF+} - V_{RF-}) \\ &= \left(\frac{\beta^2 R_f R_B}{2}\right)(\sin 2\omega_{vco}t)(V_{RF+} - V_{RF-}) \end{aligned}$$

The negative-feedback structure of the opamp in the mixer is shown in a simplified form in Figure 3.14(a). An ideal opamp can suppress any signal at the virtual ground. However, for a real opamp having only a limited Gain-Bandwidth (GBW), the transfer functions from the input to the output and to the virtual ground thus become

$$\frac{V_{out}}{V_{in}} = \frac{-\frac{R_f}{R_{in}}}{1+\frac{R_f+R_{in}}{R_{in}}\cdot j\frac{\omega}{2\pi\cdot GBW}} \cong \frac{A}{1+A\cdot j\frac{\omega}{2\pi\cdot GBW}} \tag{3.9}$$

$$\frac{V_v}{V_{in}} = \frac{\frac{R_f}{R_{in}}\cdot j\frac{\omega}{2\pi\cdot GBW}}{1+\frac{R_f+R_{in}}{R_{in}}\cdot j\frac{\omega}{2\pi\cdot GBW}} \cong \frac{A\cdot j\frac{\omega}{2\pi\cdot GBW}}{1+A\cdot j\frac{\omega}{2\pi\cdot GBW}} \tag{3.10}$$

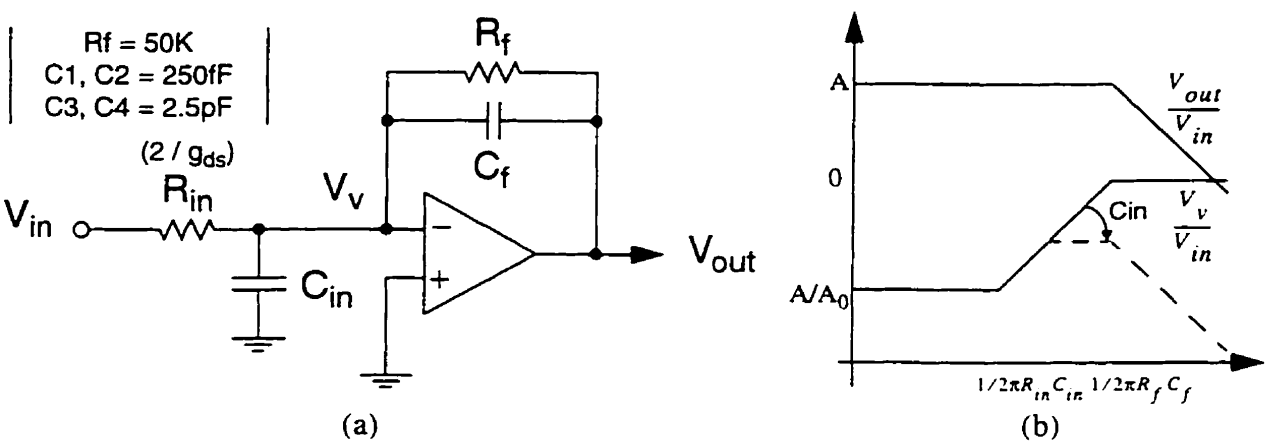


Figure 3.14 (a) The negative-feedback configuration and (b) the transfer functions of the mixer

The output bandwidth, *GBW/A*, given in (3.9) has to be larger than 8 MHz for our application[44]. In combination with the feedback capacitor, C_f, the bandwidth can be positioned more accurately. The use of an opamp with a small GBW does pose a problem. As shown in (3.10), input signals with a frequency spectrum beyond *GBW/A* are directly transferred from the virtual ground to the output without being suppressed by the feedback configuration. One solution is to add an extra capacitor, C_{in}, to the virtual ground and, therefore, introduce a pole at $1/(2\pi\cdot R_{in}C_{in})$ to sup-

press the high-frequency signal without degrading the output bandwidth. The pole must be positioned between the $1/(2\pi \cdot R_f C_f)$ and *GBW/A*, as shown in Figure 3.14(b).

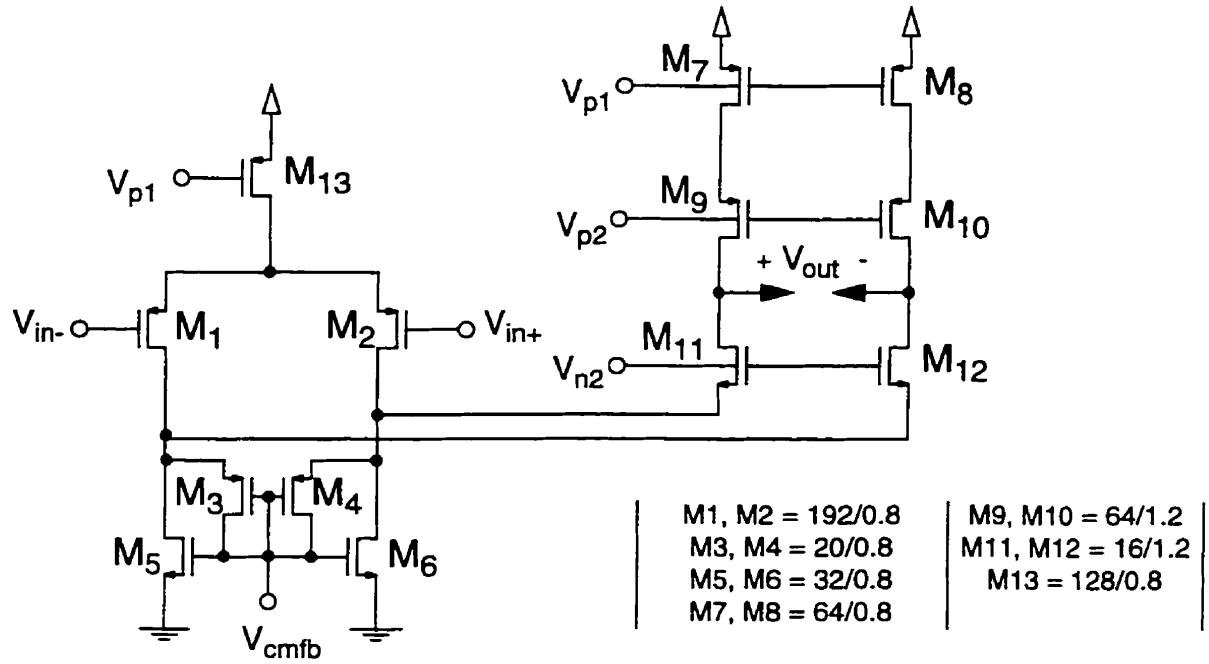


Figure 3.15 A PMOS-input fully-differential opamp

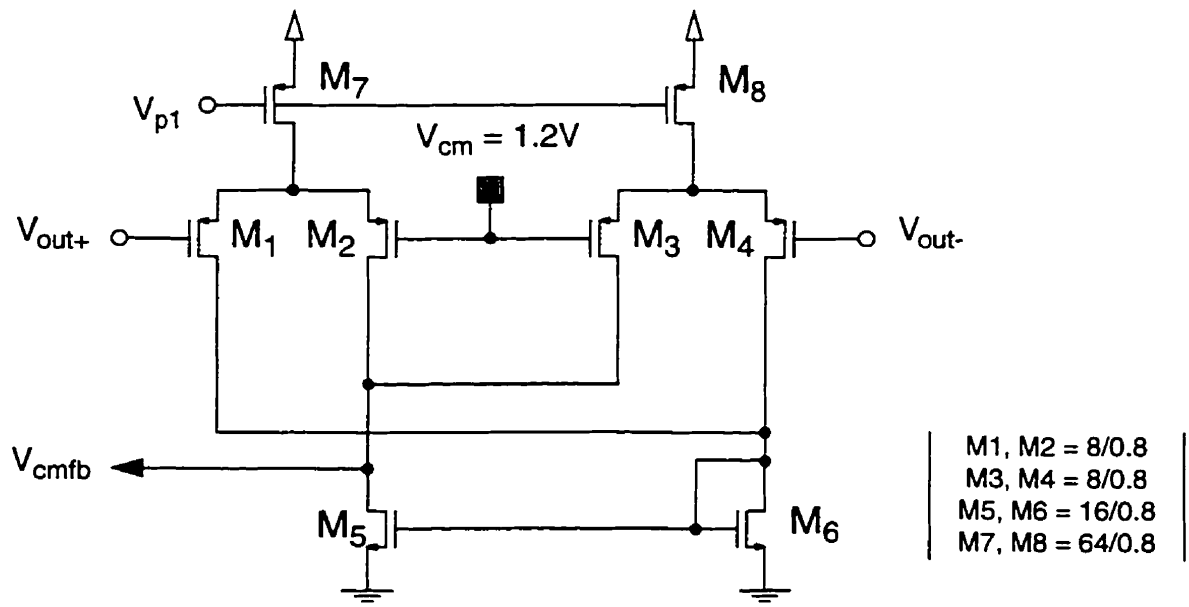


Figure 3.16 A standard common-mode feedback

The opamp circuitry used in the mixer is shown in Figure 3.15. Its specifications are the same as those used for the single-ended version (See Figure 3.5) except that it has a PMOS input

because of the noise considerations[37]. The DC of the input RF is set at 1V by an external bias, and that of the opamp's outputs is set at 1.2V by a standard common-mode feedback as shown in Figure 3.16. This ensures the switching transistors always work in their triode mode because their effective-gate voltages are always greater than their drain-to-source voltages.

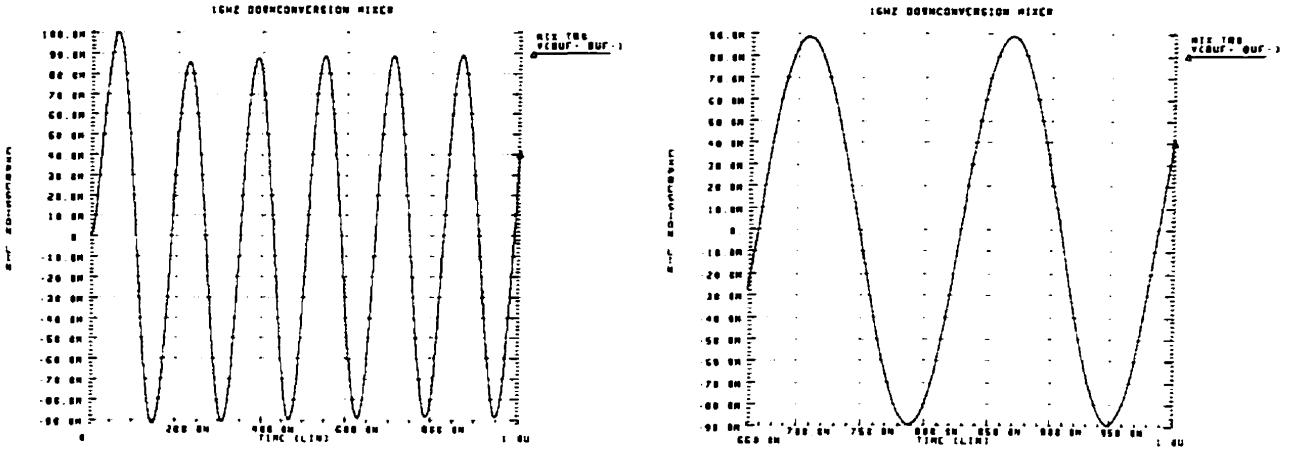


Figure 3.17 Demodulated IF-waveform of an incoming RF: (a) a switching transient (b) a zoom-in plot

In Figure 3.17(a), an incoming RF of 1.60625GHz is demodulated by a 1.6GHz signal which is doubled from the 800MHz output of the VCO. The frequency of the demodulated waveform is found to be 6.025MHz from Figure 3.17(b).

3.4 Multi-Modulus Divider

The multi-modulus divider is shown in Figure 3.18. The buffered oscillation signal from the VCO, V_{vco}, is divided by the prescaler. It provides four shifted versions of the divided-by-4 signals, $V_{4.0,90,180,270}$. The phase selector picks up one of the four signals and delays according to the outputs of the phase modulator, S_1 and S_0. The asynchronous divide-by-64 block consists of five low-speed ripple counters. All circuits of these blocks have been simulated and their results

are presented in the following sections.

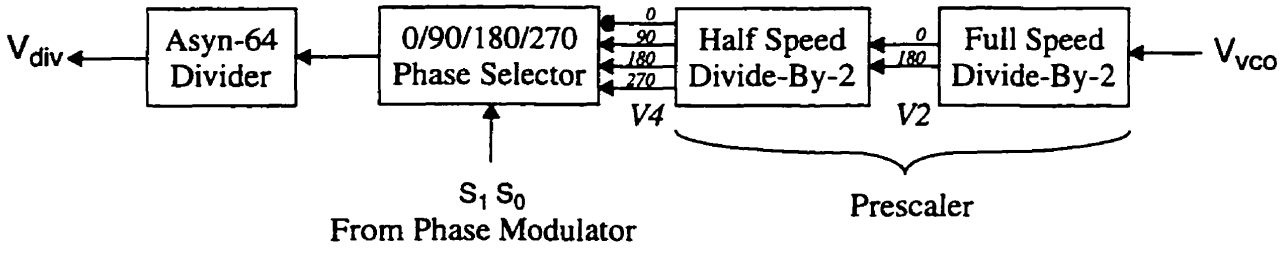


Figure 3.18 Block diagram of the multi-modulus divider

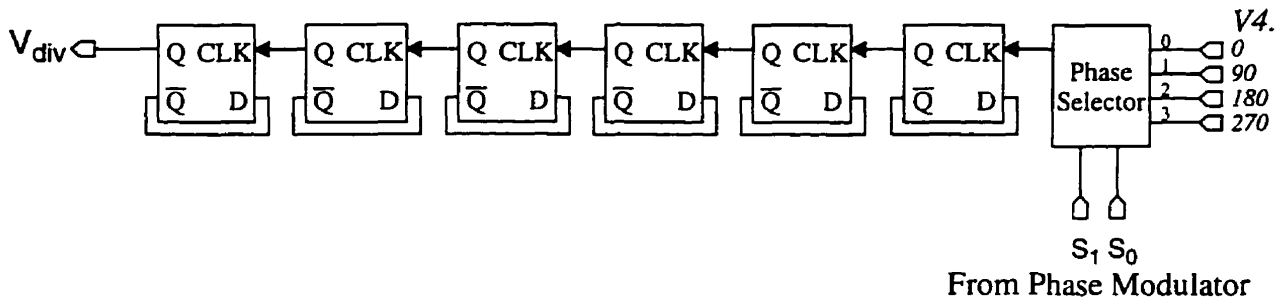


Figure 3.19 The phase selector and a chain of low-speed divide-by-2 circuits

Prescaler

The divide-by-2 circuit[45] used in the prescaler is depicted in Figure 3.20. It contains two high-speed latches and is configured in a master-slave structure. There are two sensing devices, M1 and M2, a cross-coupled regenerative loop, M3 and M4, and two active loads, M5 and M6, in the master latch (and similarly in the slave latch). For instance, if the input differential signals, $f_{in.0}$ and $f_{in.180}$, are H and L respectively, the active loads of the master latch shall be turned off and the master latch will be in the sense mode while those of the slave latch shall be turned on and the slave latch will be in the store mode. Similarly, if the logic levels of $f_{in.0}$ and $f_{in.180}$ are reversed (i.e. L and H respectively), the modes of the latches shall also be reversed. The gate capacitances of all transistors are always parallel to either the inputs or the outputs and hence no internal node exists. In addition, it is worth mentioning that the voltage swings of the divider's output, as shown in Figure 3.21, are not rail-to-rail (~25% duty cycle) when the device is operating at its

maximum speed. The simulated waveform from the extracted layout is shown in Figure 3.21.

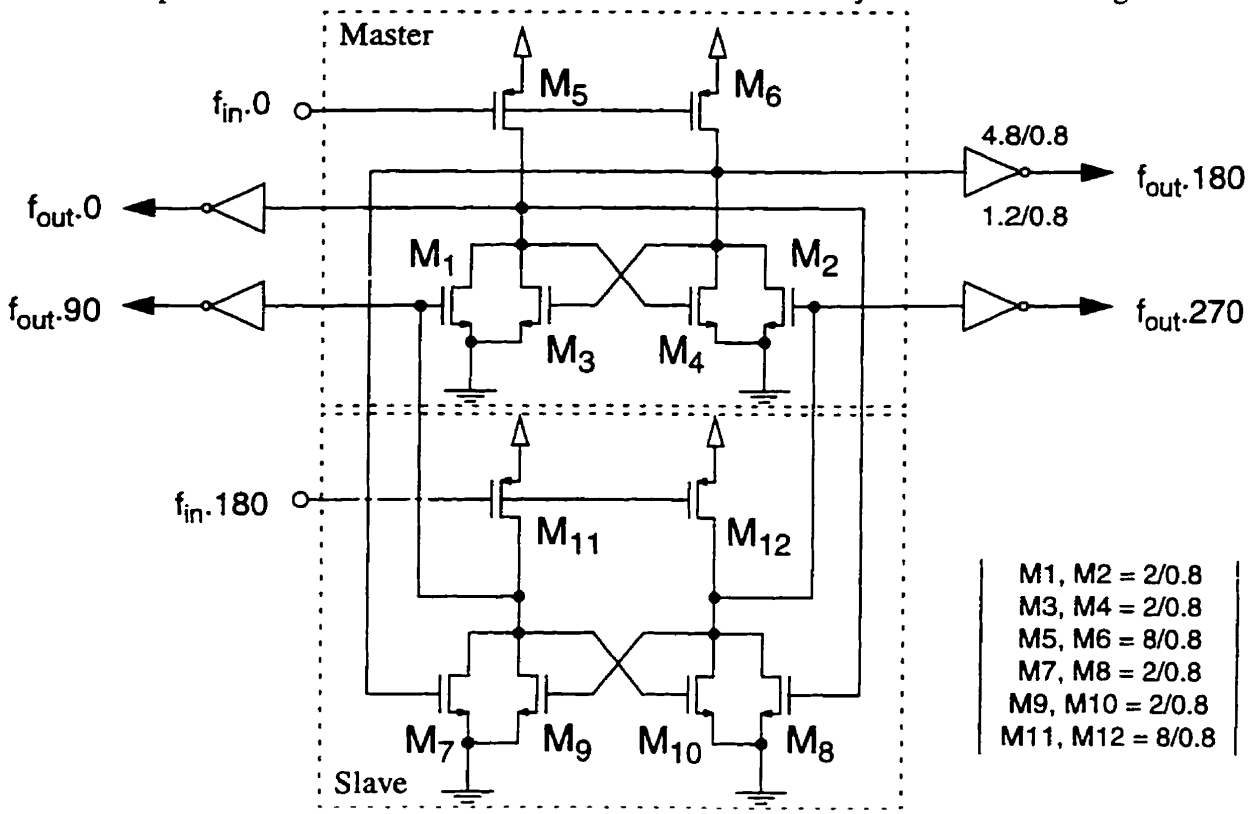


Figure 3.20 High-speed divide-by-2 circuit

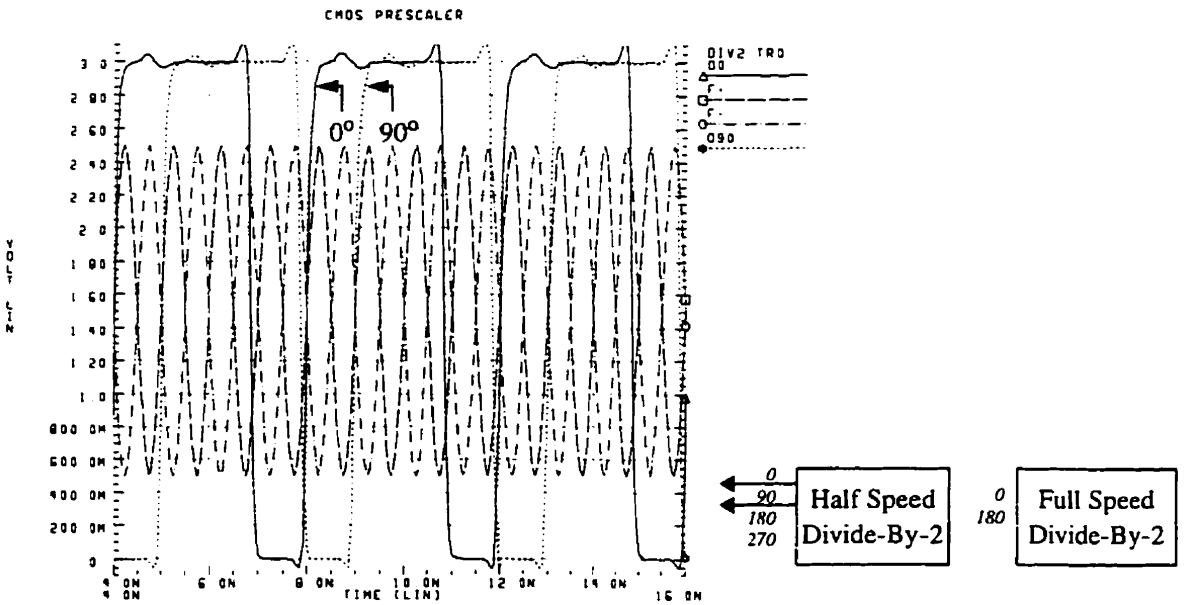


Figure 3.21 Simulated waveforms of the prescaler running at 1GHz

While designing this divider, we can take advantage of the insights obtained from the design of the VCO. In fact, if the swing of the differential inputs is very small, the divider will

even oscillate itself. It imposes a lower limit on the voltage swing of the input to start the oscillation. The maximum toggling frequency can be roughly estimated as

$$f_{tog} = \frac{G_m}{C_L}$$

where G_m is about half of the transconductance of each n-mos transistor and C_L is the capacitance at each output node. The result has been shown in [37] and is given as

$$\begin{aligned} f_{tog} &\cong K \cdot \frac{\mu_n V_{eff}}{L^2} \\ &= \frac{0.5}{(W_{inv-p} + W_{inv-n} + W_n)} \cdot \frac{\mu_n V_{eff}}{L^2} \\ &= \frac{0.5}{(4.8 + 1.2 + 2)} \cdot \frac{0.05(0.5)}{0.8^2} \\ &= 0.33\text{ns} \end{aligned} \tag{3.11}$$

In a master-slave flip-flop, the maximum clock rate can be no faster than half of the toggling rate and thus equals to 1.2GHz (reduced by a 20% design margin). As shown in (3.11), the divider can be further optimized by reducing the channel length to a minimal-possible value as long as the technology permits.

Low-Speed Asynchronous Frequency Divider

A chain of low-speed dividers is responsible for further dividing the one-fourth frequency of the VCO for the phase detector. Since the maximum frequency of the low-speed divider is not as critical as that of the prescaler, a simple D-flip flop is used, as shown in Figure 3.22. It is an asynchronously resetable flip-flop. Its inverted output is connected back to its input and, thereby, the flip-flop will work as a divide-by-2 circuit. The simulated waveform of the divider toggling at 90% of its maximum frequency is shown in Figure 3.23. The maximum frequency of the extracted circuit is found to be 270MHz and meets the requirement we stated in Section 2.3.

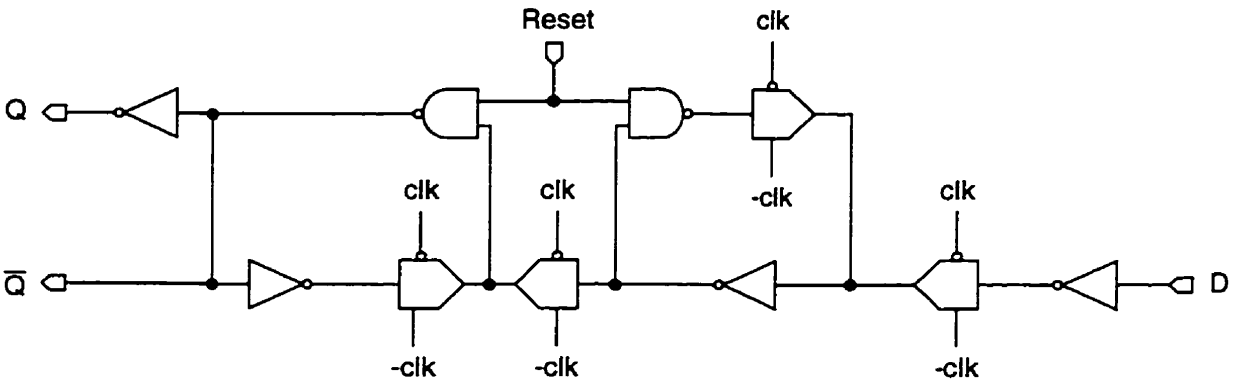


Figure 3.22 Logic diagram of an asynchronously resetable D-flip-flop

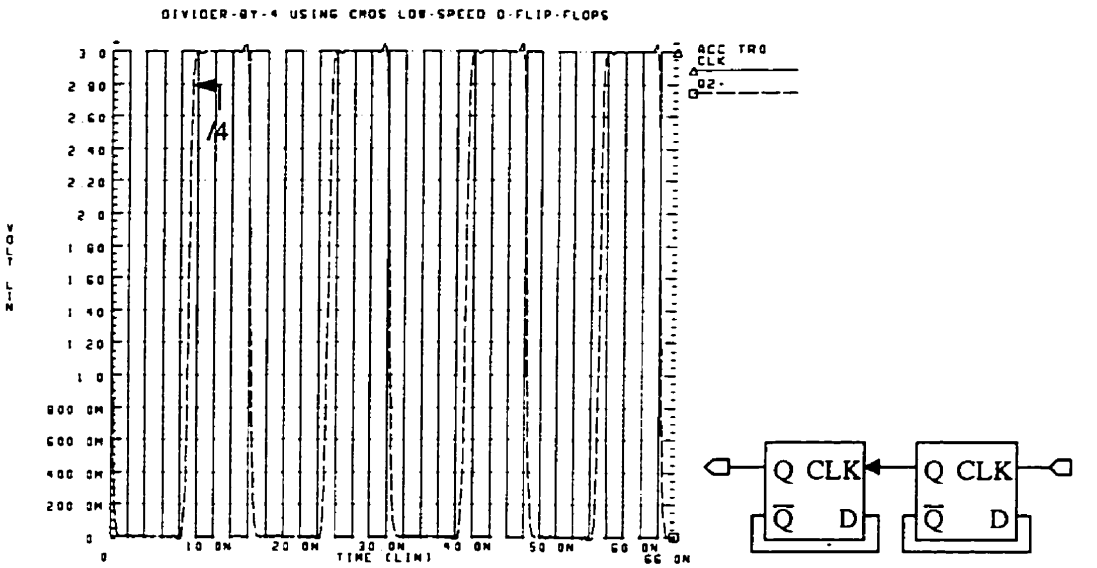


Figure 3.23 Simulated waveforms of two cascaded divide-by-2 circuits with an input frequency of 90% of their maximum frequency

3.5 Phase Modulator

A complete logic diagram of the phase modulator is shown in Figure 3.24. A logic diagram of adders used in the phase modulator is shown in Figure 3.25. The registers are re-used from the design of the resetable D-flip flop in the previous section. The channel select, k, is a 4-bit input and the outputs, S_0 and S_1, are the interfaces to the phase selector which is depicted in Figure 3.26. The AND gates in the phase selector turn the 25%-duty-cycle waveform into a sym-

metric one. A system-simulation software, Ptolemy[1], performs the digital simulation. Figure 3.27 shows the output waveform of the phase modulator.

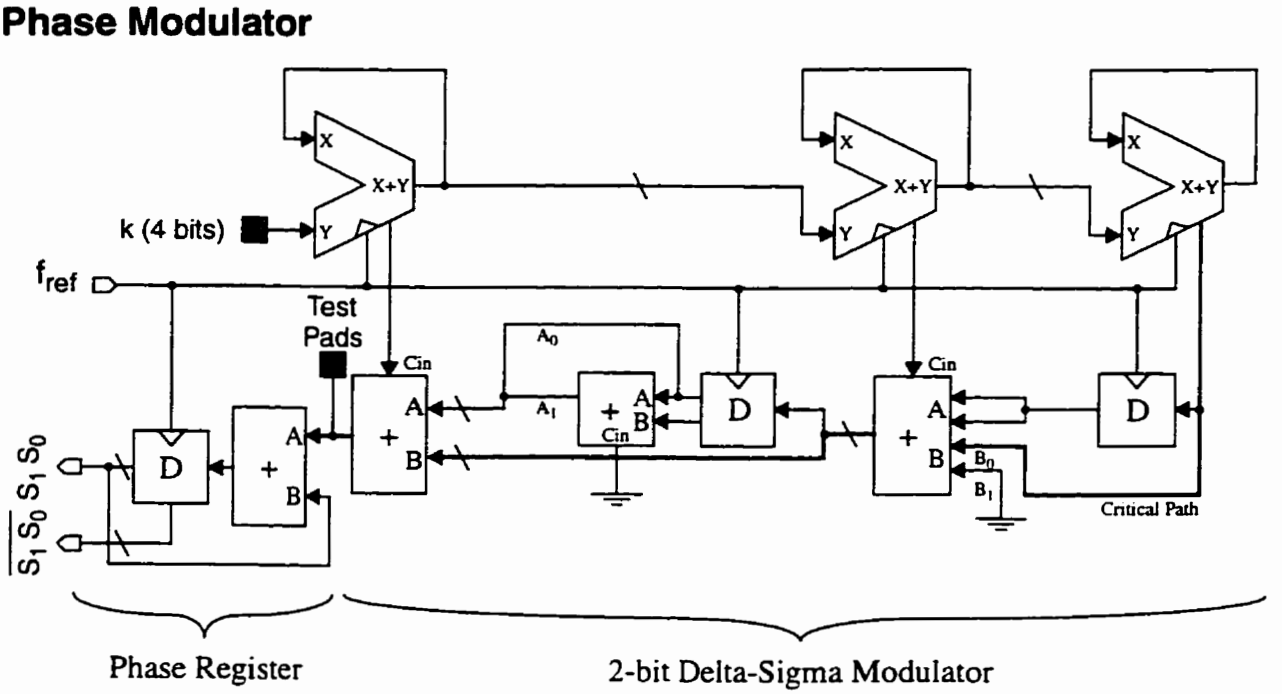


Figure 3.24 Complete logic diagram of the phase modulator (delta-sigma modulator)

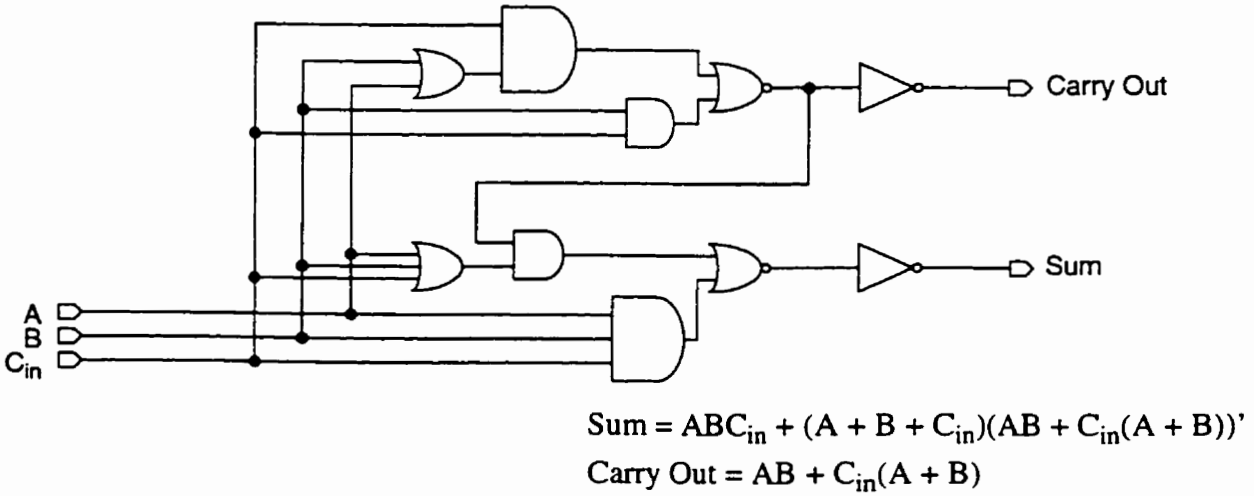


Figure 3.25 Logic diagram of the full adder

1. Ptolemy is developed by UC berkeley and the version we used is 0.7.

Phase Selector (Multiplexer)

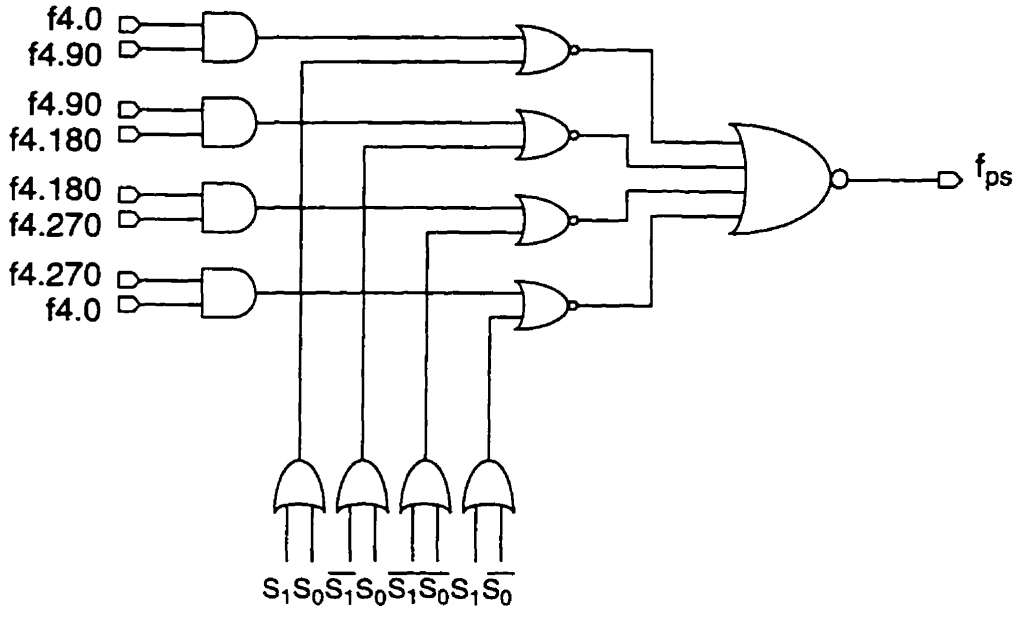


Figure 3.26 Logic diagram of the phase selector

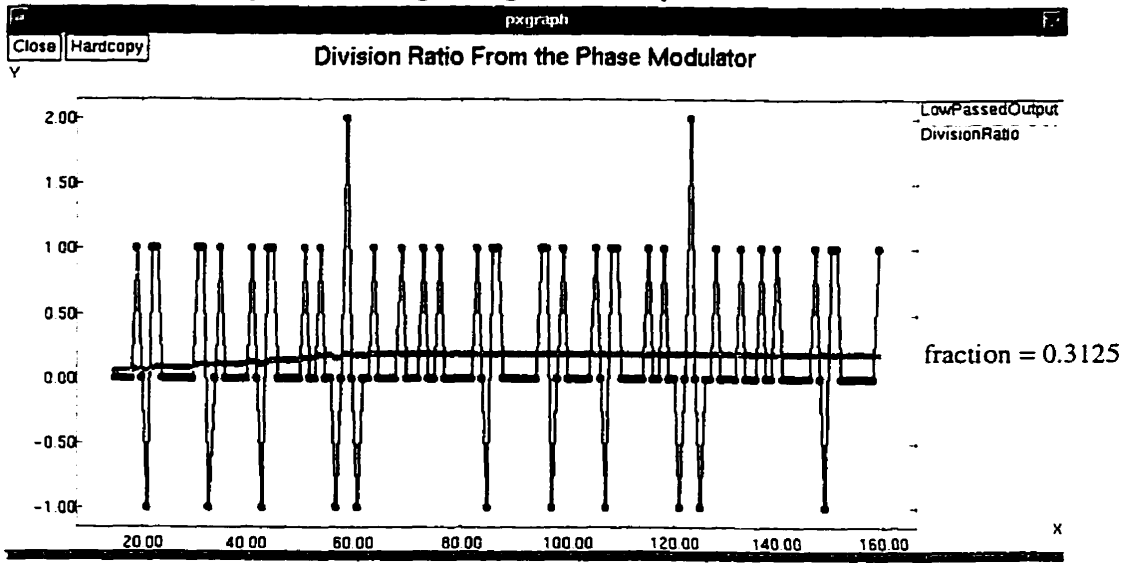


Figure 3.27 Control waveform of the phase modulator (k = 5, n = 4)

3.6 Precharge-type Phase/Frequency Detector

A digital phase/frequency detector (PFD) was chosen for its ease of implementation and the built-in frequency-detection feature. A precharge-type PFD shown in Figure 3.28 is chosen. It is a

modified version from which we discussed in the previous chapter. Not only is it capable of providing a high resolution in the phase difference of two input signals, it can also act exactly as a conventional PFD by adding an NAND gate in front of the original half phase-detector[47]. The NAND gate prolongs the evaluation period and inhibits any succeeding signal from V_{lead} when the phase error is greater than 180°. An external reference oscillator (~3.2MHz) is used to generate the reference frequency for V_{ref}.

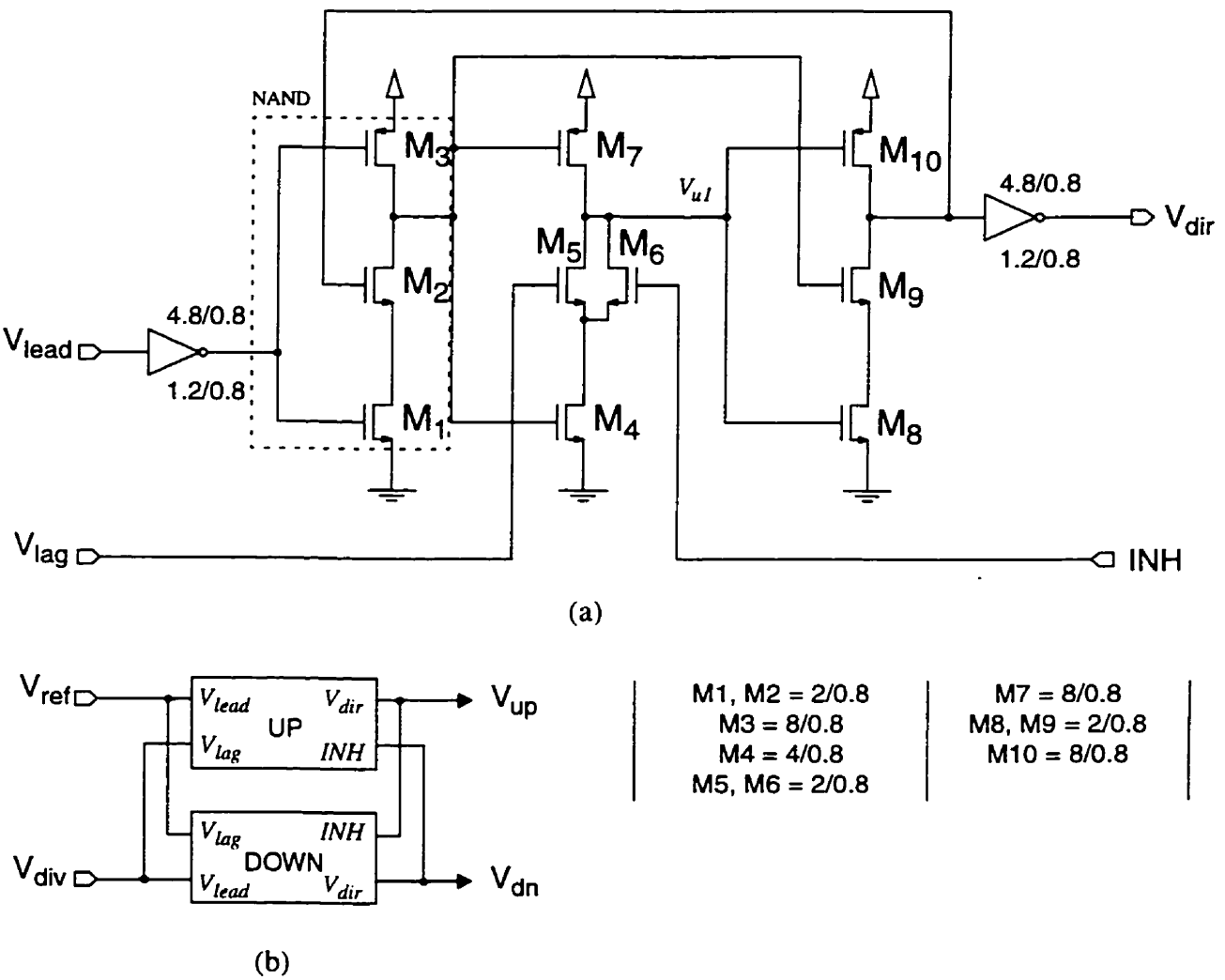


Figure 3.28 Precharge-type phase detector: (a) Half circuit of the phase/frequency detector (b) Complete PFD configuration

Figure 3.29 shows the charge pump with a first-order loop filter. The charge pump contains two wide-swing current switches controlled by the UP and the DOWN signals from the phase detec-

tor. The loop filter consists of a capacitor in series with a resistor and a de-glitching capacitor. In Figure 3.30(a), the PFD is driven at 3.2MHz with an initial phase difference of 1.2° which corresponds to a time difference of 1ns. In Figure 3.30(b), the frequency acquisition is examined by initiating a frequency difference of 3.2MHz.

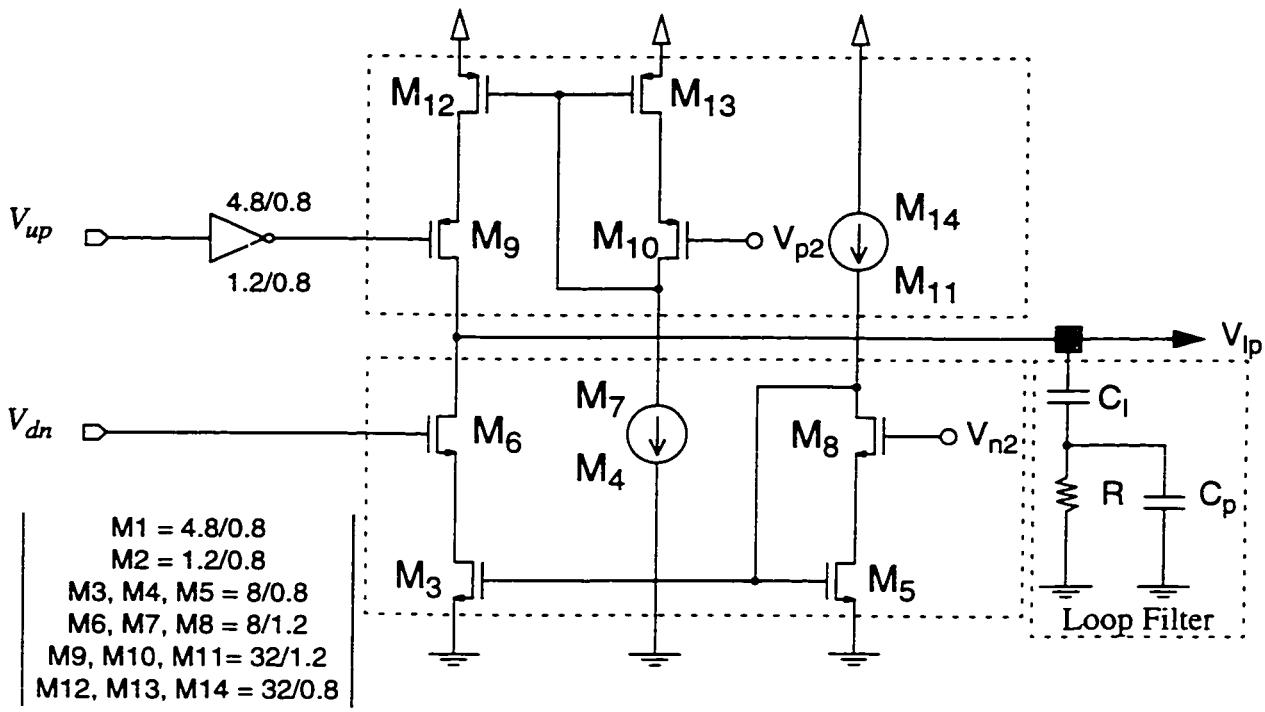
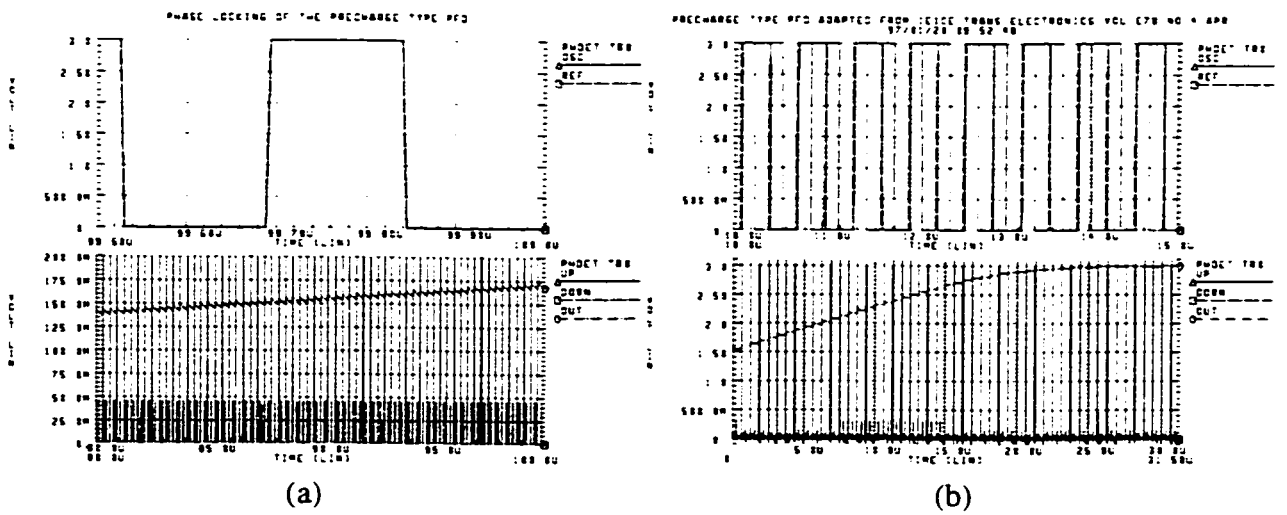


Figure 3.29 Charge pump and loop filter



(a) (b)

Figure 3.30 Simulated waveforms of the PFD for (a) Phase detection (b) Frequency detection

3.7 System Simulation

All circuits in the frequency synthesizer were simulated using Hspice as well as Ptolemy. Ptolemy provides a system-simulation environment that allows linear blocks of the PLL to be simulated much more quickly. A full simulation performed in Hspice would take several days before the phase-locked-loop settled. The reason is due to the fact that the pole of the loop filter is at a much-lower frequency than the oscillation frequency of the VCO. After the oversampling of the system (e.g. a factor of 128) is taken into account, the simulation step is as small as 10ps for a VCO's frequency of 1GHz, while the settling time can be as long as 6/(pole frequency of the loop filter) = $6*\sqrt{256}/200\text{kHz} = 0.5\text{ms}$. For Ptolemy, the simulation takes about only an hour on a Pentium-166. Code of all the blocks are written in C++ and are compiled by a scheduler inside Ptolemy. Futhermore, additional system elements such as mixers and monitoring devices can be easily added to the entire synthesizer.

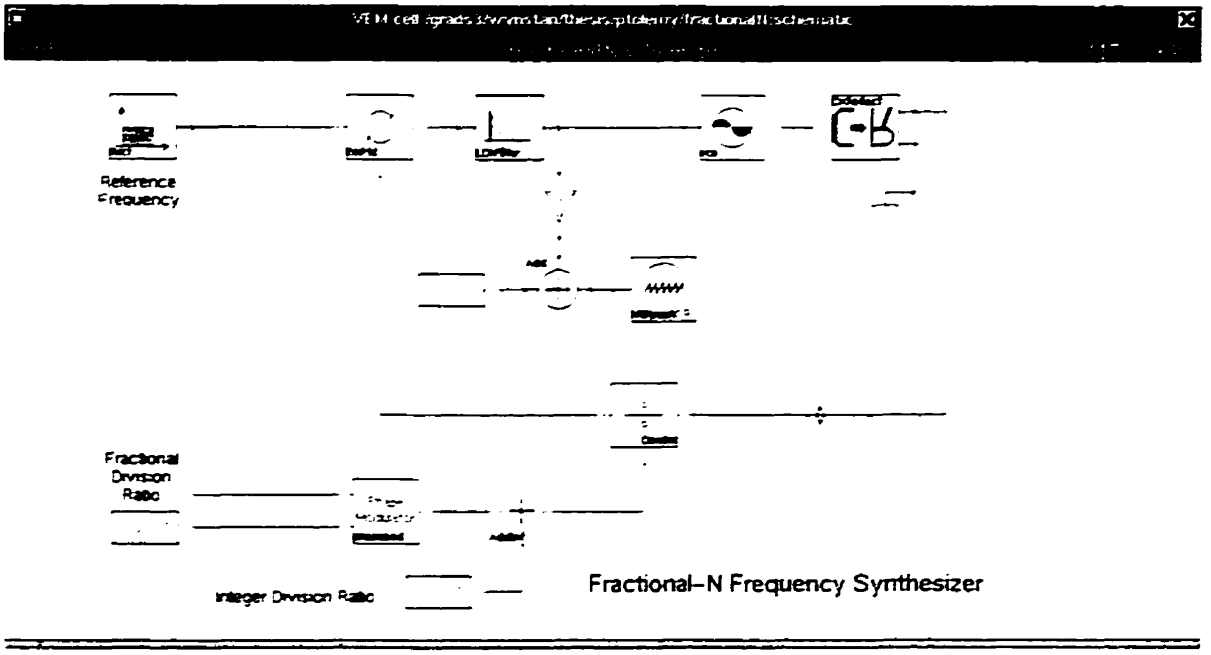


Figure 3.31 Ptolemy block diagram

The Ptolemy block diagram is given in Figure 3.31. The function of each block is readily apparent except for the VCO and the phase modulator. Because the phase of a signal is the integral of the frequency, the VCO is modeled as a gain stage and an integrator. The phase modulator is modeled in its exact form as we discussed before. The phase-frequency detector is emulated by using ideal digital switches to implement the normal and tri-state logic blocks.

The design parameters of the loop filter such as the loop frequency, Q-factor, and charge-pump's current can be edited by pressing "e" on the "LDIfilter" icon. The structure of the loss-less-digital-integrator (LDI) can be found in [37]. It can maintain a high numerical accuracy even in this kind of extreme situation. The division ratio is controlled by adding the output of the phase modulator which provides a fractional value, together with an integer value. The plot in Figure 3.32 shows the system simulation for N = 256 and f_{ref} = 3.2MHz. Frequencies generated with different fractional values, k, are plotted on the graphs below.

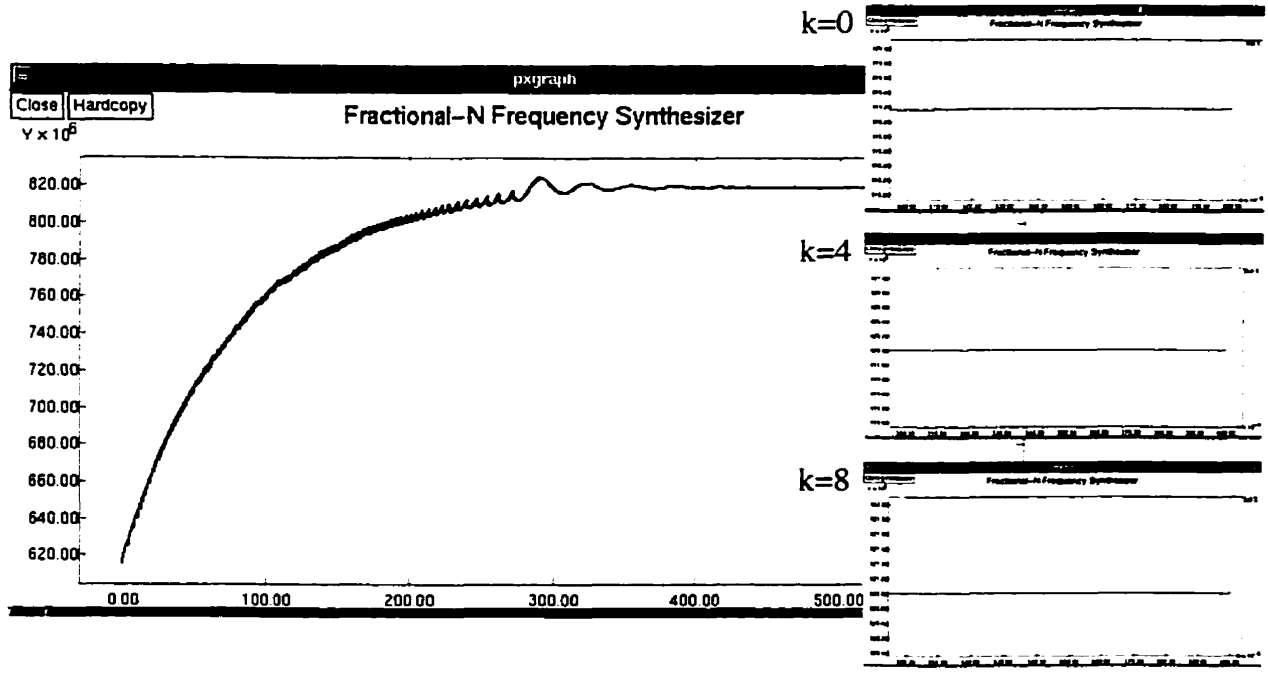


Figure 3.32 System Simulation of the frequency synthesizer

The loop bandwidth is set to be 5kHz and the Q-factor is 0.8. The settling time is about

450us. During the locking period, the control signal resembles an exponential curve even though the system contains some digital elements. As the VCO frequency approaches to the reference frequency times the division ratio, the phase-frequency detector mostly sends out UP signals to advance the phase of the VCO until the control signal settles.

3.8 Layout Considerations

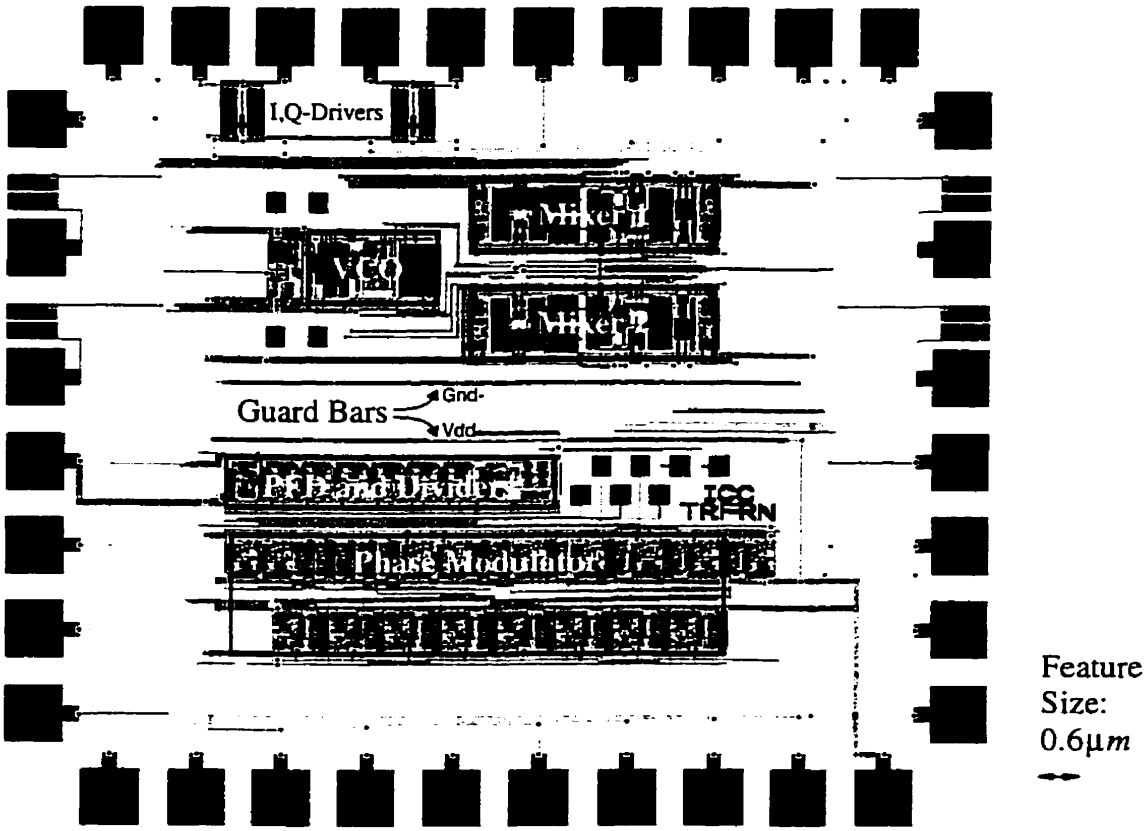


Figure 3.33 The complete layout of the receiver front-end

The above layout was done in Ballistic[48] which allows the designer to write code to place and route each circuit building block by their relative positions. The structure of the layout is based on the figure shown on the first page of this chapter, Figure 3.1. The size of the chip is 1mm x 1.5mm. The off-chip driver is at the upper-left-hand corner. The voltage-controlled oscillator (VCO) is on the left-hand side of mixer 1 and mixer 2 which demodulates the I- and Q-channels

respectively. These parts are running at the highest frequency in the entire design. Therefore, a compact and symmetric layout is desired, so as to minimize the parasitic effects and the layout mismatches. A detailed layout of the ring oscillator is shown in Figure 3.34. A table, which contains the values of the parasitic capacitance at each output node, is also summarized in Table 3. The layout of the mixer is also magnified in Figure 3.35. In order to separate the noise and substrate current coupled from the digital part to the analog part (or vise-versa), two guard bars are placed horizontally in the center of the chip layout. The Gnd-connected guard bar serves as a substrate contact to reduce the possibility of latch-up. The depletion region formed underneath the Vdd-connected guard bar will act as a by-pass capacitor to absorb the high-frequency noise going from one side to another. Decoupling capacitors (~3.3pF) are also placed for stabilizing important voltages, such as the bias voltages and common-mode voltages of the opamp. The multi-modulus divider, the phase modulator and the phase/frequency detector are positioned in the lower part of the chip layout. Test pads are also available next to the chip label. Internal states of the phase modulator and the prescaler can be tested through those test pads.

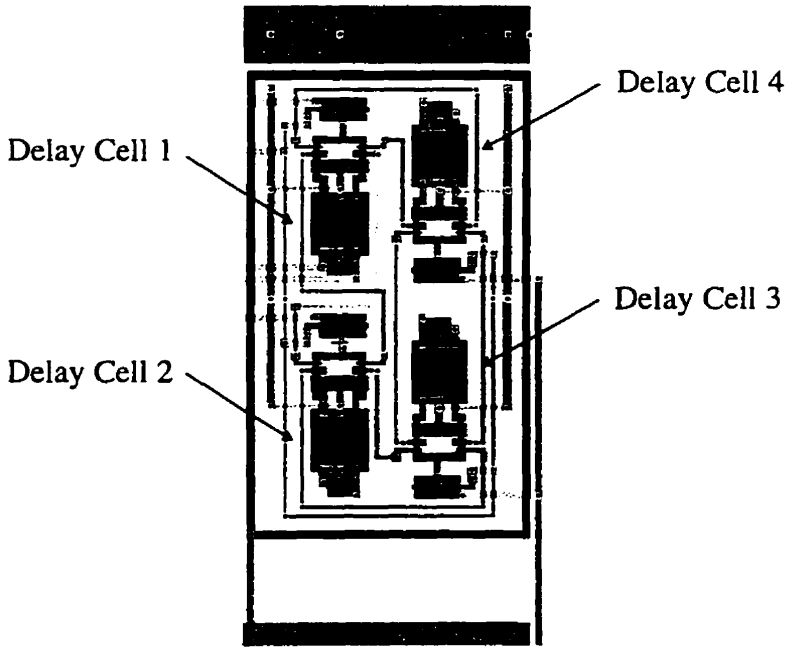


Figure 3.34 Symmetry layout of the ring oscillator

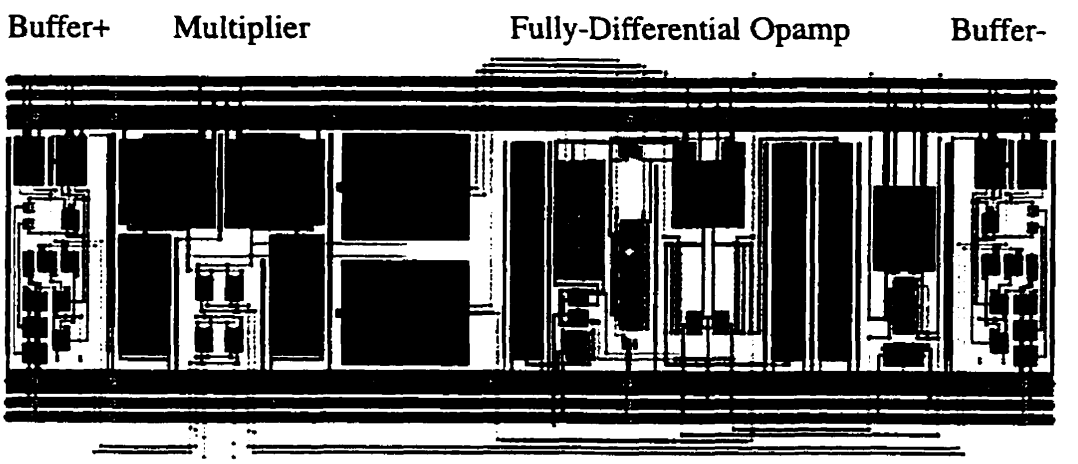


Figure 3.35 Layout of the mixer

Nodes	Capacitance
V_{vco-0+}	9.81ff
V_{vco-0-}	9.84ff
$V_{vco-45+}$	10.01ff
$V_{vco-45-}$	9.98ff
$V_{vco-90+}$	9.97ff
$V_{vco-90-}$	9.94ff
$V_{vco-135+}$	9.83ff
$V_{vco-135-}$	9.87ff

Table 3 Extracted Capacitances of the VCO

3.9 References

[35] N.S. Sooch, "MOS Cascode Current Mirror," *U.S. patent no. 4,500,284*, October 1985

[36] J.M. Steininger, "Understanding Wide-Band MOS Transistors," in *IEEE Circuits and Devices*, Vol.6, No.3, pp. 26-31, May 1990

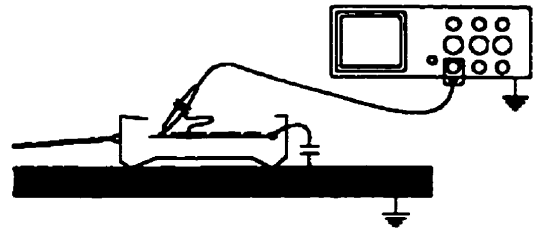
[37] Ken Martin and David Johns, *Analog Integrated Circuit Design*, Wiley, 1996

[38] Beomsup Kim, Todd C. Weigandt, Paul R. Gray, "PLL/DLL System Noise Analysis for Low Jitter Clock Synthesizer Design", Department of Electrical Engineering and Computer Sciences, University of California, Berkeley and Department of Electrical Engineering, Korea Advanced Institute of Science and Technology

[39] Aaron Buchwald, Ken Martin, "High-Speed Voltage-Controlled Oscillator with Quadrature Outputs," *Electron. Letter*, Vol. 27, No. 4, pp. 309-310, Feb 1991

[40] Aaron Buchwald, *Class Note*, The Hongkong University of Science and Technology,

1993
[41] J.K. Roberge, *Operation Amplifiers*, John Wiley & Sons, New York, 1975
[42] Robert Bayruns, R.L. Johnston, and others, "Delay Analysis of Si NMOS Gbit/s Logic Circuits," IEEE Journal of Solid-State Circuits, Vol. 19, No. 5, pp. 755-764, Oct 1984
[43] Jan. Crols and Michiel S.J. Steyaert, "A 1.5 GHz Highly Linear CMOS Downconversion Mixer", in *IEEE Journal of Solid State Circuits*, Vol. 30, No. 7, July 1995, pp. 736-742
[44] Steve Jantzi, Kenneth Martin, M.Snelgrove and Adel Sedra, "A Complex Bandpass $\Delta\Sigma$ Converter For Digital Radio," *ISSCC 1997, http://www.eecg.toronto.edu/~analog/PUBS/adel/www/ Complex_Bandpass_DS_Converter_for_Digital_Radio.ps*, University of Toronto, 1995
[45] Behzad Razavi, F.Lee, and Ran H.Yan, "Design of High-Speed, Low-Power Frequency Dividers and Phase-Locked Loops in Deep Submicron CMOS," in *IEEE Journal of Solid-State Circuits*, Vol. 30, No.2, Feb 1995, pp. 101-108
[46] CMOS5S Cell library, 1990
[47] Harufusa Kondoh, Hiromi Notani, Tsutomu Yoshimura, Hiroshi Shibata, and Yoshio Matsuda, "A 1.5V 250MHz to 3.0V 622MHz Operation CMOS Phase-Locked Loop with Precharge Type Phase-Frequency Detector," *IEICE Trans. Electronics*, Vol. E78 C, No.4, Aprl 1995
[48] Bryn Own, "Ballistic: An Analog Layout Language," *Reference Document*, 1996.



Test Results

4

This chapter describes details of the test setup and the methods of testing for the circuit building blocks. Plots shall be presented in the following sections to illustrate the results.

A high-frequency circuit board was built to test the chip. The board was designed to allow different sections to be tested independently. A photo of it is shown in Figure 4.1.

Figure 4.1 A photo of the test board

The board, containing our testing circuit and a battery holder, is mounted onto a grounded copper plate. The plate allows the board to be more portable and prevents the board from moving around. By limiting the mobility of the circuit board, any fatigue in the solder joints can be avoided.

4.1 Test Setup

#	Pins
1	Vvco
2	Fref
3	Idn
4	Iup
5	$\overline{Rst}$
7	k1
8	k2
9	k3
10	k4
11	Vdd(d)
12	Vdd(a)
14	$\overline{RF}$
16	RF
17	Vcm
19	MxQout
20	$\overline{MxQout}$
22	$\overline{MxQin}$
23	MxQin
24	IFIout
25	$\overline{IFIout}$
26	$\overline{IFQout}$
27	IFQout
29	LOIout
30	$\overline{LOIout}$
31	$\overline{LOQout}$
32	LOQout
33	MxIout
34	$\overline{MxIout}$
36	$\overline{MxIin}$
37	MxIin
39	Gnd
40	Rbias
42	Rctl
44	Vctl

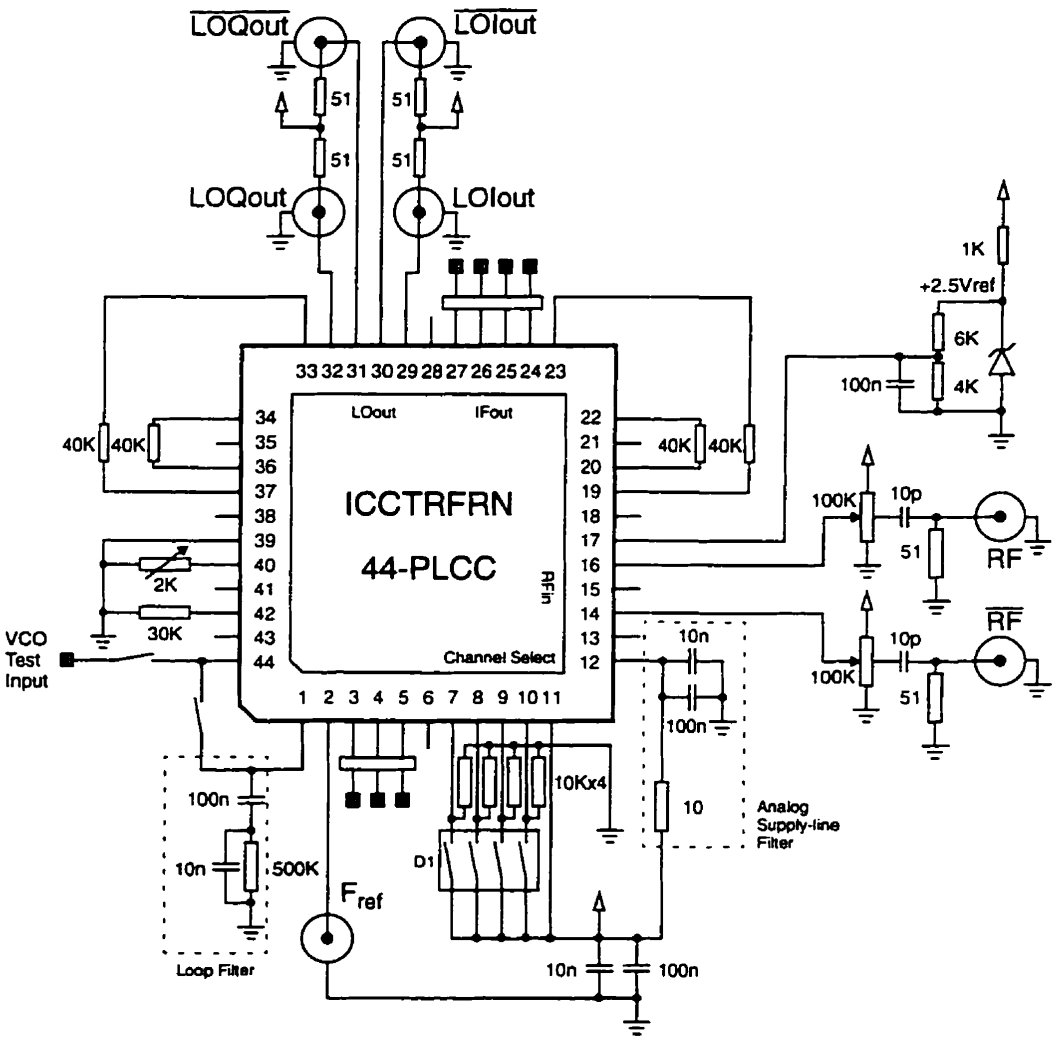


Figure 4.2 Schematic of the test setup

The schematic of the circuit board is shown in Figure 4.2. It provides all supply voltages, i.e. Vdd, Vcm and Vctl, for testing. By generating all the required supply voltages, fewer external

supplies or adjustments are required, and additional filtering can be applied to the supply lines. The chip is packaged in a 44-pin plastic-leadless-chip-carrier (PLCC). The socket in the photo contains the test chip. All bias and supply lines are decoupled at their socket pins with 100nF and 10nF ceramic capacitors. A four-dip switch serves as the digital input for the channel select. All high-frequency lines are connected to SMA connectors and are terminated with 50-ohm resistors.

The testing instruments that were used include a high-speed signal generator(SMT03), a high-speed spectrum analyzer(HP8595E), a low-speed frequency synthesizer(Wavetek395), and a Tektronix medium-speed oscilloscope.

4.2 Bias Circuit

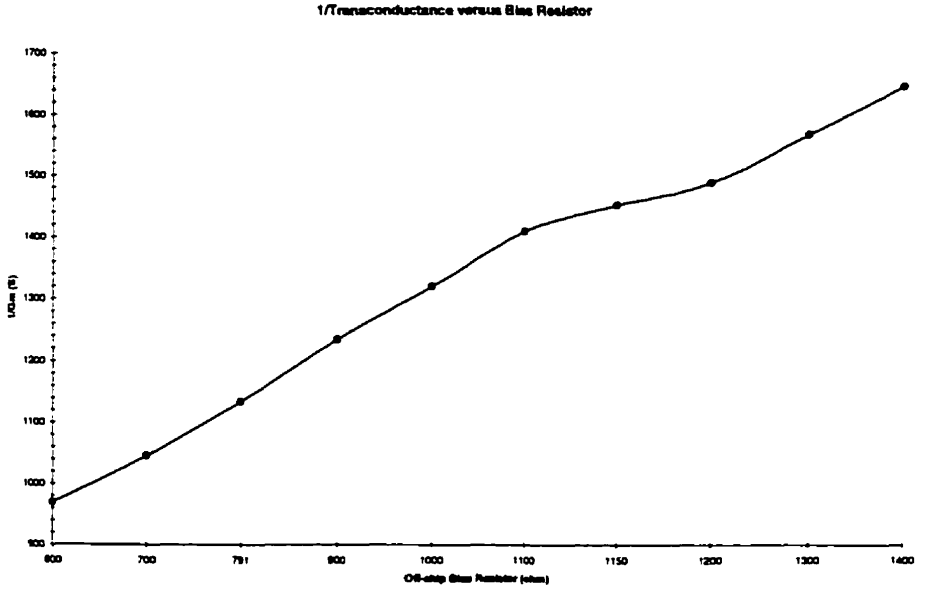


Figure 4.3 A plot of gm versus bias resistor

First, the bias circuit was tested. The bias current is determined by the conductance of a bias resistor. The bias resistor is composed of an internal resistor in series with an external one. The internal resistor has been designed to be 400-ohm, making use of the N-well resistor available inside the chip. The external one is a variable resistor whose maximum value is 1.4K-ohm. By

changing the resistance of the variable resistor, the voltage across it is measured. The transconductance, g_m, is then calculated by $\sqrt{2\mu_n C_{ox}(8/0.8)I_{bias}}$. A slope of 1 is shown in Figure 4.3. It confirms the relationship between the transconductance and the resistance of the bias resistor, i.e. $1/g_m = R_{bias}$.

The difference between the x- and y-intercept represents the value of the internal resistor. It is about 370-ohm as opposed to the 400-ohm as we designed. If we assume the process variation is linear, a factor of 7.5% is reduced.

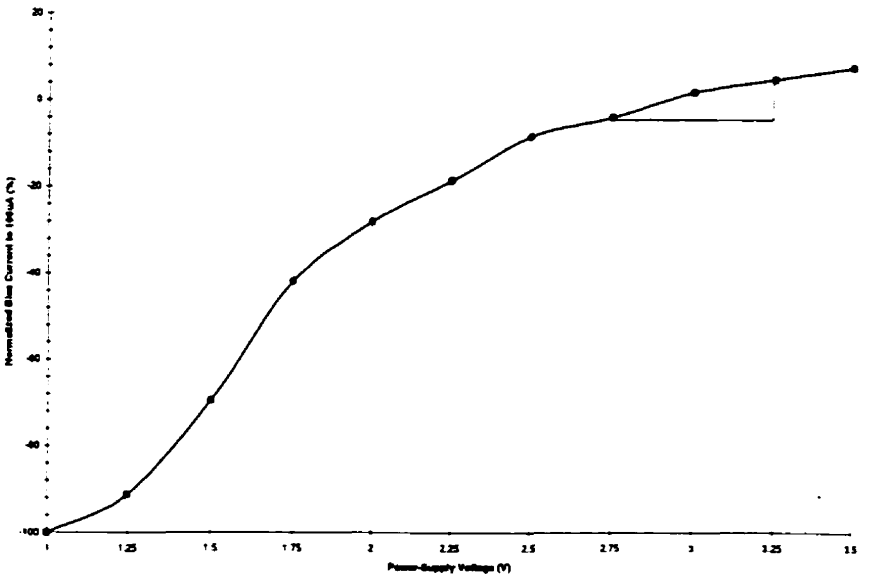


Figure 4.4 A plot of the bias current versus power-supply voltage

The measurement of the sensitivity of bias current over the power-supply voltage is given in Figure 4.4. Since the range of operation voltages are from 2.7V to 3.3V, the bias current can differ +/-5μA, which is about 4.7%, from its nominal value, 106μA.

4.3 Voltage-Controlled Oscillator

The voltage-controlled oscillator(VCO) is one of the two blocks which runs at the highest frequency. The supply voltage is fixed while the control voltage is varied. A plot of frequencies versus the control voltage is shown in Figure 4.5.

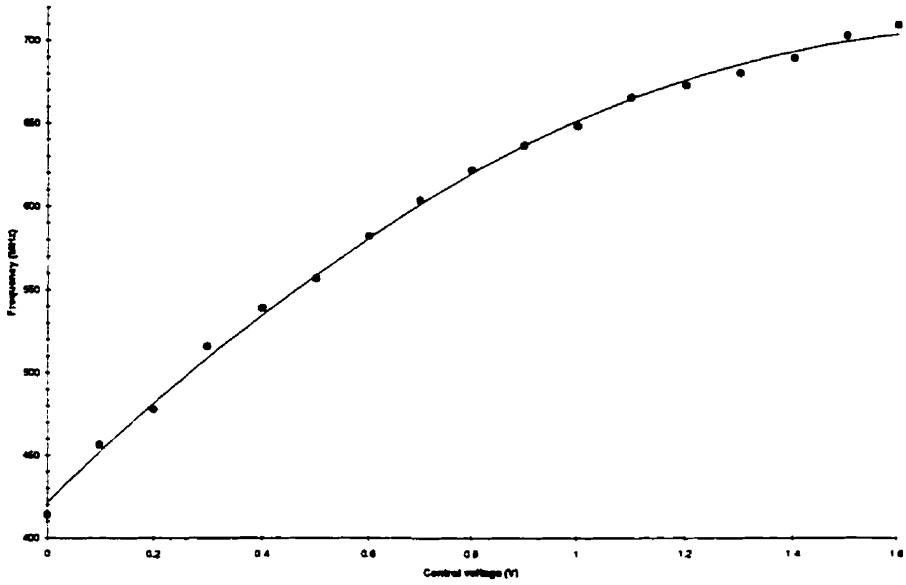


Figure 4.5 Gain curve of the VCO

The above figure shows that the frequency of the VCO does not rise beyond 710MHz even though the control voltage continues to increase. The tuning range is 298MHz. As the bias current increases, which is determined by the control voltage, the sources of the differential pair drop in voltage, until the bias transistor is forced into triode. Once in triode, the bias transistor will not follow the control voltage and the bias current will cease to increase. The effective-gate voltage of the differential pair will also drop and deteriorate the noise performance.

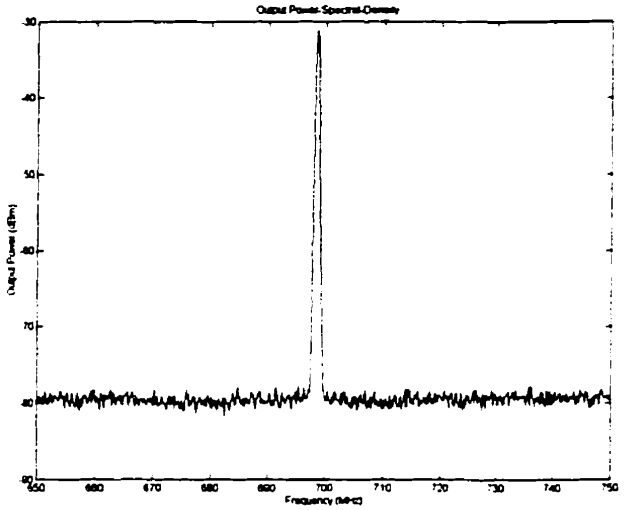


Figure 4.6 Frequency spectrum of the VCO's output - 100MHz span, 1MHz resolution-bandwidth

From the power-spectral-density(PSD) plot depicted in Figure 4.6, a noise floor is clearly visible. The noise floor is 48dB below the signal tone while the strength of the signal is -32dBm at 699.3MHz.

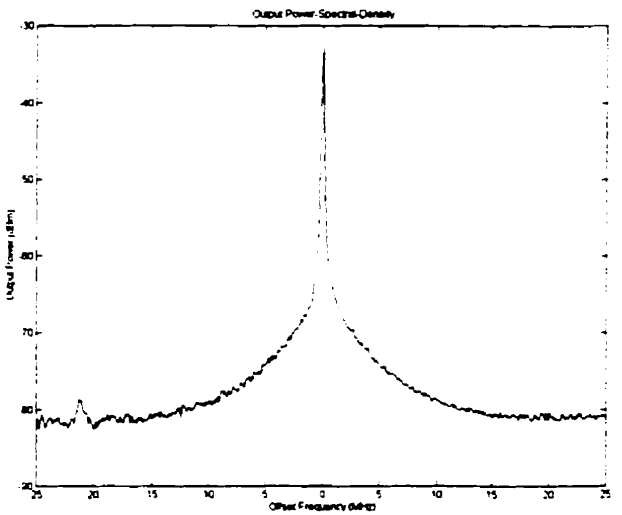


Figure 4.7 Frequency spectrum of the VCO's output - 50MHz span, 100kHz resolution-bandwidth

When the resolution bandwidth of the spectrum analyzer is narrowed to 100kHz, another PSD diagram is plotted in Figure 4.7. The noise floor begins to rise towards the signal tone. A 3dB corner above the noise floor is at 8.42MHz from the signal peak. This corner corresponds to an

effective Q-factor of the oscillator. It is expected that as the VCO becomes less sensitive to noise variations, this corner frequency will decrease. For the noise getting closer to the signal tone, the slope sideband is also rising faster. It is mainly because the 1/f noise of transistors causes the VCO to wander even more and the noise spectrum begins to follow a +30dB/dec slope according to the Lession's Model[49].

Phase Noise Measurement

Another function of the built-in down-conversion mixer is to measure the phase noise of the oscillator. The noise performance is usually given as a plot of RMS power versus the offset frequency from the carrier. This plot is generated by taking the single-sideband power of the phase noise, normalizing it to a 1Hz bandwidth and converting it into the dBc scale. A typical test setup is shown in Figure 4.8.

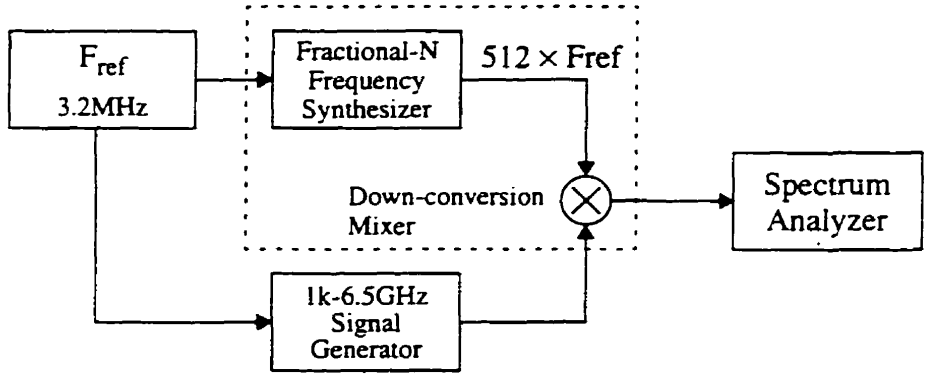


Figure 4.8 Phase noise measurement using a downconversion mixer

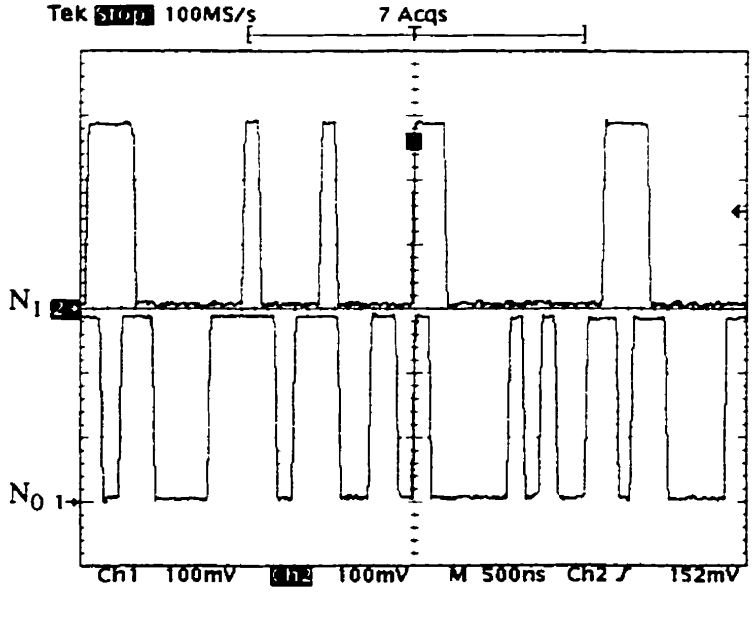
When the two inputs to a down-conversion-mixer are in quadrature, the output of the mixer is equal to the sine function of the phase difference of the input signals. If the level of the phase noise is low, the function $\sin(\Phi)$ can be approximated as Φ . Therefore, the mixer acts as a phase detector, converting the phase noise of the oscillator into a voltage.

4.4 Downconversion Mixer and Prescaler

The differential outputs of the prescaler, f4.0 and f4.180, were probed. Their DC levels were found to be 0V and 2.9V respectively. When the mixers were tested, no oscillation signals could be found from their outputs. The root of these phenomena is due to a wrong connection in the secondary buffer which is responsible to amplify the signal from the VCO to the mixer and the prescaler. The DC level of the mixer's differential outputs were found to be the same as the common-mode voltage input which had been set to be 1.2V.

Since only the prescaler can run at a comparable frequency with that of the VCO and is the front-end of the multi-modulus divider, the dynamics of the PLL cannot be tested. However, further attempts, such as ion-beam implantation and laser cutting, shall be used to re-route the connection in the secondary buffer and correct the mistake.

4.5 Phase Modulator



(k = 5, n = 4)

Steps	N_1N_0	Steps	N_1N_0
1	01	17	00
2	11	18	00
3	10	19	01
4	11	20	01
5	01	21	00
6	00	22T	11
7	00	23	10
8	00	24	00
9	01	25	00
10	01	26	00
11	11	27	00
12	01	28	01
13	00	29	00
14	01	30	01
15	01	31	00
16	11	32	00

Figure 4.9 Control waveform of the phase modulator (10X probes are used)

The states of the phase modulator was examined by probing the test pads next to the phase modulator. A timing diagram downloaded from the oscilloscope and a truth table are shown in the Figure 4.9. The channel select has been set at 5. The period of the waveform is also found to be 32 steps, as we expected.

4.6 References

[49] D.B. Lesson, "A Simple Model of Feedback Oscillator Noise Spectrum," *Proceedings of the IEEE*, February 1966, pp. 329-330

Conclusions

5

All building blocks for a fractional-N frequency synthesizer and a downconversion mixer have been studied, developed and implemented in a standard 0.5μm -CMOS technology. In chapter 1, different methods of frequency synthesis are presented. A basic phase-locked-loop (PLL) with a divider has been used to work as a frequency synthesizer for a long time. In chapter 2, the delta-sigma theory is brought into the traditional PLL design. Thus, a fine resolution for channel frequencies becomes possible without sacrificing too much settling time. In addition, other system issues in the frequency synthesizer, such as the noise performance of the voltage-controlled oscillator, the phase selection technique, and the resolution of the phase detector, are also discussed. Designs of all building blocks are presented in chapter 3. Theories were verified by simulations. Finally, testing results for the circuit building blocks are given in chapter 4.

5.1 Suggestions for future work

Reducing the Circuit Noise

A number of improvements can be made to reduce the sideband noise of the VCO. The control voltage of the VCO should not be connected to any external pin because this voltage is very susceptible to interference. This connection should be isolated or buffered in the final design. The noise floor is high due to the wrapped-wires all over the circuit board. Signal tones from other lab equipment, such as computers, can jam into the spectrum. A wire with a high-frequency signal acts like an antenna and radiates electromagnetic waves to its adjacent wires. Therefore, especially for the RF inputs and the VCO outputs, signal connections have to be shielded by the micro-coaxial cables. Besides, a printed circuit board has to be used and carefully designed for a 50ohm environment so as to reduce the cross-talk and reflection in the high-frequency routes.

From the circuit point of view, one CMOS latch for the output driver is not enough for overcoming the background noise and the attenuation from the external connection. In future designs, one more gain stage would be added to increase the signal strength.

Higher Operation Frequency

In the present design, the maximum oscillation frequency is only 710MHz, which is 165MHz (or 20%) below the simulated value. The degradation arises from the variations in the parasitic capacitance, partly, due to the crossed metal wires inside the chip. In a future design, extra work has to be done to ensure minimum overlaps between metal layers.

As we can observe from the frequency-spectrum plot, the quality factor of our ring oscillator is rather low compared to those of the other oscillators using, for example, the on-chip induc-

tors. The CMOS VCO proposed in [50] has utilized hollow inductors to obtain a high operation frequency up to 1.8GHz with an outstanding phase noise performance. Another VCO design making use of the bondwires' inductance[51] from the same author is also a very valuable reference.

Finally, since it is our first attempt to design a circuit using the HP-0.5um technology, many features have not yet been exploited extensively. In order to achieve higher speed, shorter channel lengths for the differential pairs inside the delay cells and for the prescaler should be used. In addition, BiCMOS is an attractive alternative because Bipolar transistors can be driven with more bias current in the delay unit and the performance of the buffered outputs would be substantially improved.

2nd Generation: A Frequency-discriminator-based Implementation

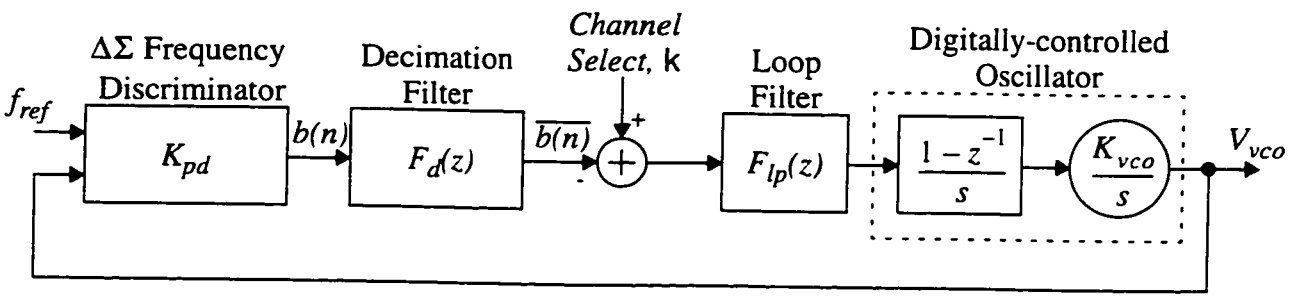


Figure 5.1 A frequency-discriminator-based frequency synthesizer

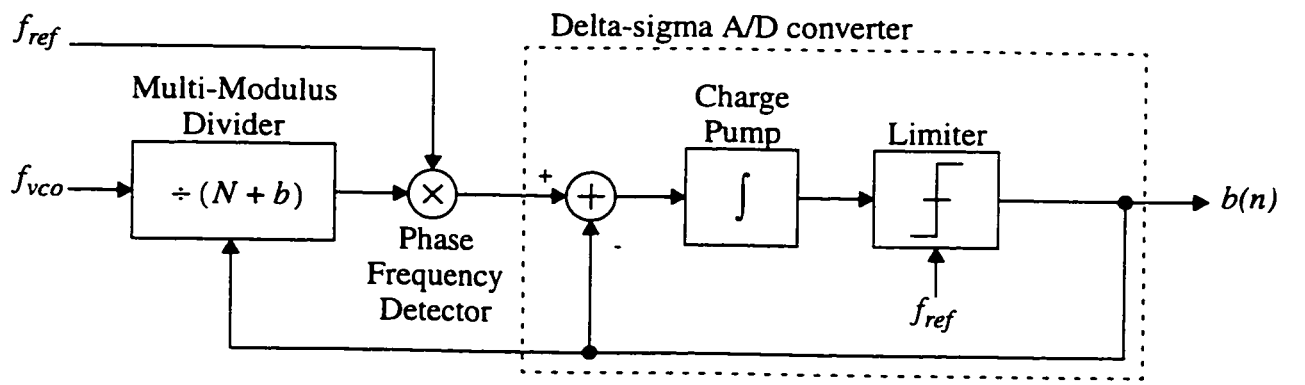


Figure 5.2 A delta-sigma(ΔΣ) frequency-discriminator

In Figure 5.1, a frequency-discriminator-based frequency synthesizer[52][53] is presented. The details of the delta-sigma frequency-discriminator[54] in the loop is shown in Figure 5.2. Simply speaking, the working principle is that the average density of the delta-sigma bit-stream, *b(n)*, is trying to equal the channel select, k. The VCO will increase or decrease its own frequency according to the difference between $\overline{b(n)}$ and k, until they are both equal.

The oversampling delta-sigma A/D inside the frequency discriminator directly converts the phase difference into the bit-stream, *b(n)*. This *b(n)* can reflect the offset of the VCO's frequency from $N \times$ Reference-Frequency by means of the feedback in the multi-modulus divider[54]. The use of the decimator allows the rest of the digital circuits to run at a lower rate, without introducing any new quantization error to the measured frequency from the VCO. The loop filter is implemented digitally to control the loop bandwidth. To close the loop, a D/A converter is required in front of the VCO. An implementation using an active time integrator with an opamp has been done in [55].

A number of advantages of using the above approach have also been discussed in [53], which include

- Robustness from the digital implementation
- Better integration for there is no need to use large RC constant in the charge pump
- Flexible designs in the loop filter

All of the above give us a new direction for how indirect analog frequency synthesizers should go and we hope to implement these ideas into a single-chip solution in our future designs.

5.2 References

[50] Jan Craninckx, and Michiel Steyaert, "A 1.8GHz Low-Phase-Noise CMOS VCO using

Optimized Hollow Spiral Inductors," *IEEE Journal of Solid-State Circuits*, Vol., 32, No. 5, May 1997, pp 736-744

[51] Jan Craninckx, and Michiel Steyaert, "A 1.8GHz low-phase-noise voltage controlled oscillator with prescaler," IEEE Journal of Solid-State Circuits, Vol. 30, pp.1474-1482, Dec. 1995

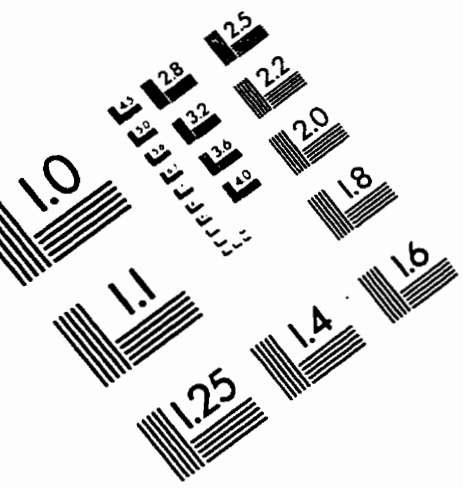
[52] Ian Galton, "Analog-Input Digital Phase-locked loops for Precise frequency and Phase Demodulation, "*IEEE Transactions on Circuits and Systems*, Vol. 42, No. 10, October 1995

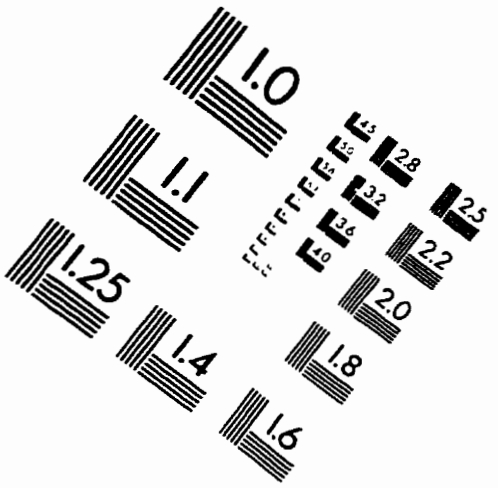
[53] Tom A.D. Riley, Miles A. Copeland, "A 2GHz Low-Power Frequency Synthesizer," *Papers of the Workshop on Advances in Analog Circuit Design*, April 1995

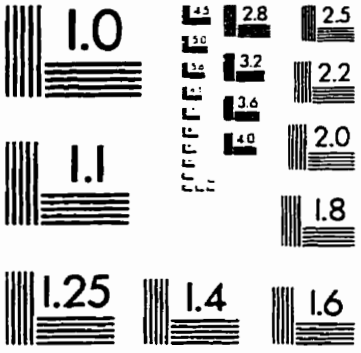
[54] R. Douglas Beards, Miles A. Copeland, "An Oversampling Delta-Sigma Frequency Discriminator," *IEEE Transactions on Circuits and Systems - II*, Vol. 41, No. 1, Jan. 1995, pp 26-32

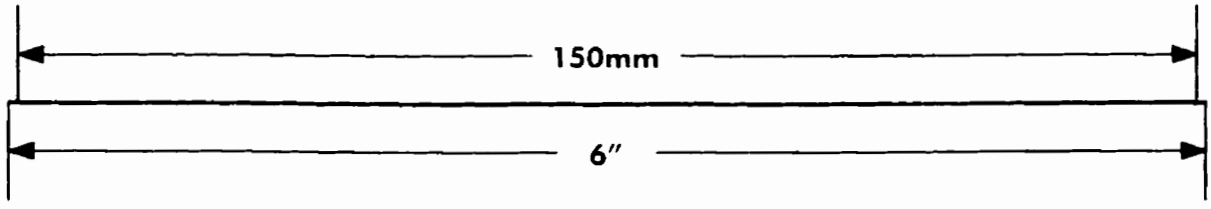
[55] Walt T.Bax, Tom A.D. Riley, Calvin Plett, Miles A. Copeland, "A Delta-Sigma Frequency Discriminator Based Synthesizer," *Proc. IEEE ISCAS*, May 1995

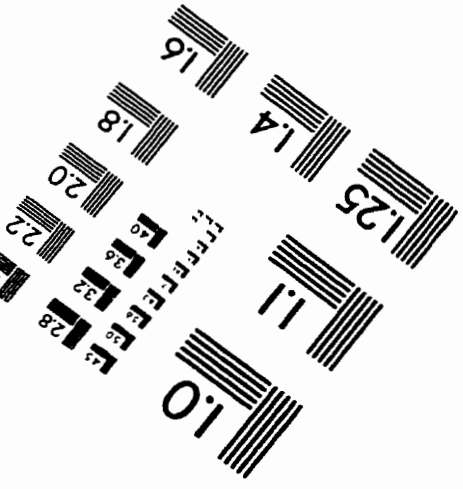
IMAGE EVALUATION TEST TARGET (QA-3)

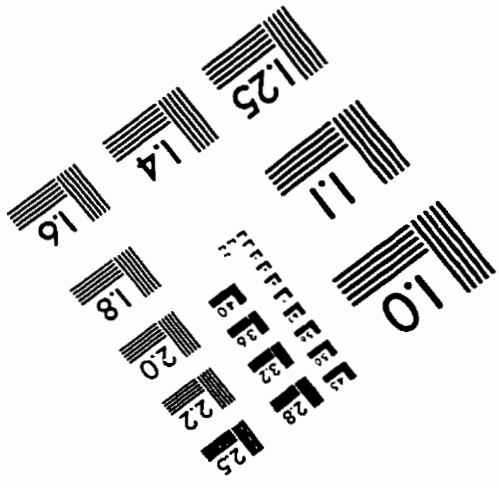












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