

**A 3.8-6.4GHz Local Oscillator System
Using an Injection-Locked Frequency Doubling
and Phase Tuning Technique**

by

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A thesis submitted in conformity with the requirements
for the degree of Master of Applied Science
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Abstract

This thesis studies the design of a novel local oscillator system based on low-voltage and low-power regenerative (injection locking) techniques. The LO system converts an input signal of frequency $f_{LO}/2$ into a quadrature pair of LO signals at a frequency of f_{LO} , intended to drive a pair of I and Q down-converting mixers. A new IC compatible technique for regenerative frequency doubling is presented. Regenerative frequency doublers are cascaded on-chip to provide a net multiply-by-4 function, generating frequencies in excess of $\frac{f_T}{2}$ without the need for interstage filtering. A new technique is also presented for frequency-independent phase control of the quadrature LO signals of a regenerative divider (I-Q generator), achieving a precision on the order of 0.01° . Results are presented in the context of a fabricated 5-6GHz image reject receiver.

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CHAPTER

1

Introduction

1.1 Introduction

The success of cellular telephony and the internet has lead to growing consumer demand for wireless connectivity, products, and services. Although the vast majority of this growth so far has been in mobile voice telephony applications, there is increasing interest in low-rate wireless data applications such as message services or wireless e-mail to consumers[1]. Significant advancements in the area of radio-frequency integrated circuit (RFIC) technology are required to achieve the power, performance, cost and size requirements for these next-generation wireless applications.

In this thesis, new RF circuit techniques are presented which enable an increased level of system integration in an integrated receiver by providing a means of frequency multiplication and precise phase quadrature signal generation. The phase accuracy of the quadrature signals realized enables a Hartley-type downconverter to achieve an image rejection that is sufficient to eliminate the requirement for external (discrete) RF filters in the first RF stage of a receiver. This allows for a simpler package and increased design flexibility without sacrificing significant receiver performance. These techniques are demonstrated in a test receiver IC in the 5-6 GHz band as this is an area of increasing commercial interest for broadband wireless data communications.

1.2 Next Generation Wireless LAN

Over the last five years, the unlicensed 900MHz ISM (instrument, scientific and medical) band (13MHz of spectrum) has become completely saturated in many urban centers by low-end applications such as cordless phones, cheap analog extensions, remote control devices, etc. In anticipation of this congestion, the 2.4 GHz ISM band (which has roughly 83 MHz of spectrum) is considered as an up-banded alternative for WLAN applications. However, the ISM band at 2.4GHz is insufficient for the anticipated level of activity in WLAN, although it is available worldwide. In the late 90's, 300-500 MHz of licence-exempt spectrum in the 5-6GHz band was allocated in many regions[2,3], which can be used for both fixed and portable wireless multimedia applications at data-rates between 20 and 150 Mb/s.

1.2.1 Frequency Specifications and System Design Challenges

Table 1.1 Comparison of various WLAN standards [4,2,3]

Standard	Bluetooth	HomeRF	IEEE 802.11b FH	IEEE 802.11b DS-SS	HIPERLAN	IEEE 802.11a UN-II	HIPERLAN/2
Frequency allocation	2.402 -2.480 GHz	2.404 -2.478 GHz	2.400 -2.4835 GHz	2.400 -2.4835 GHz	5.15-5.35 GHz	5.150-5.350 and 5.725-5.825 GHz	5.150-5.350 and 5.425-5.725 GHz
Total spectrum	78 MHz	74 MHz	83.5 MHz	83.5 MHz	200 MHz	300 MHz	500 MHz
Modulation scheme	FHSS-1600hops/sec, GFSK	FHSS-50hops/sec, FSK & 4-FSK	FHSS-variable, 2-FSK, 4-FSK,...	BPSK, QPSK	Differential GMSK	OFDM 52-car. BPSK,QPSK, 16QAM, 64QAM.	OFDM 52-car. BPSK,QPSK, 16QAM, 64QAM.
Peak raw data-rate	0.721 Mbps	0.8 and 1.6 Mbps	1 and 2 Mbps	11 Mbps	23.5 Mbps	54 Mbps (increase proposed)	54 Mbps (increase proposed)
RF channel bandwidth	1 MHz	1 MHz	1MHz	22MHz	23.5 MHz	20 MHz	20 MHz

Table 1.1 compares the key physical-layer attributes for some of the more popular WLAN standards in order of increasing data-rate from left to right. Although the 802.11b standard enables a rate of 11 Mbps (competitive with the Ethernet rate of 10 Mbps), there is a growing movement to use the 2.4GHz band exclusively for sub-1 Mbps applications due to the limited total channel capacity (limited by the 83.5MHz spectral width available). Wireless computer peripheral devices that are supported by Bluetooth and HomeRF standards, add more electromagnetic clutter to the 2.4 GHz band and motivate migration to the 5-6GHz band for Mbps WLAN.

One of the challenges faced by RFIC designers of next generation WLAN equipment, is the doubling of operating frequency and increase in bandwidth compared to the previous (2.4GHz) generation. Power consumption is always an important consideration in portable applications, and a significant increase in bias current for the RF circuits (for a given technology) can be expected as the frequency of operation is doubled due to the relationship between device bandwidth and supply current. New low-voltage topologies are therefore needed to keep the overall power dissipation down and maintain supply compatibility between analog and digital circuit blocks. Also, tuning range is arguably one of the most important considerations for architects of a 5-6 GHz receiver.

According to the IEEE 802.11a standard, the frequency allocations for unlicensed operation in North America (UN-II) have been split into two bands: 5.15-5.35GHz and 5.725-5.825GHz[2]. In Europe however, the HIPERLAN/2 standard shares the lower band with UN-II but specifies the upper band at 5.47-5.725GHz[3]. Other non-WLAN potential applications lie in the 5.8-5.9GHz region where international allocations have been made for intelligent transportation system services using dedicated short-range communications[5]. Unlike the spectral allocations for cellular telephony, the specific frequency plan (including the uplink and downlink splits) within the unlicensed band can be determined arbitrarily by the applications engineer. A 1 GHz tuning range, centered at 5.5 GHz, represents a 20% relative bandwidth or tuning ratio, which is significantly larger than the 3% requirement at 2.4 GHz. Although none of the 5-6GHz WLAN standards currently require the receiver (or transmitter) to tune over the entire band, the lack of a unified global standard encourages the design of a wideband generic IC in order to broaden the scope of its application.

At the time of writing, two commercial solutions have appeared on the market for the 802.11b standard[6][7]. Both are highly integrated, two-chip solutions implementing both RF and baseband functions in standard CMOS processes.

1.3 Organization of this thesis

Chapter 2 of this thesis begins with a general discussion of the heterodyne and image-reject receiver architectures, followed by an overview of the process technology and a

description of the 5-6 GHz receiver testchip. One of the main goals of this work is to enable an increased level of integration in a receiver by eliminating the need for an off-chip image-reject filter in the RF front-end. The challenges and benefits involved in replacing this filter are discussed in detail, and an integrated receiver concept is presented to accomplish this.

The main focus of this work is on the generation of a pair of highly-accurate quadrature-phase-shifted local oscillator signals at 5-6 GHz. Injection locked oscillators are employed in the design and enable a new method of frequency doubling on an IC. The underlying concept of an injection-locked oscillator is studied and then extended to the locking of ring-type oscillators. Hand analysis and Simulink models are used to illustrate the key characteristics of the injection-locked ring-oscillator. Injection-locking techniques are exploited in both frequency-doubling and dividing circuits to generate local oscillator signals for the receiver. The multi-oscillator system employed in the IC is presented along with the schematics of the individual oscillators and a full discussion of their operation. The thesis is concluded with an overview of the test setup and a discussion of the measured results.

CHAPTER

2

The Local Oscillator System

This chapter begins with a review of superheterodyne and image-reject receiver architectures, followed by a block-level description of the test-receiver IC characterized in this work. The portion of the receiver referred to as the “local oscillator system” is defined, and a breakdown of its requirements and design specifications is given. The process technology used to fabricate the IC is also presented and discussed briefly within the context of a 5-6 GHz receiver.

Frequency doubling is an important part of the contribution of this thesis and so a background review of some of the current methods of frequency doubling on an IC is covered at the end of the chapter.

2.1 The Basic Superheterodyne Receiver

The superheterodyne receiver is one of the most common receiver topologies employed in radio communication systems today. Invented by Edwin Armstrong in the early 1900’s, the basic structure is illustrated in Figure 2.1. This block diagram shows an example of the heterodyne concept applied to an AM (amplitude-modulated) broadcast-band application.

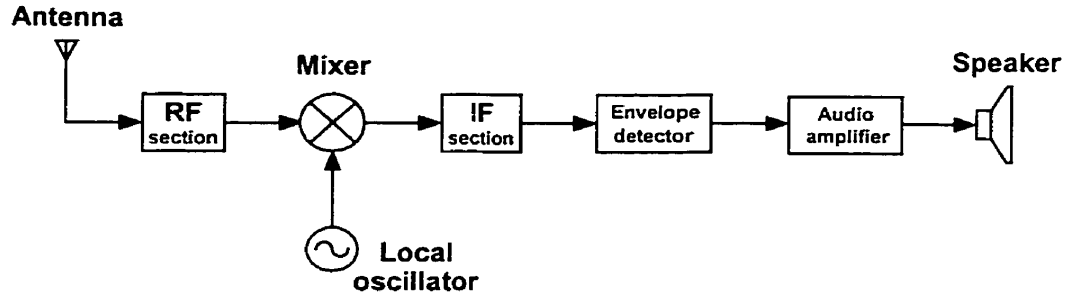


Figure 2.1: Single-conversion superheterodyne AM-receiver block diagram.

The general requirements of a receiver include: the ability to select the desired RF signal (or station) through carrier-frequency tuning, filtering out unwanted or adjacent channels, as well as amplifying the desired signal. In addition to these requirements, the information contained in the received signal must be extracted (i.e. demodulated). In the case of the AM-radio example, the received radio waves from the distant station are converted to audible sounds at the speaker.

Beginning at the left of the diagram, RF waves are picked up by the antenna and fed to the input of the receiver. The RF section typically provides signal amplification as well as some bandpass filtering. In an AM broadcast-band radio, the RF section is designed to amplify signals from 535KHz to 1600KHz and to also reject signals at frequencies which are outside of this band.

The local oscillator (LO) block generates a constant envelope (or non-modulated) carrier-wave (CW) signal which is multiplied with the received RF signal in the mixer. The result of the multiplication is a double-frequency translation of the input signal, up and down in frequency, by the LO. This multiplication can be expressed by the equation,

$$A_m(t) \cos(2\pi f_{RF} t + \phi_m(t)) \cdot \cos(2\pi f_{LO} t) = \frac{A_m(t)}{2} [\cos(2\pi(f_{RF} + f_{LO}) t + \phi_m(t)) + \cos(2\pi(f_{RF} - f_{LO}) t + \phi_m(t))], (2.1)$$

where $A_m(t)$, $\phi_m(t)$, and f_{RF} represent the amplitude modulation, phase modulation, and frequency of the input RF carrier, and where f_{LO} represents the frequency of the LO. From the right side of equation 2.1, it can be seen that the RF input signal is converted from f_{RF} to a pair of signals found at $f_{RF} + f_{LO}$ and $f_{RF} - f_{LO}$ at the output of the mixer. Also,

amplitude and phase modulation of the original signal is preserved in the translated outputs. The use of frequency translation (or frequency conversion) in this way is heterodyning.

In the receiver of Figure 2.1, the desired RF signal is down-converted by the LO to a lower, fixed intermediate frequency (or IF). By adjusting the frequency of the LO, the frequency of the signal being received is “tuned” to fall into the chosen IF band,

$$f_{RF} - f_{LO} = f_{IF} \quad (2.2)$$

In the IF section, the received signal is amplified and passed through a fixed-frequency channel-select filter. This filter is designed to suppress both adjacent as well as out-of-band signals, and provides frequency selectivity in receiver. The width of the passband of the channel-select filter is determined primarily by the channel spacing and modulation characteristics of the signals being received.

The IF is usually chosen to be much lower in frequency than the signals being received in order to realize a number of practical advantages, such as: increased efficiency in the amplifying devices, a reduction of unwanted parasitics, and a relaxed relative bandwidth ($\Delta f/f_o$) requirement for the channel-select filters. Consider for example, a receiver which is designed to receive a 100KHz channel at 1 GHz. If channel-select filtering is implemented directly at RF, then a filter with a 0.01% relative bandwidth would be necessary. This is an extremely difficult specification to meet at 1GHz with current filtering technology[8]. A single-pole RLC filter for example, requires a resonator quality factor on the order of 10,000 (i.e., 1/relative bandwidth)[9]. Implementing the channel-select filtering directly at the IF is an alternative. Consider the same passband filtering requirement when implemented in the IF section, after translating the received 1GHz signal down to an IF of 1MHz. The relative bandwidth is now 10% and the Q-factor requirement for the resonator has been reduced to 10. This relative-bandwidth parameter flexibility is one of the key reasons why the heterodyne architecture is so popular.

The circuit blocks in Figure 2.1 to the right of the IF section complete the AM receiver. All of the blocks lying in the path of the received signal from the IF section to the end of the receiver, are collectively known as the “back-end” of the radio. The back-end in Figure 2.1 is capable of receiving and demodulating AM signals at the IF and is essentially a fixed-

frequency receiver. Conversely, the “front-end” of the radio is everything in the receive path prior to the IF and is in essence a frequency converter. It should be noted however, that the LO generator (or synthesizer) is not in the direct path of the received signal and is therefore not included as part of the front-end.

2.2 The Image band in a Heterodyne Receiver

In equation 2.1, the process of mixing the LO with the RF was shown to generate two products, one at the sum of the LO and RF frequencies (referred to as the upconversion) and one at the difference between them (downconversion). The upconversion term can be ignored since it is filtered away in the IF section, leaving only the downconversion term,

$$x_{IF}(t) = \frac{A_m(t)}{2} \cos(2\pi(f_{RF} - f_{LO})t + \phi_m(t)) . \quad (2.3)$$

Equation 2.3 is appropriate in situations where the frequency of the RF signal being considered is above the frequency of the LO. Since a cosinusoid is an even function of time, equation 2.3 can also be written as

$$x_{IF}(t) = \frac{A_m(t)}{2} \cos(2\pi(f_{LO} - f_{RF})t - \phi_m(t)) \quad (2.4)$$

if the frequency of the RF signal is below the frequency of the LO. From equations 2.3 and 2.4, the RF signal frequencies which will be converted to a specific IF for a given LO frequency are

$$f_{RF} = f_{LO} \pm f_{IF} . \quad (2.5)$$

This means that for a 500MHz LO and a 10MHz IF, a mixer will convert RF signals received at both 510MHz and 490MHz to the IF. The RF band located above the LO is referred to as the upper sideband (or USB) whereas the RF band below the LO is referred to as the lower sideband (or LSB). In many applications, only one of the sidebands is desired. The unwanted part of RF spectrum which converts to the IF is commonly referred to as the “image” band. This is illustrated in Figure 2.2 for the case where the LSB is the desired RF band to be received.

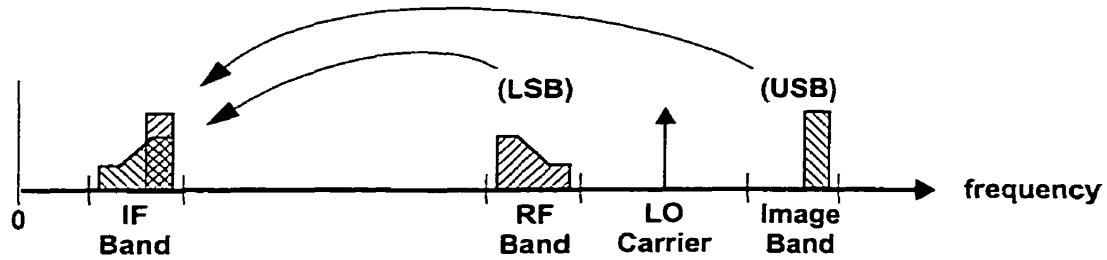


Figure 2.2: Frequency spectrum showing a double sideband (DSB) down-conversion.

The image band in a receiver is normally filtered out before mixing so that only the desired (RF) band is converted to the IF. The amount of image band suppression (or image rejection) in a receiver is an important receiver performance specification. In high-end wireless applications, a total image rejection (IR) on the order of 70-100dB is typically required[10].

2.3 Filtering out the Image Band

Figure 2.3 illustrates a common heterodyne front-end employed in many receiver designs to reject the image.

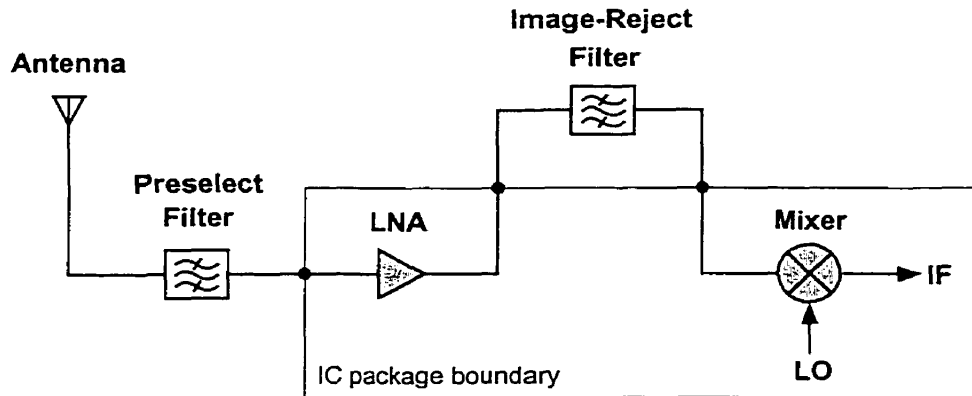


Figure 2.3: Conventional integrated heterodyne receiver front-end.

The RF input signal at the antenna passes through a preselect filter which band-limits the input of the receiver to prevent out-of-band carriers from desensitizing or overloading the low-noise amplifier (or LNA). In situations where the image band can be designed to fall

outside of the passband of this filter, an image rejection on the order of 20dB is realized. The stopband attenuation of this filter is typically limited by the amount of insertion loss that can be tolerated at the input of the receiver, as this adds directly to the overall noise figure of the system[11]. The bulk of the image rejection in an integrated application is usually provided by a second off-chip filter placed between the LNA and mixer. This IR filter is typically more aggressive than the preselect filter (~ 45dB), and has a higher insertion loss (~3-4dB). The noise introduced by the this second filter is acceptable since it is suppressed by the gain of the LNA[11].

A common design strategy employed in tandem with this filtering arrangement is to use a multiple frequency-conversion scheme so that the RF and image band are widely separated (which relaxed the image filtering requirements), while subsequent IFs are chosen to be much lower in frequency to relax the relative bandwidth requirements for channel selection filtering or to suit A/D conversion requirements.

This front-end topology works well in many low-cost integrated circuit packages up to the 2-3GHz range[12,13,14]. In the 5-6GHz range however, receiver performance is unnecessarily compromised by having to route RF signals through off-chip filtering components. Wideband impedance matching networks required to match the on-chip LNA and mixer to the external filter introduce loss. Also, undesired mutual coupling across bond wires of the package and among the printed circuit board lines also degrade receiver performance. Multi-chip modules with controlled impedance packages reduce parasitics and losses but not power consumption and add significant cost. Furthermore, fixed-frequency discrete RF filters limit system flexibility in an open standard environment.

2.4 Image-Reject Mixing

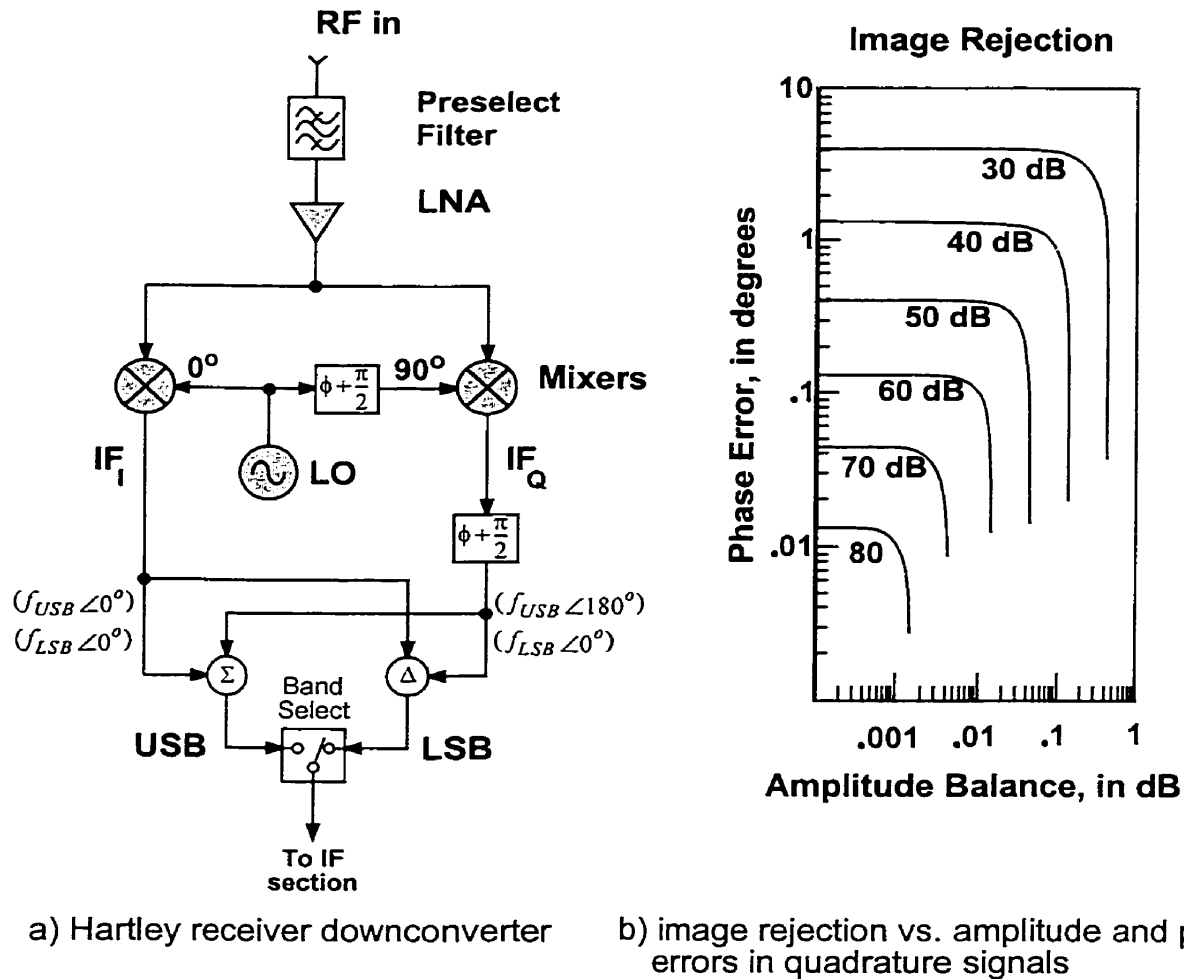


Figure 2.4: Image reject mixer topology and rejection.

An alternative frequency-conversion architecture which also rejects the image band at the IF is the Hartley image-reject mixer [15] illustrated in Figure 2.4a. Here, the RF input is split into two paths and downconverted by a quadrature (or 90° phase shifted) pair of LO signals into an IF_I (in-phase) and an IF_Q (quadrature) path.

The frequency conversion of the input RF to the IF_I path has already been expressed by equations 2.3 and 2.4. The signals which appear at the IF_Q node can also be determined in a similar way. In the quadrature path, the RF and LO multiplication can be expressed as,

$$A_m(t) \cos(2\pi f_{RF} t + \phi_m(t)) \cdot \sin(2\pi f_{LO} t) = \frac{A_m(t)}{2} [\sin(2\pi(f_{RF} + f_{LO})t + \phi_m(t)) + \sin(2\pi(f_{LO} - f_{RF})t - \phi_m(t))] \quad (2.6)$$

The upconversion term $(f_{RF} + f_{LO})$ can be dropped (as it is filtered out in the IF), and the IF_Q signal can be expressed for LSB RF signals as,

$$IF_Q(t) = \frac{A_m(t)}{2} \sin(2\pi(f_{LO} - f_{LSB})t - \phi_m(t)) \quad (2.7)$$

(where $f_{LSB} = f_{RF}$ for $f_{RF} < f_{LO}$). Since a sinusoid is an odd-symmetric function of time, RF signals above the frequency of the LO (i.e., f_{USB}), will appear in the IF with a polarity reversal,

$$IF_Q(t) = (-1) \frac{A_m(t)}{2} \sin(2\pi(f_{USB} - f_{LO})t + \phi_m(t)) \quad (2.8)$$

The $\frac{\pi}{2}$ phase shift block in the IF_Q path effectively converts the sine functions in equations 2.7 and 2.8 into cosine functions so that the USB and LSB signals in the I and Q paths will have the phase relations as noted in parentheses on Figure 2.4a. When the two IF paths are summed, the LSB signals are (ideally) anti-phase and cancel out leaving only the USB remaining in the IF output. When the difference element is selected however, the opposite occurs and (ideally) only LSB signals remain.

In practice there are many parasitic sources of error which can degrade the receiver's image-reject performance. Any gain or quadrature phase errors between the I and Q-LO signals or between the IF_I and IF_Q signal paths, degrades the rejection of the undesired sideband at the output. The image rejection obtained can be expressed in dB as,

$$IR(\theta_e, G) = -10 \log \left[\frac{1 - 2\sqrt{G} \cos(\theta_e) + G}{1 + 2\sqrt{G} \cos(\theta_e) + G} \right] \quad (2.9)$$

where θ_e is the overall phase error from quadrature and G is the total gain imbalance factor between the IF_I and IF_Q signals[16]. The amplitude imbalance in dB is related to the gain imbalance factor by

$$A = 10 \log G \quad (2.10)$$

Figure 2.4b shows a plot of the image rejection calculated as a function of the total phase and amplitude error. In order to achieve an image rejection on the order of 40-50dB (and thus eliminate the need for off-chip image filtering), a total system phase error of less than 1° is necessary (given an amplitude imbalance < 0.1 dB).

2.5 5-6 GHz Receiver Architecture

In a 5-6GHz integrated receiver application, the image-reject receiver topology is desirable as since it does away with the need for discrete filtering at the RF. This enables the use of a lower cost RF package and achieves a higher level of system integration. In order to use the image-reject mixing technique, a means of generating accurate on-chip quadrature LO signals in the 5-6GHz range is required. In this thesis, new circuit techniques are developed which provide an efficient means of generating low-noise quadrature LO signals on-chip from a lower-frequency external source or tank resonator. In order to verify the performance of these techniques, a 5-6GHz image-reject test receiver was fabricated in a silicon-bipolar technology with 0.5 micron minimum feature size and a unity gain frequency (f_T) of 25 GHz[17].

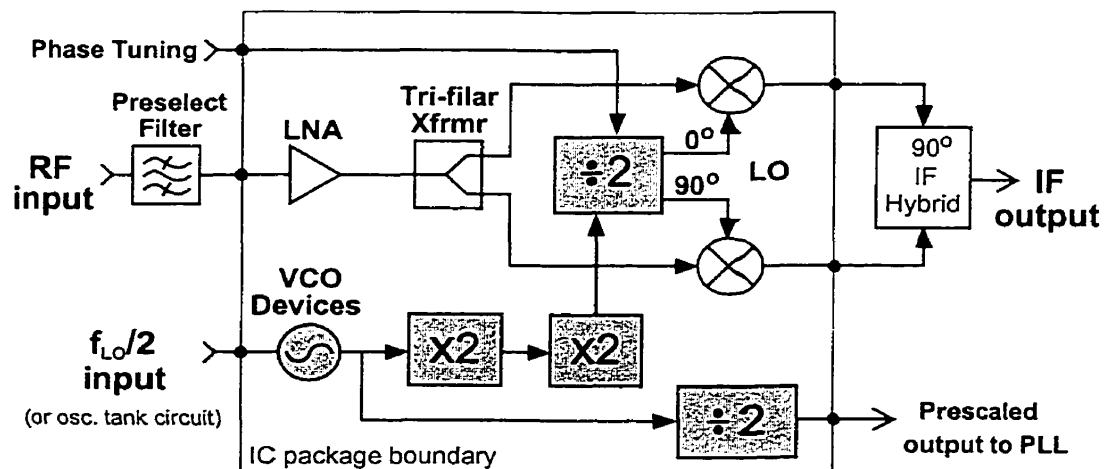


Figure 2.5: Receiver IC block diagram.

Figure 2.5 shows a block diagram of the test receiver IC and supporting circuitry. The circuits presented in this thesis are identified by the shaded blocks in the diagram and are

collectively referred to as the “LO system”. The LO system includes the active devices for a voltage-controlled oscillator (VCO), a cascaded pair of regenerative frequency-doubling stages, a regenerative quadrature divider with phase control, and an analog divide-by-2 prescaler. The image-reject receiver front-end (unshaded blocks in the IC) were first presented in [18].

2.5.1 Overview of the Receiver Front-End

Balanced differential circuitry is used throughout the IC to reduce signal injection into the substrate and to help reduce crosstalk by minimizing stray ground currents. This doubles the power consumption in many of the blocks compared to single-ended realizations and therefore low-voltage operation is emphasized throughout the IC.

Referring to Figure 2.5, the RF input signal first passes through an off-chip preselect filter and then enters the IC. Package parasitics at this transition are absorbed in the design of the LNA’s input matching network. An integrated three filament transformer is used to both split and couple the output of the LNA to the inputs of the I and Q mixers. The mixer LO ports are driven by a quadrature divide-by-2 stage in the LO system, and the converted outputs are taken off-chip and recombined in a discrete IF quadrature combiner (e.g., 90° hybrid).

Illustrated in Figure 2.6 is a schematic diagram of the test-receiver’s front-end designed by Long[19]. The LNA is formed by Q_1 and Q_2 and has emitter degeneration inductance L_{ee} to improve matching and linearity of the stage. A 4:1:1 turns-ratio integrated transformer, T_1 provides both impedance matching and differential coupling between the high impedance output of the LNA and the low impedance inputs of the mixer quads. Discrete off-chip transformer baluns are used to bias the collector nodes of the mixers and to impedance match the output to 50 ohms. The base-node inputs of the I and Q mixer-quad transistors (Q_3 - Q_6 and Q_7 - Q_{10}), are driven by quadrature LO signals generated by the LO system. The transformer allows for separate biasing of the LNA and mixers. The front-end can operate from a 0.9 V supply without significant performance degradation.

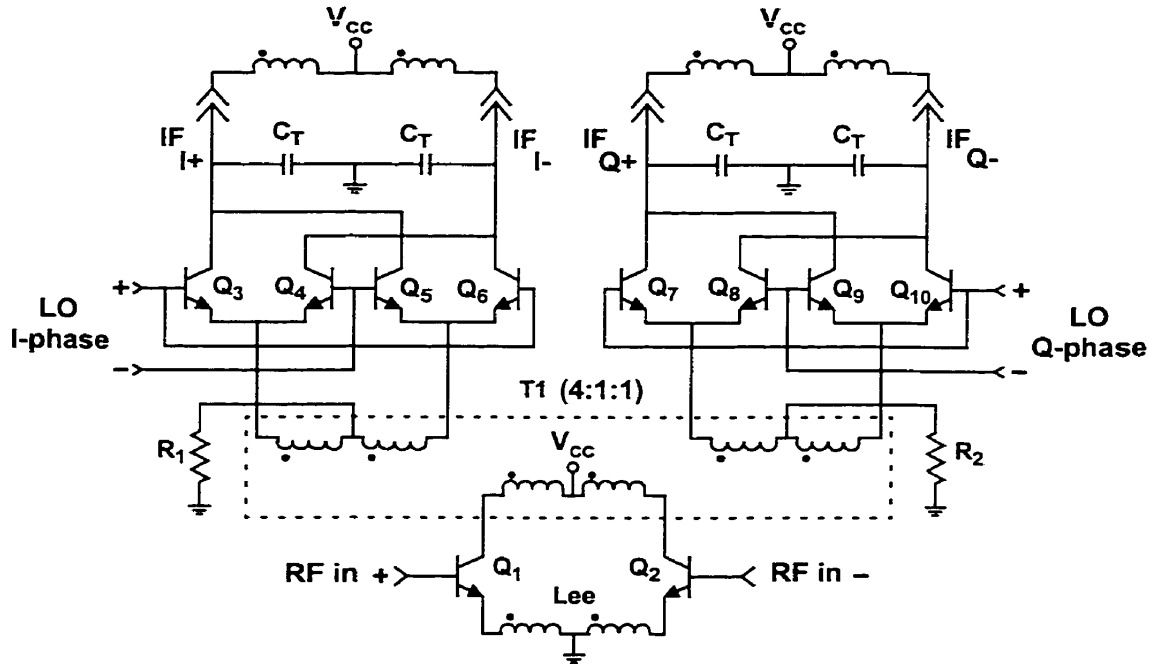


Figure 2.6: Internal schematic view of the receiver front-end.

2.6 LO System Overview

Referring again to Figure 2.5, the primary function of the LO system (identified by the shaded blocks), is to generate a low phase noise, accurate, quadrature LO pair of differential signals to drive the I and Q mixers. The external LO source is multiplied by a factor of four through a cascade of frequency doublers (“X2” stages) and then divided-by-two in order to generate an accurate quadrature pair of LO signals internally at twice the external source frequency. A divide-by-2 frequency prescaler is also included on the IC to allow easy compatibility with low-cost, sub-2GHz PLL synthesizer ICs.

In the image reject mixer architecture, the second 90° phase shift required at IF is one of the most difficult functions to realize. In the test setup for this receiver, this phase shift is carried out off-chip by a discrete component. Ideally this phase shift should be constant over the required bandwidth (which can be as wide as 50MHz in a 5GHz application), highly linear, and of relatively low loss. Although a digital implementation is possible, it is very advantageous to perform this function in the analog domain (preferably using passive

networks) so that any large interferers in the image band can be cancelled out prior to digitalization where spurious components can be generated in the IF. This significantly eases the linearity requirements for the receiver's A/D converter.

A systematic offset error (as small as 2°) in any part of the I-Q signal path will seriously degrade the overall image rejection (as observed in the curves of Figure 2.4b). One option is to cancel out any phase error at IF by providing an equal and opposite phase shift in the quadrature LO signals. Included in Figure 2.5, is a dc-input "phase control" line to the IC which provides a means for precisely adjusting the phases of the I and Q LO signals.

Also shown in the block diagram is an oscillator symbol labeled "VCO devices". The LO system is designed to allow either an external signal source or tank resonator to be used with the IC. A possible differential tank structure is illustrated in Figure 2.7.

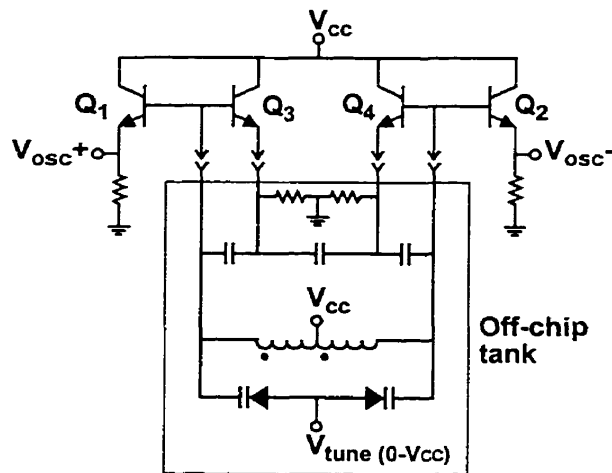


Figure 2.7: Oscillator tank resonator and feedback network

Using the active devices available on the IC and a minimum number of external components (found in the shaded region), a voltage-controlled Colpitts-type oscillator can be implemented [20].

2.7 IC Fabrication Technology Overview

Nortel's 25GHz f_T self-aligned double-poly silicon bipolar technology (NT25) was used for the test-chip implementation. The NT25 process has three layers of aluminum metallization with a 2 μm thick top metal, a 1 fF/ μm^2 capacitor dielectric layer, and polysilicon resistors. The NT25 design kit also includes fully-scalable HSPICE and Spectre RF simulation models as well as the corresponding device physical layouts.

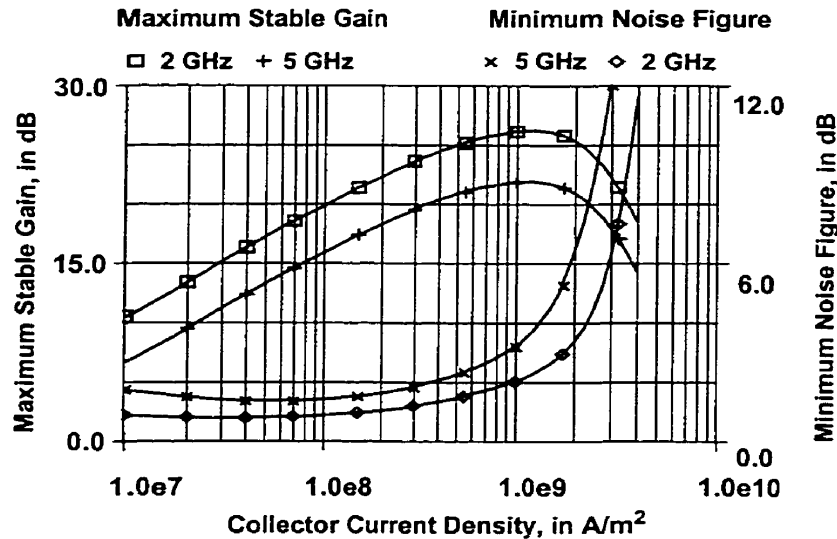
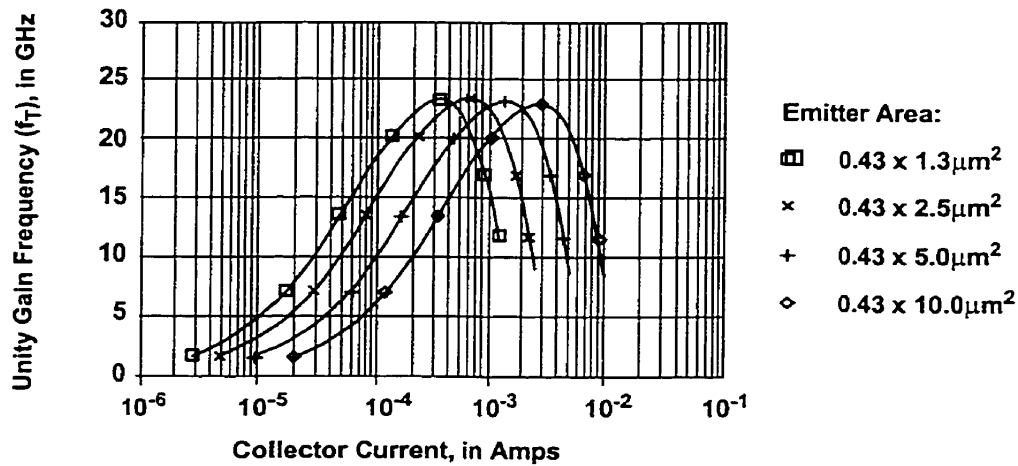


Figure 2.8: Small signal performance of a minimum-size NT25 device.

Shown in Figure 2.8 is the maximum stable gain and minimum noise figure for a $0.5\mu\text{m} \times 2.5\mu\text{m}$ emitter area device. The overall conversion gain targeted for the front-end of the receiver is 15dB, and it can be seen that at a collector current density of $3.5 \times 10^8 \text{ A}/\text{m}^2$, a 2dB noise figure(NF) and a maximum stable gain (G_{max}) of 20dB is achievable.

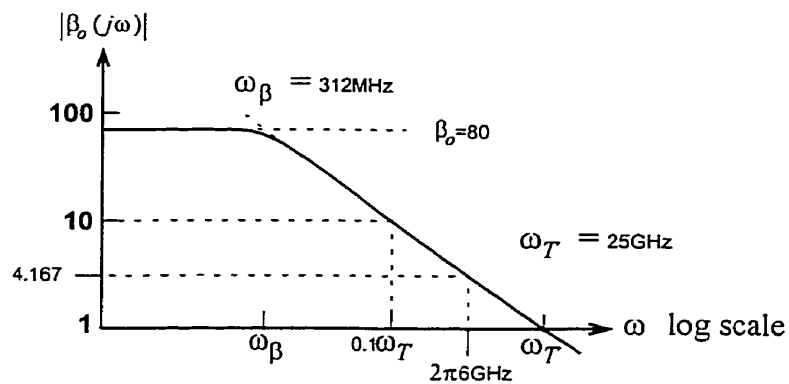
Figure 2.9 plots the unity current-gain frequency (f_T) as a function of the collector current for various transistor sizes[21]. From the above plotted data it can be seen for example, that a collector current of approximately 1.5mA is required for maximum f_T biasing of a $0.43 \times 5.0\mu\text{m}^2$ emitter area device.

f_T Versus I_C Characteristics for “nominal” BJT’s with $V_{CE} = 1V$ Figure 2.9: Unity gain frequency (f_T) versus I_C for a “nominal” device with $V_{CE} = 1V$.

The magnitude of the small-signal ac current gain of a bipolar transistor ($|\beta_o(j\omega)|$) above the cut-off frequency can be approximated as,

$$\omega_T = \omega_x |\beta_o(j\omega)| \quad (2.11)$$

where ω_T is the unity gain frequency of the transistor and ω_x is the operating frequency[22]. This relation is plotted in Figure 2.10 for a typical transistor available in the NT25 technology.

Figure 2.10: Magnitude of the small-signal ac current gain $|\beta_o(j\omega)|$ versus frequency

This implies that many of the devices must be biased near maximum f_T due to the low current gain available in the 5-6GHz range. Careful transistor bias optimization is required in order to keep power dissipation low.

2.8 LO System Operating/Design Requirements

Table 2.1 LO system design, target specifications.

Specification	Design Target
Minimum voltage	2V
Total IC power dissipation target	< 50mW
LO system power dissipation	< 25mW
Receiver operating range	5-6GHz
Intermediate frequency range	DC-500MHz
LO output frequency range (i.e., $f_{RF} \pm f_{IF}$)	4.5GHz-6.5GHz
Image Rejection Target	> 45 dB
LO quadrature phase accuracy	< 1°
LO I and Q amplitude balance	< 0.1 dB

Table 2.1 describes the overall requirements for the design of the LO system. A 2-volt supply is targeted in order to reduce power consumption in the receiver and to maintain compatibility with signal processing circuits that will likely be implemented in deep sub-micron CMOS technologies. A total power dissipation of less than 50mW is desired for the entire receiver, of which half is allocated to the LO system.

Although the front-end topology has been presented in the context of an image-reject architecture, it can just as easily be employed in a direct conversion design. In a direct conversion receiver, the RF is converted directly to baseband or zero-IF[23]. In this configuration, the LO system must be capable of operating over the entire 5-6GHz range. Furthermore, to maximize system flexibility, the IC should support the image-reject architecture with either high-side or low-side injection over the entire band without the need for switching sidebands half way. This implies that in order to support an IF of up to 500MHz, the operating range of the LO system must be at least 4.5-6.5GHz. A 500MHz IF capability is

targeted for the design. The motivation for supporting such a high first IF in an image-reject architecture is that if the 90° quadrature combiner is realized using a passive network, a higher IF reduces the fractional bandwidth ($\Delta f/f_{IF}$) over which the hybrid must maintain a constant 90° phase shift. This eases the design of the hybrid.

In order to eliminate the need for external image-band filtering, the receiver should achieve greater than 40dB of image rejection. An important design goal of the LO system is to minimize I-Q phase errors and to provide a high-resolution method of correcting phase error offsets which may exist in the IF_I and IF_Q paths.

In addition to these specifications, there are many other side goals for the design of the LO system. The phase noise of the external LO source to the IC should be the dominant source of noise seen by the inputs of the mixers. This will ensure that the implementation chosen does not degrade receiver performance. Furthermore, inductors are avoided in the LO system design to conserve chip area. Finally, a fully-differential signal path is needed to minimize the spurious coupling of unwanted harmonics to the substrate or the supply rails. This helps to maximize the isolation between the LO circuitry and the receiver front-end.

2.9 Quadrature Signal Generators

The main function of the LO system is the generation of a pair of quadrature LO signals. Generating a broadband 90° phase shift is relatively easy with passive networks however, keeping the amplitude constant at the same time is quite difficult. Three of the most popular circuit techniques used to generate I and Q signals are: quadrature oscillators[24], RC poly-phase filters[25], and frequency divide-by-2 circuits[26].

A quadrature LC oscillator, such as the one shown in Figure 2.11, uses a pair of coupled LC oscillators to generate accurate I and Q signals directly. In order to maintain an accurate quadrature output, the oscillator requires the use of closely matched integrated tank resonators which is difficult since mutual couplings between the inductors and surrounding circuitry can limit matching capabilities.

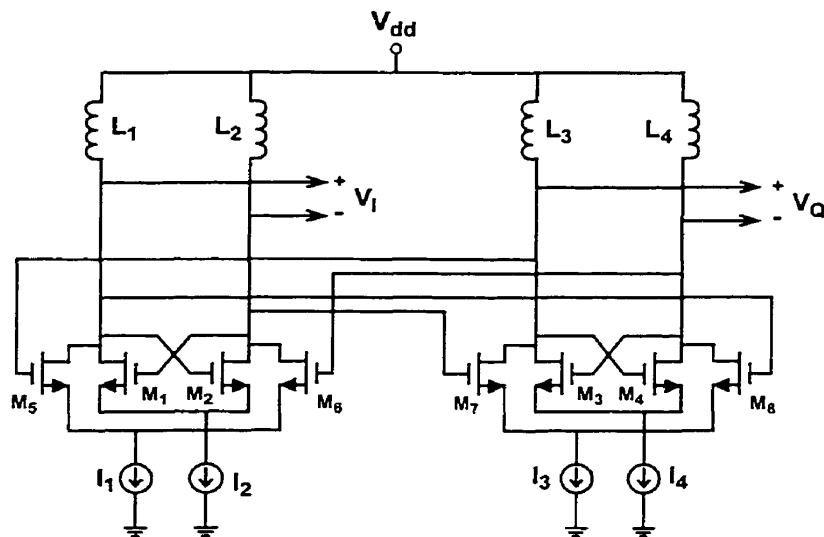


Figure 2.11: Typical CMOS quadrature LC oscillator[27].

Another characteristic of this circuit is that the phase noise of the signals generated are determined by the performance of the oscillator and so if high quality factor inductors are not available in an IC technology, then the phase noise of the LO signals will be degraded. The output frequency of the oscillator also needs to be controlled and thus the use of this circuit demands that supporting circuitry such as a phase locked loop (PLL) be included. In addition to these problems, the quadrature LC oscillator is also susceptible to multi-moding and mode hopping phenomenon.

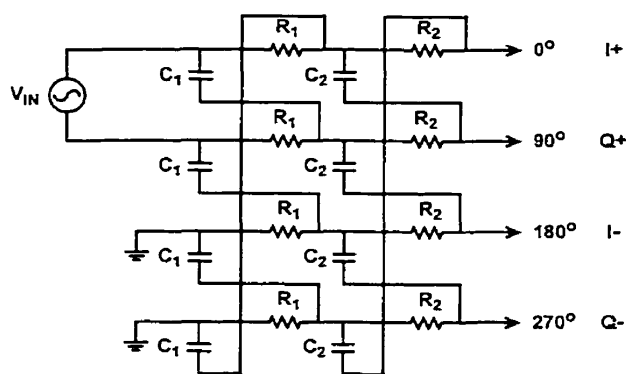


Figure 2.12: Polyphase filter (2-stage).

RC polyphase filters, by contrast, use high-order resistor-capacitor networks to generate quadrature-phased signals from a single phased input[25,28]. Although RC polyphase filters are capable of generating accurate I and Q signals over relatively wide bandwidths, they add attenuation, noise, and typically consume significant chip area[29]. The choice of using either a quadrature oscillator or a single-phased oscillator followed by polyphase filtering to generate quadrature LO signals in a receiver can depend on a number of design constraints such as power dissipation, die area costs, and phase noise requirements[30].

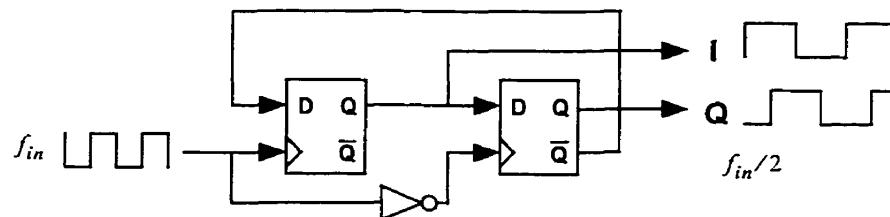


Figure 2.13: Digital divide-by-2, I-Q generator.

Frequency divide-by-2 circuits also generate accurate quadrature LO signals. They typically have a phase error of $< 1^\circ$ over their entire operating range and occupy an area significantly smaller than an equivalently wide-band, RC polyphase filter. Illustrated in Figure 2.13 is a simple digital divide-by-2 formed using a cascade of digital latches. One of the main drawbacks with this technique at high frequencies is that the input frequency (f_{in}) must be twice as high as that of the desired output frequency. Rather than attempt to generate this signal directly, a frequency doubling stage can be used in cascade with the divider to allow the I and Q signals to be effectively generated by an input signal of the same frequency.

In this thesis, frequency doubling followed by frequency division was chosen over the other methods of quadrature generation to allow an externally synthesized, low-phase noise source to be used with the IC, thus removing the need for an integrated quadrature VCO. Doubling techniques explored in later chapters enable frequency division beyond 12GHz, and so the use of an accurate I-Q divider precludes the use of a larger-area polyphase filter.

2.10 IC Compatible Methods of Frequency Doubling

Frequency doubling can provide significant system design flexibility in an RFIC. Unfortunately, with the quality factor of integrated inductors typically on the order of 15 or lower, traditional methods of using selective networks to extract a desired harmonic from a non-linear amplifier will, in most cases, have unacceptably poor performance in terms of both area requirements and power efficiency. The art of frequency doubling in microwave systems has almost always involved resonant circuits and so it is not surprising to find that there are very few RFIC-compatible frequency-doubling techniques currently in the literature. Some of the more promising candidates for use in a high-frequency (5-6GHz) application are presented below along with some of their associated drawbacks.

2.10.1 Frequency Multiplier Using Unbalanced Emitter-Coupled Pairs

Figure 2.14a shows a frequency-squaring circuit based on a modification of the popular Gilbert-cell mixer topology[31,32].

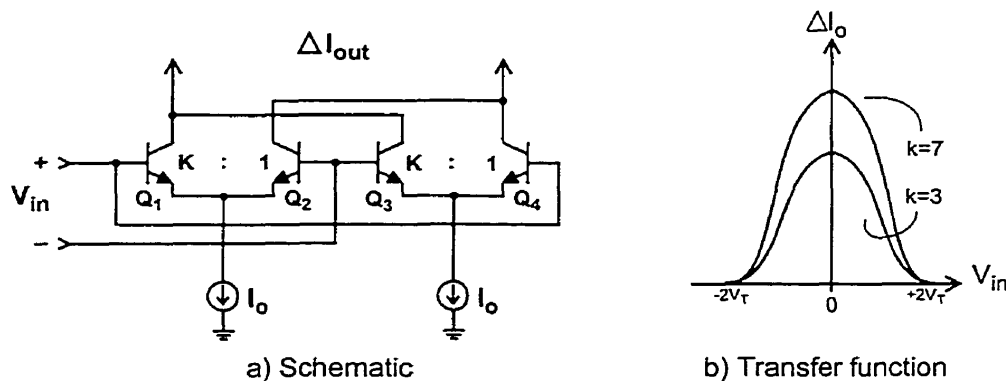


Figure 2.14: Scaled-emitter Gilbert quad multiplier.

The emitter-coupled transistor pairs of the quad (Q_1 - Q_2 and Q_3 - Q_4) have unbalanced emitter areas such that a differential output current (ΔI_{out}) will exist at the output of the circuit when the voltage across the input terminals (V_{in}) is zero. When the input voltage becomes large (approximately $> 2V_T$) however, the current flow through each half of the circuit becomes balanced and ΔI_{out} tends towards zero. In a frequency doubling application, emitter-

scaling factor (K) is chosen to maximize the second-order component of the transfer function illustrated in Figure 2.14b.

It can be shown that the differential output current is,

$$\Delta I_{out} = \alpha_F I_o \left\{ \tanh\left(\frac{V_{in} + V_K}{2V_T}\right) - \tanh\left(\frac{V_{in} - V_K}{2V_T}\right) \right\} \quad (2.12)$$

where $V_T = kT/q$ is the thermal voltage, α_F is the dc common-base current gain, I_o is the bias current, V_{in} is the input voltage, and V_K is the offset voltage defined as $V_K = V_T \ln K$, where K is the emitter-area scaling parameter[32].

This can then be simplified to,

$$\Delta I_{out} = \alpha_F I_o \ln K \left\{ 1 - \frac{1}{4V_T^2} V_{in}^2 - \frac{1}{12} (\ln K)^2 \right\} \dots, \quad (2.13)$$

indicating that the differential output current includes a component that is proportional to the square of the differential input voltage. Equation 2.2 also illustrates that the output signal (ΔI_{out}) has a natural dc offset for a zero volt input. This can be a serious problem in a balanced or fully-differential receiver design since the output current will tend to be slightly biased towards one polarity. Even if capacitive coupling is used to isolate the dc component of this stage from the next, the ac output impedance of the circuit will still be unbalanced due to the different transistor parasitics of the nominal-area devices (Q_2 and Q_4) compared to the scaled-area devices (Q_1 and Q_3). Such an effect is undesirable since it can degrade the symmetry of the receiver and increase the even-order harmonic distortion of subsequent RF stages.

2.10.2 Balun Transformer with Differential-Pair Doubler

Another frequency doubling technique[33] (shown in Figure 2.15) employs an integrated transformer balun to split the input into 0° and 180° phases and an active rectifying circuit to perform the multiplication. The positive going halves of each phase cause alternating conduction cycles in Q_1 and Q_2 at RF, which generate a rectified output (V_{out}).

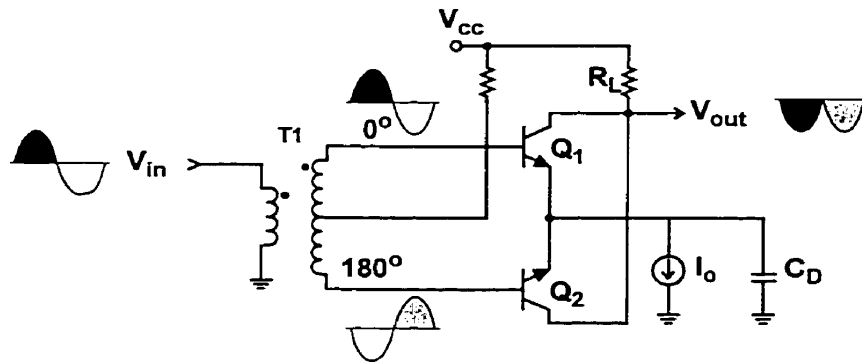


Figure 2.15: Transformer based frequency doubler.

The input signals to Q_1 and Q_2 are intended to be larger than approximately $2V_T$ to fully switch the transistors on and off, and the decoupling capacitor C_D (not necessarily an explicit component) prevents current steering from occurring at RF. This effectively causes the transistors to act as individual common-emitter (CE) amplifiers with a common load R_L such that the input is inverted and rectified to a single-ended output (V_{out}), resulting in a strong second-order component.

One of the major limitations of this circuit is the single-ended output is ground referred to the supplies and substrate. Employing this type of circuit runs counter to good differential RFIC design, since preventative measures are usually taken throughout the RF signal path to minimize the occurrence of ground loops and the injection of stray currents into the supplies or substrate. It is also difficult to convert a single-ended signal into a fully differential one at RF in an IC, since common-mode rejection of any kind is usually degraded by unwanted parasitic capacitance at key nodes such as the common-emitter node of a differential amplifier. An integrated transformer at the output of Q_1 and Q_2 might be more successful at rejecting common-mode signals, but it too loses its ability to generate a fully-differential output at increased frequencies due to parasitic effects between the input port and the inverting output terminal of the transformer[34].

In addition to the above stated concerns, the area penalty of implementing the integrated transformer (T_1) on an IC, for the purpose of realizing a frequency doubling circuit is difficult to justify in a low-cost, highly integrated receiver application.

2.10.3 An Emitter-Coupled Transistor Pair Frequency Doubler

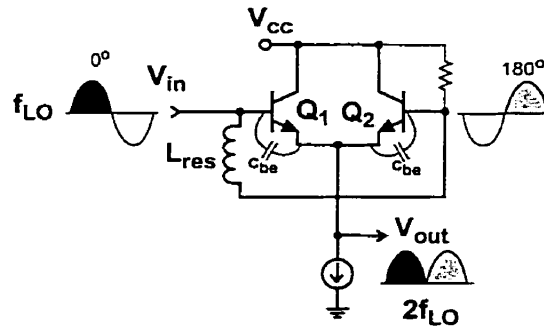


Figure 2.16: Resonator based frequency multiplier.

Figure 2.16 shows a circuit very similar to that of Figure 2.15 except the function of the transformer balun has been replaced with a simple LC-tank resonator (formed by L_{res} and $C_{be}/2$) [35]. With the input signal intended to be larger than approximately $2V_T$, Q_1 and Q_2 are alternately switched into conduction for each positive half-cycle of input as illustrated in the diagram. The transistor which is conducting will act as an emitter follower while the other transistor remains inactive (or reverse biased) thus generating a rectified signal at the emitter-coupled output node.

The fundamental harmonic (or input signal frequency) is typically undesired at the output of a doubler, and in this circuit it is suppressed by the 0° and 180° differential symmetry of the input voltage realized by the tuned LC tank.

One very desirable quality of this topology is that by having an emitter-coupled node as an output, this circuit has the same wideband properties as the emitter follower and can operate successfully to frequencies beyond $f_T/2$. In addition, third-order harmonics are suppressed by the differential symmetry of the circuit and thus with the added transistor parasitics at frequencies in excess of approximately $f_T/10$, the doubled frequency output is predominantly sinusoidal. Further filtering is typically not required and multiple stages can be easily cascaded.

Unfortunately, this technique also has a single-ended output and requires excessive area for an integrated inductor. Even if chip area is not a concern, the radiating electromagnetic fields and capacitive coupling of the input to the substrate by the inductor can cause

undesirable interference with other sensitive circuit blocks in a receiver such as the LNA or its bondwire matching network.

2.11 Summary of IC Frequency Doublers

A few of the more appropriate methods for frequency doubling in an RFIC have been presented along with some of their respective pros and cons. However, none of these techniques are suitable for generating a 10-12GHz differential signal on-chip using a 25 GHz f_T IC technology. As will be seen in later chapters, a frequency doubler with a fully-differential output is essential in order to obtain an accurate pair of quadrature signals from a frequency divider. To this end, a new regenerative method of frequency doubling, which is compatible with monolithic integration and which has a fully-differential output, is presented in subsequent chapters. The fundamental operation of this new doubler is based on the concept of an injection locked ring oscillator, which is the topic of the next chapter.

CHAPTER

3

Injection Locked Ring Oscillators

There is a renewed interest in some reviving RF techniques and topologies of the past, such as: direct conversion, polyphase filtering, first order frequency synthesis and injection locking to increase the level of functional integration on an RFIC.

In this chapter, a resistively-loaded injection-locked ring oscillator (ILRO) is examined. A Simulink model of the system is also developed and validated through comparisons with HSPICE simulations. This model is then used to provide insight into the fundamental characteristics of the ILRO. Finally, some current and historical uses for simple injection locked oscillators are also briefly mentioned. In later chapters, ILRO based circuits and their characteristics are exploited to perform very useful LO signal processing functions.

3.1 Injection Locking of Oscillators

Injection locking is the process by which a free-running oscillator is synchronized in frequency and phase to an external source. This effect has been observed in many oscillating systems and was first noticed by Huygens in the synchronization of mechanical pendulums[36]. One useful property of an injection locked oscillator is that the phase noise properties of the injecting source are preserved by the locked oscillator because it is locked in phase to the external signal. Thus, if an oscillator with poor free-running phase noise characteristics is locked to a high quality (low-phase noise) source, the phase noise of the locked oscillator is also low.

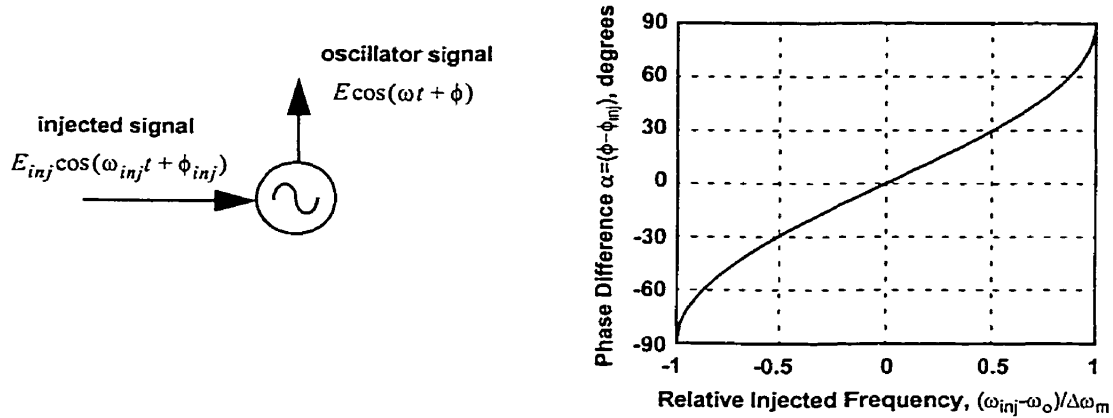


Figure 3.1: Phase of an injection locked oscillator versus the relative injected frequency[37].

For a single tuned oscillator model, it can be shown that the phase of an injection locked oscillator is described by Adler's equation,

$$\frac{d\alpha}{dt} = \omega_o - \omega_{inj} - \underbrace{\frac{E_{inj} \omega_o}{E 2Q}}_{\Delta\omega_m} \sin(\alpha) \quad (3.1)$$

where ω_{inj} is the injected signal frequency, ω_o is the free-running frequency of the “undisturbed” oscillator, Q is the quality factor of the oscillator's resonator, and E_{inj}/E is the ratio of the injected signal amplitude to the oscillator's amplitude[38]. The remaining variables are defined in Figure 3.1, where ω is the instantaneous frequency of the oscillator and α is the phase relation between the oscillator and the injected signal (i.e., $\alpha = \phi_{inj} - \phi$). For a more complete explanation and a full derivation of Adler's equation, see Appendix A.

Using Adler's equation, an oscillator is said to be locked or synchronized to the injected signal if a steady-state solution can be found for the phase such that $d\alpha/dt = 0$. Solving (3.1) for steady-state phase gives,

$$\alpha = \sin^{-1} \left(\frac{\omega_{inj} - \omega_o}{\Delta\omega_m} \right) \quad (3.2)$$

Thus, a solution exists when the injected signal frequency lies within the range,

$$\omega_{inj} = \omega_o \pm \Delta\omega_m \quad (3.3)$$

$\Delta\omega_m$ is often referred to as the “locking range” of the oscillator (even though it only physically represents half the lock range), and although there are always two solutions for α in equation 3.2, a stability analysis can be used determine which of the solutions is physically realizable. Since only one unique solution to equation 3.2 exists, it can be shown (section II of [38]) that the phase difference between the oscillator and the injected source (α) is restricted to,

$$-\frac{\pi}{2} \leq \alpha \leq \frac{\pi}{2}, \text{ for } \alpha \text{ in radians.} \quad (3.4)$$

This phase difference as a function of the relative injected signal frequency (i.e., equation 3.2), is plotted in Figure 3.1. Two key observations from this plot are: firstly, that if the oscillator is locked at its free-running frequency, there is no phase shift between the injected signal and the locked oscillator, and secondly that as the locked oscillator’s frequency approaches the edge of it’s locking range, the phase shift between the injected signal and the oscillator approaches $\pm 90^\circ$. This is the angle at which the oscillator can no longer be injection locked, and beyond which the oscillator runs freely.

The upper and lower ends of the locking range are referred to as the “locking boundary” frequencies, and are defined as the frequencies beyond which the oscillator cannot remain synchronized to the injected source over an indefinite period of time. The symptoms of an unlocked oscillator near the boundary frequency are easily identified in the lab or in transient simulation. Typically, at the threshold frequency where the oscillator cannot maintain lock, the output is severely amplitude modulated by a low beating frequency and can be observed to slip in and out of lock periodically. The oscillator’s output frequency in this condition appears to chirp between the injected signal’s frequency and somewhere near it’s free-running frequency during each beat cycle. An interesting mechanical model to help visualize the cause of this phenomenon is described in[38].

Due to the unique mechanism of oscillator synchronization, most injection-locked oscillators (ILOs) share a number of characteristics. Shown in Figure 3.2a, is a simple block diagram of an ILO (taken from Appendix A).

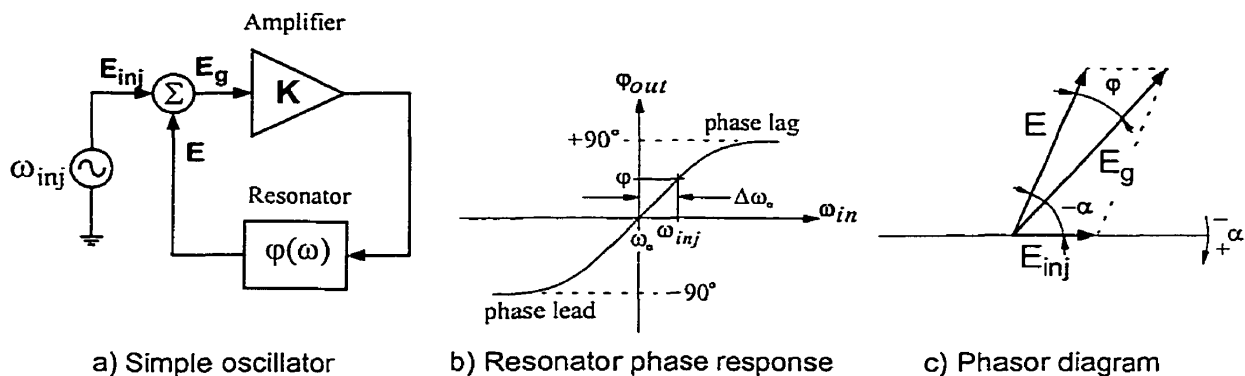


Figure 3.2: Injection locked oscillator model.

The necessary condition required to injection-lock the oscillator can be derived from equation 3.1 by setting

$$\frac{d\alpha}{dt} = 0, \quad (3.5)$$

and noting that,

$$-1 < \sin(\alpha) < 1. \quad (3.6)$$

This gives

$$\frac{E_{inj}}{E} > 2Q \left| \frac{\Delta\omega_o}{\omega_o} \right|, \quad (3.7)$$

where $\Delta\omega_o$ is the difference between the frequency of the injected signal (ω_{inj}) and the free-running frequency (ω_o). Figure 3.2b illustrates the phase to frequency response of the single LC section resonator.

From equation 3.7, for a given level of injected signal drive E_{inj} , we see that an ILO will have a finite band of frequencies ($\Delta\omega_o$) centered around the free-running frequency ω_o , over which it is able to become locked. The ratio of $\frac{\Delta\omega_o}{\omega_o}$ is defined as the relative locking bandwidth of the oscillator and is typically expressed as a percentage. The relative locking bandwidth is directly proportional to the ratio $\frac{E_{inj}}{E}$, and inversely proportional to the Q of the

oscillator. This implies that an infinitesimally small level of injected signal is required to lock the oscillator at its free-running frequency ($\omega_{inj}=\omega_o$), and that very high-Q oscillators cannot be locked over a wide frequency range without a large injection amplitude, E_{inj} .

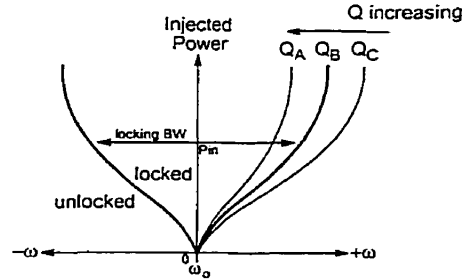


Figure 3.3: Typical locking range of an ILO.

The typical locking characteristic of an ILO as a function of injected power is plotted in Figure 3.3 for illustration. The steady state phase relationship between the injected signal and the oscillator is depicted in Figure 3.2c and is expressed as,

$$\sin \alpha = 2Q \frac{E}{E_1} \left(\frac{\Delta \omega_o}{\omega_o} \right), \quad (3.8)$$

from equation 3.1 with $d\alpha/dt = 0$.

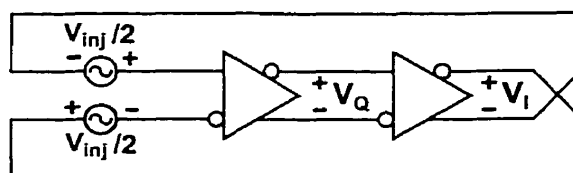
3.2 Simulink Modeling

Some of the injection-locked oscillators employed in this thesis operate at beyond 5GHz and hand calculations quickly become inaccurate and far too tedious to achieve an exact solution as a result of the complicated parasitics. Transient simulations of a simple differential-pair amplifier operating at 5.5GHz (or $\sim f_T/5$), confirm that the higher-order (small-signal) poles of the amplifier shift with quiescent point, device geometry, signal amplitude, input frequency, and harmonic levels of the input signal. To simplify the analysis, a low-frequency (~ 1 GHz) version of the oscillators that are employed in this thesis are modeled in this chapter, and serve as a tool to provide insight into the characteristics and the general behaviour of a resistively-loaded, injection-locked ring oscillator running at 5-6GHz.

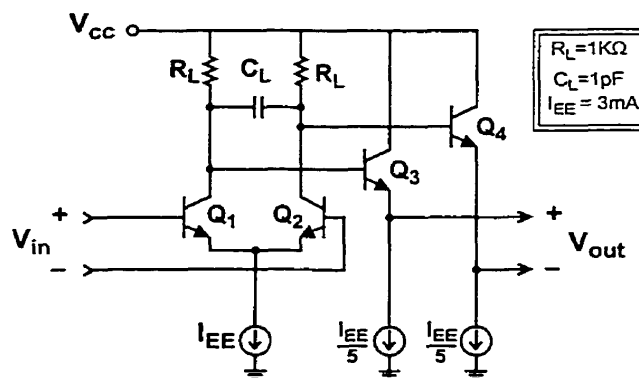
Understanding the underlying mechanics of the simplified ILRO allow the simulated behaviour of more complicated (and higher frequency) ILROs to be understood, designed and optimized directly using HSPICE computer simulations without the need to calculate or model the poles and zeros of the circuit explicitly by hand.

3.3 Injection-Locked Ring Oscillators

In this section, fundamental mode injection-locking of a quadrature (2-stage) ring oscillator with resistive loads is studied, and an appropriate (simulink) model explaining its operation and characteristics is compared with simulated (HSPICE) results.



a) Block diagram showing ideal injected signal summation



b) Differential amplifier realization

Figure 3.4: Injection locked ring oscillator topology.

Figure 3.4a illustrates a block diagram of a 2-stage differential ring oscillator with a differential injection source placed in series with the feedback path, where the differential amplifiers in the oscillator are shown schematically in Figure 3.4b. In order to simplify the analysis, the R_L - C_L load of Q_1 and Q_2 is selected to dominate the collector node parasitics and

emitter followers Q_3 and Q_4 are employed to reduce the effect of loading from the next stage. The differential output current for the emitter-coupled transistor pair Q_1 and Q_2 of Figure 3.4b can be expressed as[22],

$$I_{od} = \alpha_F \frac{I_{EE}}{2} \cdot \tanh\left(\frac{-v_{id}}{nV_T}\right), \quad (3.9)$$

where α_F is the dc common-base current gain, $v_{id} = v_{inj}$ of Figure 3.4b, I_{od} is the differential output current across the collectors, n is an ideality factor (which depends on process parameters), and $V_T = kT/q$ is the thermal voltage of the transistors.

The large signal characteristic of a differential-pair of $0.5 \times 10\mu\text{m}^2$ emitter-area devices simulated in HSPICE (at $I_{EE} = 3\text{mA}$) matches equation 3.9 for $n = 1.51$, and $\alpha = 0.98$. R_L and C_L for this model are selected to set the free-running frequency of the oscillator to approximately 1GHz (i.e. to $f_T/25$) so that the transistor gain is high and parasitic effects of the transistors can, for the most part, be neglected. Using the component parameters listed in the figure, the dominant pole of the amplifying stage is approximately,

$$f_{p1} = \frac{1}{2\pi \cdot 2k\Omega \cdot 1pF} = 79.6\text{MHz}. \quad (3.10)$$

The Barkhausen criteria for oscillation requires that the two amplifying stages in the oscillator contribute a total of 180° of phase shift at the oscillation frequency[39]; another 180° is provided by the cross-coupled feedback connection of the ring. This means that each amplifying stage will provide 90° of phase shift at the free-running frequency.

A simple first-order (low-pass) approximation of each stage is insufficient to determine the free-running frequency of the oscillator (ω_o) since the phase shift of a first order network is given by,

$$\tan^{-1}\left(\frac{\omega}{\omega_{p1}}\right) = \theta_{p1}, \quad (3.11)$$

which can only approach 90° for angular frequencies $\omega \gg \omega_{p1}$ but never reach or surpass it. A two-pole model for each amplifying stage is therefore needed to account for higher-order transistor effects, in which case restating the Barkhausen criteria gives,

$$\theta_{p1} + \theta_{p2} = 90^\circ \Big|_{\omega = \omega_o} \tag{3.12}$$

Transient HSPICE simulations of the oscillator in Figure 3.4 dictate the free-running frequency to be 898 MHz at an amplitude of 340 mV-pk. An equivalent second pole can be determined from equations 3.10, 3.11 and 3.12, such that at 898 MHz, a 90° phase shift through the two-pole amplifier realized. For $f_{p1}=79.6\text{MHz}$, the second equivalent pole frequency is determined to be $f_{p2}=10.13\text{GHz}$.

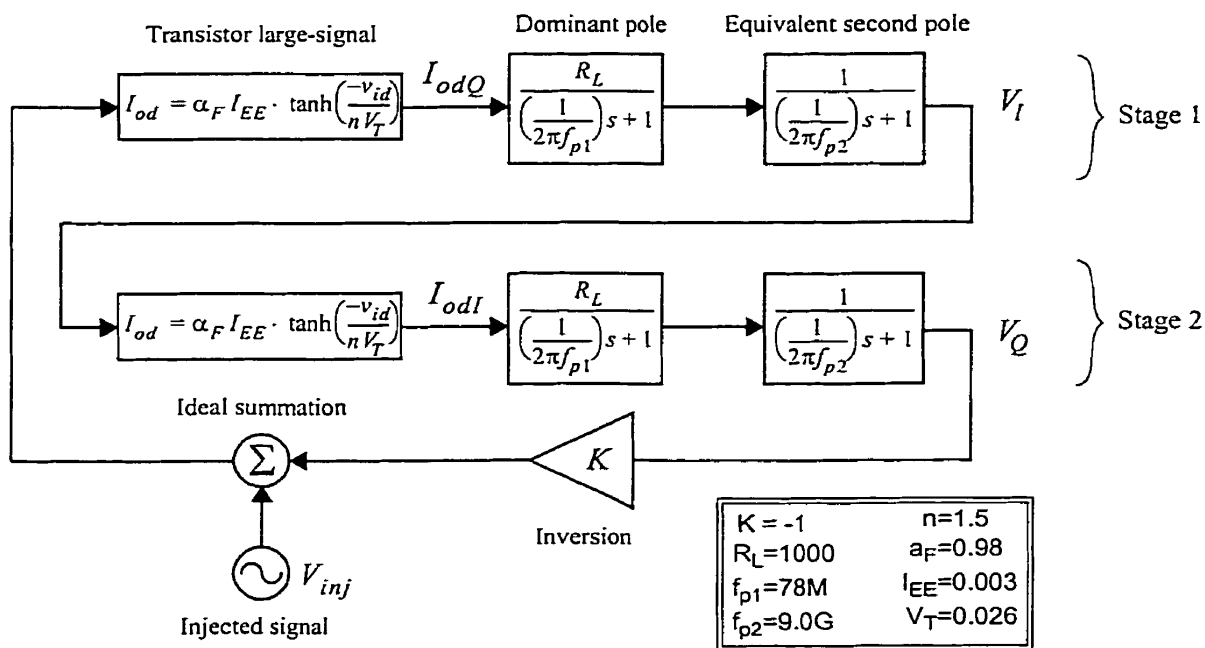


Figure 3.5: Simulink model of the ring oscillator in Figure 3.4.

A Simulink model of the ring oscillator having the topology of Figure 3.4a with the modeled amplifiers of Figure 3.4b is shown in Figure 3.5 along with its associated parameters. In this oscillator model there are two critical variables (f_{p1} and f_{p2}) available for tweaking. There are also two optimization goals: the oscillator’s free-running frequency and output amplitude. HSPICE predicts that the circuit should have a free-running frequency of

$f_{osc}=898\text{MHz}$ and an oscillator amplitude of $A_{osc}=340\text{mVp}$. The original calculations of $f_{p1}=79.6\text{MHz}$ and $f_{p2}=10.13\text{GHz}$ result in $f_{osc}=959\text{MHz}$ and $A_{osc}=295\text{mVp}$ in the Simulink model. This represents a +3.3% frequency error and -1.2dB amplitude error compared to HSPICE. The amplitude of the oscillator is expected to decrease with increasing frequency, as will be discussed shortly, and so the polarity of the amplitude error is found to be consistent with the frequency error. A possible explanation for this positive frequency shift might be that the higher-order frequency components generated by the \tanh function of the transistor large-signal equation, although small, have a non-negligible effect on the zero-crossing of v_{id} , leading to an unexpected phase shift at the oscillator's fundamental frequency.

Manual optimization of the pole frequencies in the Simulink model to $f_{p1}=78\text{MHz}$ and $f_{p2}=9.0\text{GHz}$ achieves $< 0.3\%$ frequency and amplitude error compared to HSPICE simulations of the oscillator in the free-running condition.

3.3.1 Simulink Model versus HSPICE Simulation

Two critical measurements of an injection locked oscillator are the output amplitude as a function of frequency and the locking range as a function of injected signal level. The output amplitude is measured differentially across the quadrature (V_Q) nodes (as labeled in Figure 3.4a).

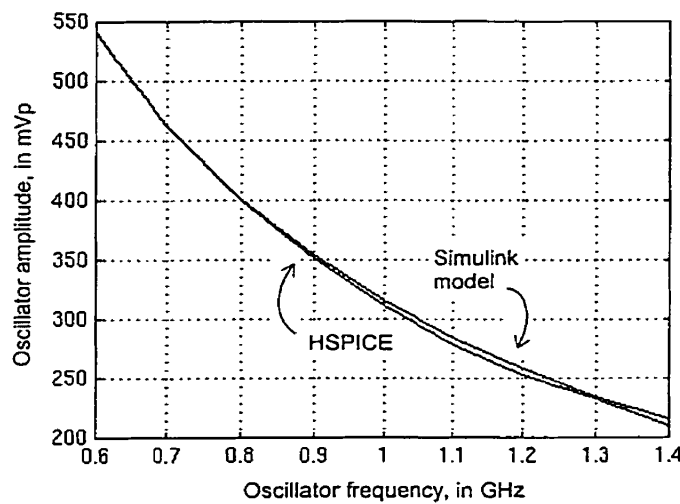


Figure 3.6: Oscillator Amplitude - HSPICE vs. Simulink.

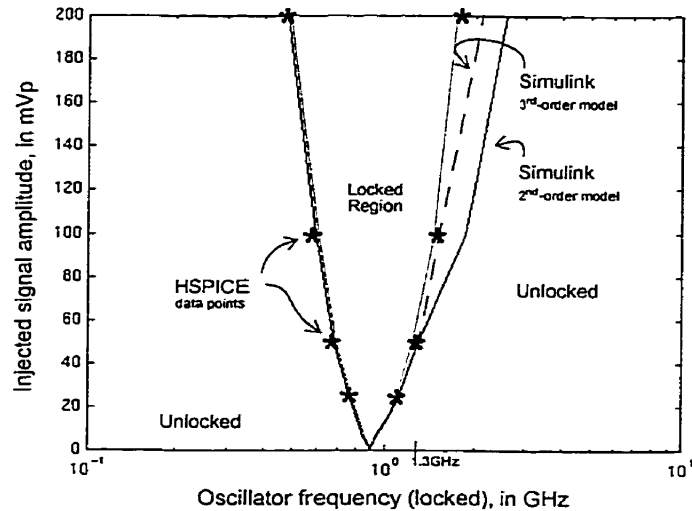


Figure 3.7: Locking range - HSPICE vs. Simulink.

Figures 3.6 and 3.7 show the output amplitude and locking range as a function of frequency for both the HSPICE simulations and the Simulink model. Both are in very close agreement for locking frequencies below 1.3GHz (with a 50mVp injection level). It should be noted that the output amplitude of the simulink model is strongly independent of the injection amplitude.

With the injection level increased to 100mVp, the Simulink model predicts that the upper bound of the locking range is 1.8GHz. HSPICE simulations, however, show an unusual phenomenon above 1.5GHz, whereby the fundamental locking mode of the oscillator is lost and the oscillator begins to act as a frequency halver (or divide-by-2 circuit). In transient simulations, the oscillator's synchronization was observed to slip with respect to the input on every second cycle of the input signal's phase. As a result the oscillator's output frequency was half that of the input signal.

It was hypothesized that this phenomenon might be influenced by the higher-order poles of the active devices in the HSPICE simulation which are not being accounted for in the Simulink two-pole amplifier models. A third pole was introduced into each amplifying half of the oscillator (Figure 3.8) to attempt to validate this hypothesis.

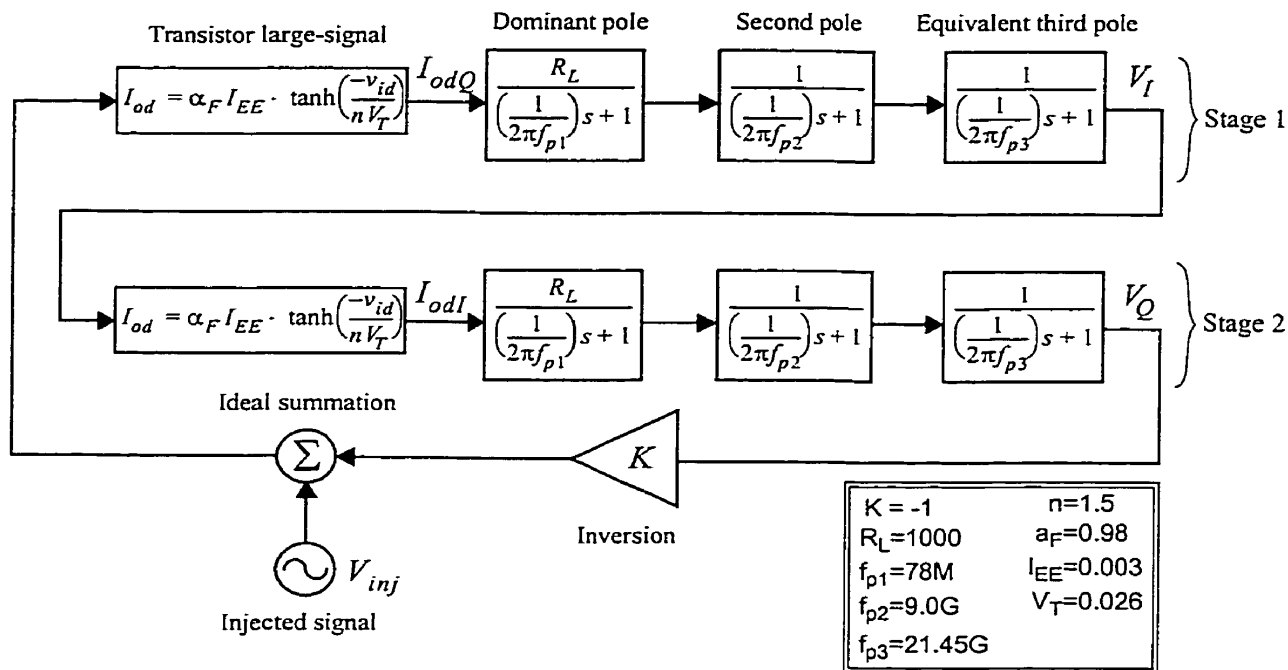


Figure 3.8: An ILRO model using a three-pole amplifier model.

Simulink simulations indeed verified that the frequency halving effect at frequencies above 1.5GHz in HSPICE are captured accurately by introducing a third pole into the model at an empirically determined frequency of $f_{p3} = 21.45\text{GHz}$. Figure 3.7 includes a curve showing the improved correlation between the locking range obtained by the third-order simulink model and the HSPICE simulated results.

Increasing the injection level further still, to 200mVp, causes the oscillator to be able to remain locked at even higher frequencies. Under this condition, the third-order Simulink model now predicts that the frequency-halving effect occurs at 1.8GHz. HSPICE simulation however, shows halving to occur at a (higher) frequency of 2.2GHz. Although only two poles are required to characterize the lower end of the frequency locking range, an increasing number of poles (and zeros) are found required to model the system at the upper end of the locking range. This suggests device parasitics begin to strongly influence the oscillator's behaviour at higher frequencies, and that at the low frequency end these higher-order effects can be neglected.

3.4 ILRO Model Observations

There are some basic observations that can be made directly from the simple two-pole Simulink model. The output amplitude, for example, is dominated by the low frequency pole of the load (f_{pl}). An injection-locked ring oscillator having RC loads will therefore have an amplitude vs. frequency curve that follows a first-order (-6dB per octave) response.

Shown in Figure 3.9 is the phase response the two-pole amplifier model used in the simulink simulation. According to the Barkhausen criteria, the free-running frequency of the oscillator is expected to occur where the phase shift in each stage is -90° , and for the two pole system, this occurs at the logarithmic center of the two poles,

$$\omega_o = \sqrt{\omega_{p1}\omega_{p2}} \quad (3.13)$$

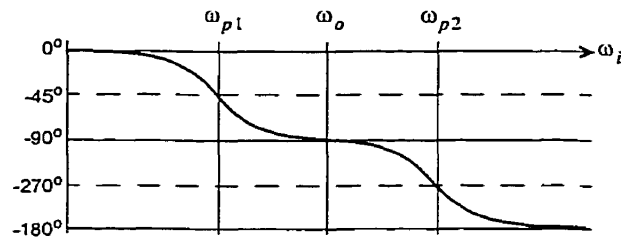


Figure 3.9: Differential amplifier phase shift.

Figure 3.9 also shows that between ω_{p1} and ω_{p2} , the slope of the phase response is a minimum at ω_o , which implies that a small phase change causes a larger change in the frequency of oscillation. This translates to a wide locking range according to equation 3.7.

The slope of the phase response (for both amplifier stages) at the free-running frequency can be determined using

$$\phi(\omega) = -2 \tan^{-1}\left(\frac{\omega}{\omega_{p1}}\right) - 2 \tan^{-1}\left(\frac{\omega}{\omega_{p2}}\right) \quad (3.14)$$

and

$$A = \left. \frac{d\phi}{d\omega} \right|_{\omega = \omega_o} = -\frac{2/\omega_{p1}}{1 + \left(\frac{\omega_o}{\omega_{p1}}\right)^2} - \frac{2/\omega_{p2}}{1 + \left(\frac{\omega_o}{\omega_{p2}}\right)^2} . \quad (3.15)$$

Combining equations 3.13 and 3.15, and by letting

$$k = \omega_{p2}/\omega_{p1} , \quad (3.16)$$

gives

$$A = \frac{-4\sqrt{k}}{1+k} \cdot \frac{1}{\omega_o} , \quad (3.17)$$

or

$$A \cong \frac{-4}{\omega_o\sqrt{k}} , \text{ for } k \gg 1. \quad (3.18)$$

For comparison with the general definition of the Q-factor of an RLC tank based oscillator, we can say that the Q-factor of a 2-stage RC ring oscillator can be approximated as,

$$Q_{RC} \cong \frac{2}{\sqrt{k}} \quad (\text{for } k \gg 1) , \quad (3.19)$$

(from equation A.10c of Appendix A). Using equation 3.19, the effective Q-factor for the oscillator model of Figure 3.5 is therefore approximately 0.2. This extremely low Q-factor enables a very wide locking range for the oscillator.

From the observations made above, it follows that raising the dominant pole frequency will raise both ω_o (i.e., the center of the frequency locking range), and the output amplitude. A consequence of placing the two poles closer together is that (along with decreasing k) the slope of the phase curve at ω_o becomes steeper and effectively decreases the locking range of the oscillator (for a given input signal amplitude).

3.4.1 Estimating the Injection Locking Range

The final step required to make this analysis complete is to verify the locking range formulas (presented earlier in this chapter) to the model. Substituting either (3.18) into (A.13c) or equivalently (3.19) into (3.7) yields the necessary condition for locking as

$$\frac{E_{inj}}{E} > \frac{4}{\sqrt{k}} \left| \frac{\Delta\omega_o}{\omega_o} \right|. \quad (3.20)$$

The only parameter which remains to be determined is the oscillation amplitude (E). In order to further simplify calculations, the \tanh function of equation 3.9, which describes the differential output current of the emitter-coupled transistors (Q_1 and Q_2), will be approximated by the signum function

$$I_{od} = \begin{cases} +\alpha_F \frac{I_{EE}}{2} & , (v_{id} > 0) \\ -\alpha_F \frac{I_{EE}}{2} & , (v_{id} < 0) \end{cases}. \quad (3.21)$$

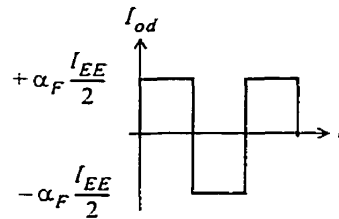


Figure 3.10: Graphical representation of equation 3.21.

The fundamental frequency component of a unity square wave signal, as depicted in Figure 3.10, from Fourier analysis has an amplitude of $\frac{4}{\pi}$, thus amplitude of the fundamental frequency component of I_{od} can be approximated as

$$I_{od}' = \frac{2\alpha_F I_{EE}}{\pi}. \quad (3.22)$$

Using equation 3.22, the differential output voltage (taken as $V_I = E$) can then be expressed as a function of the injection-locked oscillation frequency, ω_{inj} as

$$E = \frac{\left(\frac{2\alpha_F I_{EE}}{\pi}\right) \cdot 2R_L}{\sqrt{1 + \left(\frac{\omega_{inj}}{\omega_{p1}}\right)^2}}. \quad (3.23)$$

In equation 3.23, we have neglected the effect of the second-pole on the oscillator's output amplitude since f_{p2} is approximately a decade beyond the operating frequency of the oscillator.

Assuming $\omega_{inj} \gg \omega_{p1}$ and substituting,

$$K_o = \frac{4}{\pi} \alpha_F I_{EE} R_L. \quad (3.24)$$

results in

$$E = \frac{K_o \omega_{p1}}{\omega_{inj}}. \quad (3.25)$$

Evaluating equation 3.25 for the oscillator's amplitude at the free-running frequency ω_0 using $\omega_{p1} = 2\pi(79.6\text{MHz})$ results in $E = 332\text{mV}_p$ which is close to the 340mV simulated result given by HSPICE.

Finally, to calculate the locking range of the oscillator, equations 3.13, 3.16 and 3.25 can be substituted into equation 3.20 to obtain the lower and upper frequency locking boundaries as,

$$\omega_L = \frac{\omega_o}{1 + (E_1/E_o)}, \quad (3.26)$$

and,

$$\omega_H = \frac{\omega_o}{1 - (E_1/E_o)}, \quad (3.27)$$

where,

$$E_o = \frac{4K_o}{k}. \quad (3.28)$$

Table 3.1 Comparison of the Locking Boundaries for $E_{inj} = 50mV\text{-}\rho k$ Injection.

Calculation Method	Lower Frequency Locking Boundary	Upper Frequency Locking Boundary
HSPICE	670MHz (466mVp)	1270MHz (231mVp)
Simulink $f_{p1} = 78\text{MHz}$ and $f_{p2} = 9.0\text{GHz}$	670MHz (477mVp)	1325MHz (222mVp)
Equations 3.26 and 3.27 with (3.25); using original pole frequency values: $f_{p1} = 79.6\text{MHz}$ and $f_{p2} = 10.13\text{GHz}$	630MHz (473mVp)	1562MHz (191mVp)
Oscillator amplitude predicted by Equation 3.25 for 670 and 1270MHz.	445mVp @ 670MHz	235mVp @ 1270MHz

Table 3.1 compares the locking range and output amplitudes predicted by HSPICE, Simulink, and hand analysis. The Simulink upper and lower locking boundary frequencies agree well with HSPICE, as do the predicted oscillator amplitudes at those frequencies (in parentheses). Substitution of the original hand-calculated pole frequencies for f_{p1} and f_{p2} into equations 3.25, 3.26, and 3.27 resulted in hand-calculated boundary frequencies and oscillator amplitudes which also agreed reasonably well with HSPICE simulations. It should be noted however, that the hand calculated solution cannot be expected to agree with HSPICE as well as the Simulink model did mainly due to the approximations made in equations 3.21 and 3.22.

3.4.2 Some ILO Applications

ILOs (not of the ring-type) have been exploited in the past to perform many RF functions; particularly at microwave and optical frequencies. An LO phase shifter can be realized by injection locking a voltage controlled oscillator (VCO) to an input LO source[37]. As the center or free-running frequency of the VCO is adjusted by an input d.c. control voltage, the phase shift between the fixed-frequency input LO signal and the locked oscillator will vary. Although the range of phase shift possible is limited to less than 90° by equation 3.8, the main advantage of the circuit is that it can be employed very efficiently at nearly any frequency where a VCO can be realized. At baseband, where digital signal processing is readily

available, this solution is less attractive, however, in a Tera-Hertz or optical application, one might consider this to be a very high-end solution.

Microwave and optical communications systems commonly use injection-locking techniques to stabilize high power lasers (or oscillators) to precise low-power frequency references. With proper design, the high power output tracks the phase noise of the precision frequency source, usually improving clock jitter performance.

In this thesis, injection-locked ring oscillators are used to multiply, divide, and phase-shift LO signals in an efficient manner and at a high fraction of the unity gain frequency of the active devices employed. In the next chapter, an ILRO is used as the basis for a new high-performance frequency-doubling technique which is central to the LO system design.

CHAPTER

4

Regenerative Frequency Doubling

In this chapter, the fundamental characteristics of an injection-locked ring oscillator (ILRO) are exploited with a new ILRO based frequency-doubling technique. The basic concept is presented, followed by a mathematical analysis of the signal doubling mechanism itself. The fundamental properties and characteristics of the regenerative doubler are then discussed in the context of the ILRO core. Finally, variations of the regenerative doubler are presented which offer some interesting functions beyond frequency multiplication by 2.

4.1 Concept Introduction

Frequency doubling can provide a number of design options for generating the LO signals in a receiver, yet only a handful of IC-compatible circuits are found in the literature [40,31,32,33,35]. In general, most doubling techniques are limited by either having a single-ended or unbalanced output, or they require filtering between cascaded stages due to the undesired harmonic content present in the signal.

In addition to the stable circuits which were reviewed in Chapter 2, there exists another class of frequency doublers, typically found as discrete circuits, which are based on regenerative (or injection-locking) techniques. It is well known that an injection-locked oscillator, when employed as a constant envelope RF amplifier, can have an extremely high power-added efficiency over its injection locking range[41]. This characteristic of an injection-locked oscillator can also be exploited in a frequency doubler.

Traditional methods of regenerative frequency multiplication are generally based on the concept of sub-harmonic injection-locking[42]. In this technique, an LC-tank oscillator is locked to an input frequency source running at an integer sub-multiple of the oscillator's fundamental frequency. The non-linear characteristics of the oscillator's devices are relied upon to multiply the frequency of the input signal (f_{in}) up to higher integer harmonics (e.g. $2f_{in}$, $3f_{in}$, $4f_{in}$,... nf_{in}). If one of these harmonics falls within the locking range of the oscillator, then the oscillator will become locked to that harmonic and essentially will act as a selective harmonic amplifier. Although this technique works well, the stray coupling effects and area penalty of the inductors required for the oscillator core are undesirable, especially in a receiver design where other inductors are required (e.g. LNA).

Injection-locked oscillators, in general, have a number of fundamental properties which make them suitable for LO signal frequency doubling in an IC. For example the output signal amplitude is relatively independent of the injected signal amplitude. This is beneficial since amplitude modulated (or AM) noise is suppressed by the oscillator, and a constant amplitude output is obtained.

An injection-locked oscillator can also be thought of as a phase-locked loop (or PLL) with a wide closed-loop bandwidth. The settling time of an injection-locked oscillator is typically on the order of a few cycles of RF oscillation. For a 1 GHz ring, this translates to a PLL with a closed-loop bandwidth on the order of 300MHz.

With this concept in mind, some other characteristics can be discussed. Consider the properties realized by frequency modulated (FM) receivers which employ PLL-type demodulators. Once the desired FM signal is captured (or locked), the PLL inherently minimizes the effect of noise or interference by other nearby carriers, as long as the interfering signals are weaker than the desired FM input[9]. In a similar way, the injection locked ring oscillator suppresses undesired harmonics once it is locked to a (higher power) input carrier. Once frequency locked, the PLL tracks any input signal phase variations that are within the bandwidth of its feedback loop, which implies that the phase noise of a locked oscillator will also track the phase noise of the injecting source. Thus it is expected that the regenerative doubler will phase-lock to the injected LO, reject undesired harmonics, and preserve the phase

noise of the LO source. These are all beneficial and desirable qualities when applied to a receiver's LO signal.

The doubled-frequency output of the oscillator presented in this chapter is also relatively free of spurious content and does not require subsequent filtering. Furthermore, many doubling stages can be cascaded to realize higher levels of multiplication without adding significant undesired spurious components. As long as the entire chain of doublers are successively locked to one another, each stage will regenerate the desired LO signal and reject unwanted harmonics.

4.2 A Fundamentally-Locked Regenerative Frequency Doubler

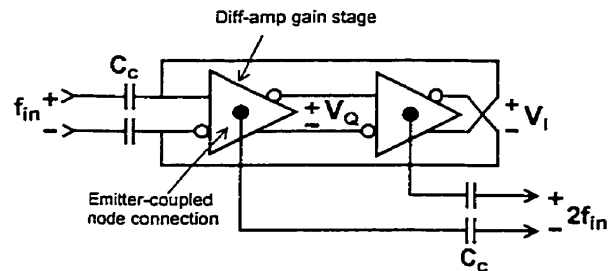


Figure 4.1: Regenerative doubler block diagram.

A new regenerative frequency doubling technique[19], which does not require the use of inductors, is illustrated in Figure 4.1. It is a quadrature ring oscillator which is injection locked in its fundamental mode to the input signal frequency f_{in} . The input signal is coupled to a 2-stage differential ring oscillator through capacitors C_c , and the double-frequency output signal is extracted across the emitter-coupled nodes of differential amplifiers within the ring.

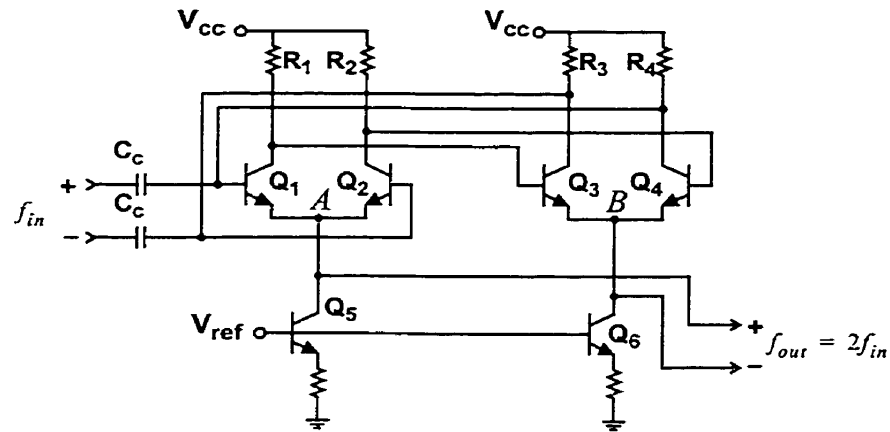


Figure 4.2: Regenerative doubler simplified schematic diagram.

A schematic diagram of the doubler is shown in Figure 4.2. The oscillator topology is similar to that of the circuit model used in the previous chapter (Figure 3.4) except that there are no emitter-followers between the stages. This results in less delay around the loop, allowing for a higher frequency of operation, and allows the circuit to operate from a lower supply voltage. The doubled-frequency output voltage (f_{out}) is taken differentially across the emitter-coupled nodes of the two amplifiers in the ring (marked as nodes A and B in the figure). These A and B outputs are anti-phase (0° and 180°) as a result of the 0° and 90° phased differential input signals appearing at the base nodes of the transistor pairs Q_1, Q_2 and Q_3, Q_4 respectively. This is illustrated graphically in Figure 4.3.

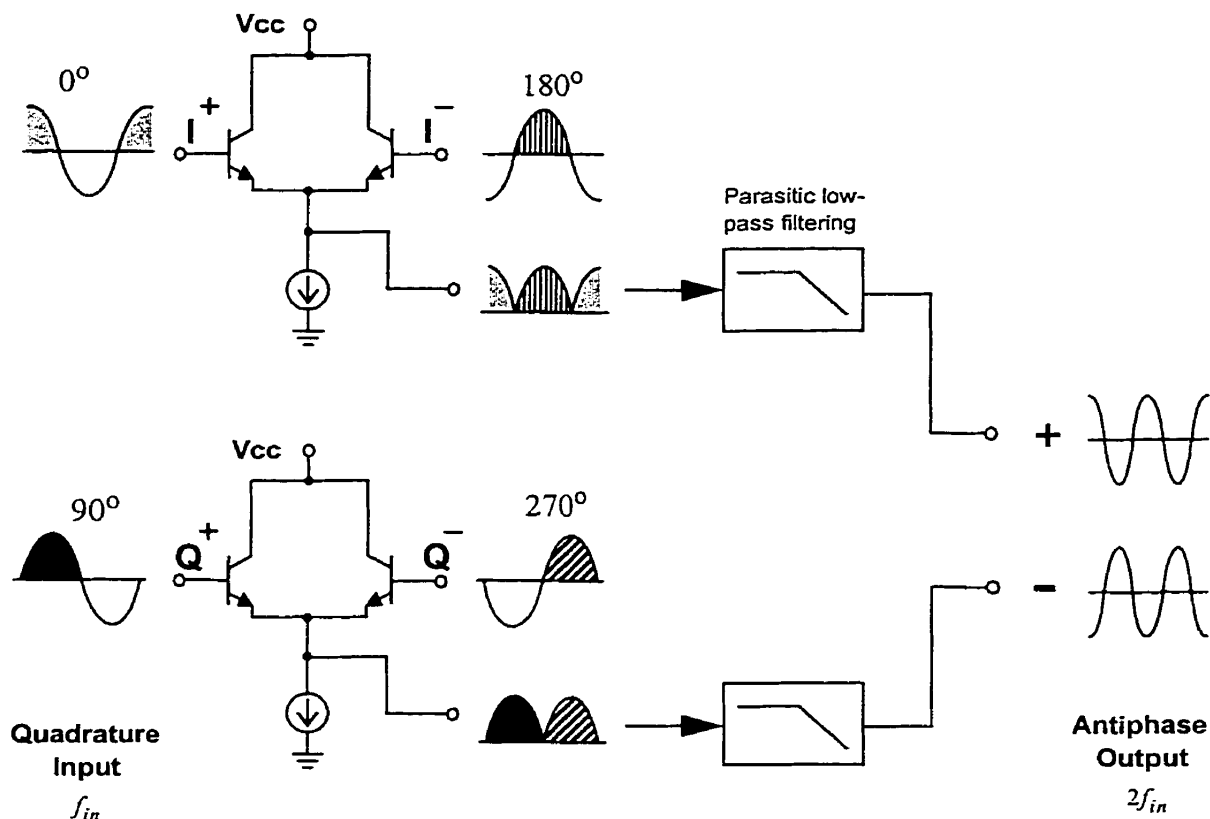


Figure 4.3: Illustration of quadrature input to differential output in the ring amplifiers.

There are many advantages that are immediately realized with this technique: good efficiency (i.e. a low-power ring oscillator design can be employed), high operating frequency range (output to greater than $f_T/2$), and a very wide locking range ($> 50\%$ relative bandwidth) is possible. Since the oscillator is being locked in its fundamental mode of oscillation, equation 3.7 remains valid and implies that if the oscillator's output amplitude is scaled down by design, then the input signal amplitude requirement will also scale proportionally. Another benefit of this technique is that the resistively-loaded ring oscillator can easily be designed for low or high-frequency operation without consuming significant chip area compared to most other types of oscillators which require the use of inductors in their resonant tanks.

4.2.1 Emitter-Coupled Doubling Mechanism

The frequency-doubling mechanism which generates the doubled-frequency output in the oscillator is based on large-signal rectification (i.e., the same mechanism exploited in the circuit of Figure 2.16). In small-signal analysis, the emitter-coupled node of a transistor differential pair (Figure 4.4) is often considered an ac ground. For signals larger than approximately $2V_T$, the signal voltage at the emitter-coupled node is not zero and consists of mainly even-order harmonics due to the full-wave rectification by the base-emitter junctions of transistors Q_1 and Q_2 . For each half-cycle of the input, one transistor drives the emitter load in an emitter-follower configuration, while the other transistor is essentially turned-off. As a result, this circuit provides a low output impedance and maintains a good load driving capability at very high frequencies (to $f_T/2$)[22].

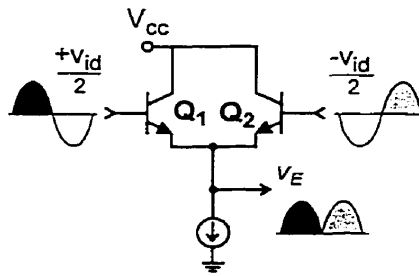


Figure 4.4: Emitter-coupled pair driven in a large-signal model.

The voltage at the emitter-coupled node is determined from the large signal equation for the base-emitter junction voltage,

$$V_{BE} = V_T \ln \frac{I_C}{I_S}. \quad (4.1)$$

Using equation 4.1 and Kirchoff's voltage law to express the base-emitter junction voltages for transistors Q_1 and Q_2 in Figure 4.4, the emitter-coupled node voltage, V_E is

$$V_E = \frac{V_T}{2} \left[1 + \cosh \left(\frac{V_{ID}}{V_T} \right) \right] + (\text{dc term}). \quad (4.2)$$

Corrections for NT25 specific large-signal parameters for a 0.5 μm x 5 μm device, results in the device-specific equation:

$$V_E = 3.2 \cdot \frac{V_T}{2} \left[1 + \cosh\left(\frac{V_{ID}}{3V_T}\right) \right] + (\text{dc term}). \quad (4.3)$$

Equation 4.3 matches the characteristic of a diff-pair simulated in HSPICE to within 2%. Both characteristics are plotted in Figure 4.5 after subtracting their respective dc bias voltages.

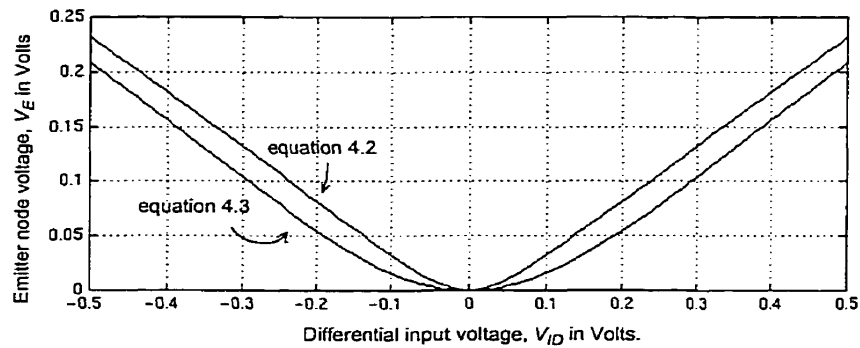


Figure 4.5: Emitter-coupled node voltage as a function of differential input voltage.

For $\|V_{ID}\|$ approximately $> 2V_T$, the equations plotted above are similar that of a full-wave rectifier,

$$V_e = \frac{1}{2} \|V_{ID}\|, \quad (4.4)$$

except for the dc bias shift.

A similar characteristic is also found at the source-coupled node of a CMOS differential pair which implies that the frequency-doubling techniques presented in this thesis using bipolar devices can also be realized using CMOS devices with only minor circuit modifications.

By substituting,

$$V_{ID} = A \cos(\omega t + \theta_e), \quad (4.5)$$

into equation 4.4, the emitter-node voltage of an input differential cosine wave of amplitude A is given by,

$$V_e(t) = \frac{2A}{\pi} \left[\frac{1}{2} + \frac{1}{3} \cos(2\omega t + 2\theta_e) - \frac{1}{15} \cos(4\omega t + 4\theta_e) + \frac{1}{35} \cos(6\omega t + 6\theta_e) + \dots - \frac{(-1)^n}{(4n^2 - 1)} \cos(2n\omega t + 2n\theta_e) \right] \quad (4.6)$$

(see [43]). From this equation it is observed that the double-frequency component at the emitter-node will have a maximum amplitude of,

$$\frac{2A}{3\pi} \cong (0.21)A, \quad (4.7)$$

and that the next higher harmonic will naturally be suppressed relative to this amplitude by,

$$20 \log \left(\frac{1/15}{1/3} \right) = -14 \text{ dB}, \quad (4.8)$$

even before parasitic filtering effects come into play.

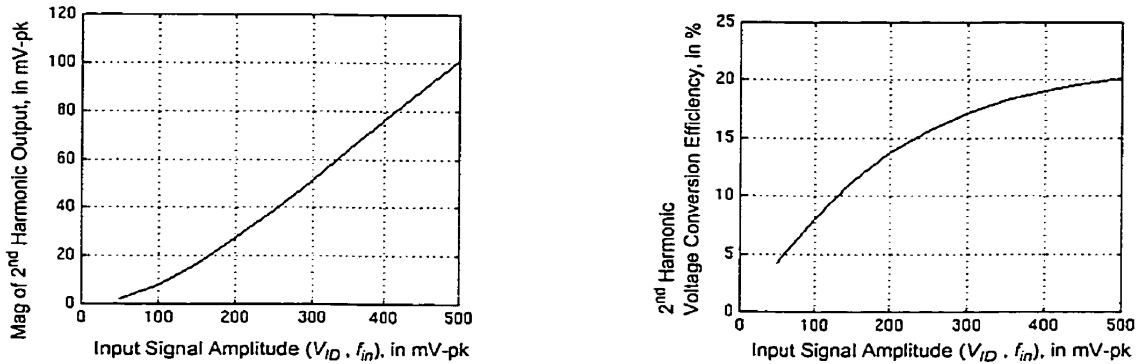


Figure 4.6: Voltage conversion.

Figure 4.6 is obtained through fast-Fourier transform analysis of the output (V_E) from equation 4.3 for a single-tone sinusoidal input. The amplitude of the second harmonic component of V_E is plotted as a function of input signal amplitude and as a fraction of the input signal amplitude (or voltage conversion efficiency $\|V_{2nd}\|/\|V_{fund}\|$). It is observed here that the maximum expected voltage conversion efficiency (of 21% from equation 4.7) is approached for an input signal amplitude of approximately 500 mV peak (differential) in the oscillator. It should be noted however, that although the voltage gain is less than unity there is current gain provided by the impedance transformation from base to emitter and additional voltage gain when the injected signal voltage is less than the oscillator output voltage.

An important quality of any frequency-doubling circuit is its ability to suppress feed-through or ‘leakage’ of the input fundamental harmonic to the output. In the circuit of Figure 4.4, the fundamental input frequency will only be suppressed from appearing at the output node (V_E) if the transistors are well matched, have an identical dc bias, and are driven from a purely differential input source. Any common-mode component at the input couples directly to the emitter-coupled node. Since transistor matching and dc bias can be balanced well in an IC, the suppression of the fundamental signal at the output depends almost entirely on the differential symmetry of the input signal.

In the regenerative doubler of Figure 4.2, capacitive coupling of the input signal to the oscillator prevents any unbalancing of the dc bias point in the oscillator. Even while oscillating, the dc symmetry of the circuit ensures that the average value of all the base node voltages of Q_1 - Q_4 are identical. Another benefit of the topology of Figure 4.2 is that even if the input source is entirely single ended, the oscillator’s feedback connection causes the input transistor pair to see a predominantly differential-mode signal across its base nodes. These properties of the differential ring-oscillator topology work to suppress the fundamental component of the input signal from appearing at the emitter-coupled output nodes.

4.2.2 I-Q Phase Errors in the Ring due to Injection

A resistively-loaded ring oscillator typically has a low Q -factor and therefore requires a relatively small amount of phase shift in the feedback loop to alter the free-running frequency. When the ring oscillator is locked at a frequency other than ω_o , the V_I and V_Q outputs of the ring (see Figure 4.1) have a small phase error (ϕ_ϵ) from 90° (or quadrature) caused by the injected signal. The magnitude of this phase error depends on how far the locking frequency is from the oscillator’s natural free-running frequency and on the value of the oscillator’s Q .

Using equation 3.7, an oscillator with a Q -factor of 0.2 (such as that of Figure 3.5), and a 50% relative locking range will have a quadrature phase error of approximately 0.2 radians or 11° at the band edges. Across the emitter-coupled output nodes of the oscillator (A and B), this translates to a 22° phase error (or $2\phi_\epsilon$) from the ideal anti-phase (180°) condition according to equation 4.6.

For a given phase error, the voltages at A and B can be broken into a sum of differential (across A and B) and common-mode (referred to ground) components. If φ_e is zero, then the output signal is (by definition) fully-differential, but if $\varphi_e = 90^\circ$, then voltages at nodes A and B are in phase, and the output signal is entirely common-mode. For a single-ended output signal amplitude of A_o (at each of the nodes A and B), the amplitude of the differential component of the output can be stated as,

$$A_{v_{diff}} = 2A_o \cos(\varphi_e), \quad (4.9)$$

and the common-mode amplitude as,

$$A_{v_{comm}} = A_o \sin(\varphi_e), \quad (4.10)$$

leading to the suppression of the common-mode expressed in dB with respect to the differential amplitude as

$$\text{Common-mode suppression} = 20 \log \left(\frac{A_{v_{diff}}}{A_{v_{comm}}} \right) = 20 \log(2 \cot(\varphi_e)). \quad (4.11)$$

Consider again, the (realistic) case of an oscillator having a Q of 0.2 and an injection locking range of 50%; an extreme locking range for most applications. With $\varphi_e = 11^\circ$, equation 4.11 describes the common-mode voltage as being suppressed below the differential signal by greater than 20 dB.

Subsequent differential RF stages, such as a buffer or a mixer, will typically provide further common-mode rejection and it is therefore suggested that the differential output of this circuit can be considered almost fully-differential for most practical design purposes.

It was determined in the previous chapter that the output amplitude of the oscillator of Figure 3.5 is approximately 340 mV-peak. Using the characteristic of Figure 4.6, the doubled-frequency output at the emitter-coupled nodes is approximately 62 mV-peak (in 0° and 180° phases). When this output is taken differentially across the two emitter-coupled nodes, it becomes 124 mV-peak.

4.3 Regenerative Doubler Variations

There are many variations of the basic doubler which can provide unique options to the designer. A few of the more interesting concepts are presented briefly in this section.

4.3.1 Regenerative Frequency Quadrupler

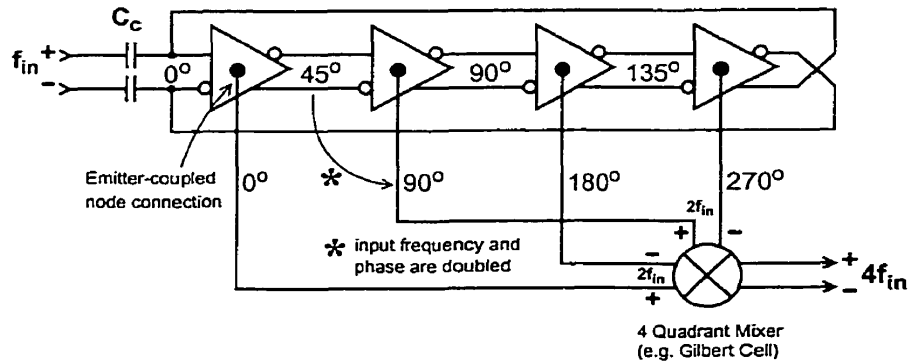


Figure 4.7: Regenerative frequency quadrupler.

In this realization, the 4-stage ring generates 4 unique phases (labeled 0° , 45° , 90° , and 135°) at the fundamental frequency. The four double-frequency emitter-coupled node voltages form two fully-differential signal pairs that are 90° phase shifted. These double-frequency quadrature signals can then be multiplied together using a 4-quadrant analog multiplier, such as a Gilbert multiplier, to generate a fully-differential, quadrupled ($4f_{in}$) output signal.

4.3.2 Regenerative Frequency Tripler

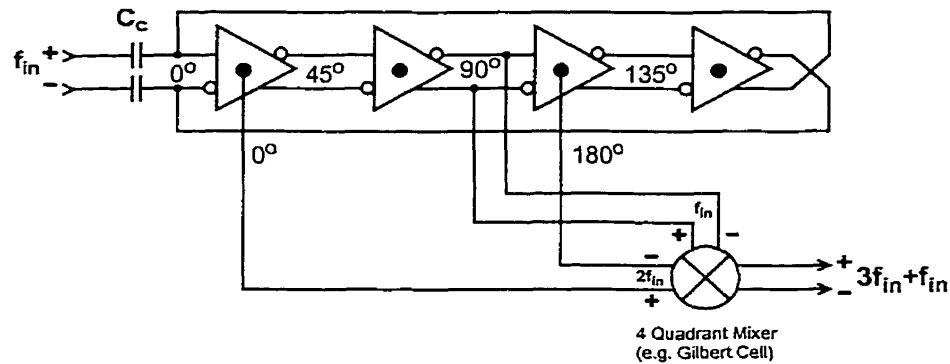


Figure 4.8: Regenerative frequency tripler.

The circuit of Figure 4.8 provides a frequency tripling function by multiplying the fundamental signal circulating around the ring with one of the double-frequency signals. The result is a $3f_{in}$ signal summed with an f_{in} signal.

4.3.3 Frequency Tracking ILRO

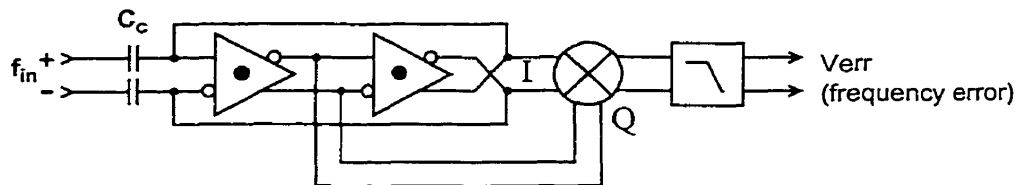


Figure 4.9: A frequency-tracking injection locked ring oscillator.

An interesting property of the injection-locked quadrature oscillator is that the I and Q outputs are only in exact quadrature (i.e. $\varphi_e = 0^\circ$) when the oscillator is locked at the free-running frequency. This property could be exploited to calibrate the oscillator's centre frequency, or to provide a frequency tracking capability.

In Figure 4.9, the I and Q outputs of the ring are multiplied together using a 4-quadrant multiplier and then passed through a low pass filter.

$$\cos(\omega t) \cdot \cos\left(\omega t + \frac{\pi}{2} + \varphi_{\varepsilon}\right) = \frac{1}{2} \left[\sin(\varphi_{\varepsilon}) + \cos\left(2\omega t + \frac{\pi}{2} + \varphi_{\varepsilon}\right) \right] \quad (4.12)$$

~~Low pass filtered~~

$$v_{err} = \frac{1}{2} \sin(\varphi_{\varepsilon}) \quad (4.13)$$

The resultant error signal v_{err} is a dc voltage defined by equation 4.13. This signal can be used to indicate the error between the free-running frequency of the oscillator and the frequency to which it is currently locked. If the ring oscillator were redesigned as a voltage controlled oscillator, a negative feedback loop could allow v_{err} to control the free-running frequency of the oscillator and cause it to track the injected signal. This would essentially cause the I and Q outputs to remain in precise quadrature for all locked frequencies. Furthermore, this would force the double-frequency output phases to always remain 180° apart, eliminating any common-mode component in the double-frequency the output.

4.4 Conclusion on Regenerative Frequency Doubling

A new method of regenerative frequency doubling using an injection-locked ring oscillator has been presented. As a result of the injection-locked nature of the circuit, this technique is especially useful in situations where the output frequency required is at a very high fraction of the unity-gain frequency available in an IC technology. In Chapter 6, this technique is employed as part of a larger LO system which cascades two regenerative doublers followed by a regenerative quadrature divider. The operation and topology of the regenerative divider is presented in the next chapter.

CHAPTER

5

A Frequency Halver with Precision Phase Tuning

In this chapter, the concept of a regenerative frequency halver is presented with the aid of another Simulink model, similar to that which was used to describe ILRO behaviour. From this model, a new technique for providing precision phase tuning is suggested along with a practical method for realizing the desired phase tuning functionality.

5.1 A Regenerative Frequency Halver (Divider)

Frequency divide-by-2 circuits based on analog injection-locking techniques to perform frequency division are known as “frequency halvers” or “regenerative dividers”.

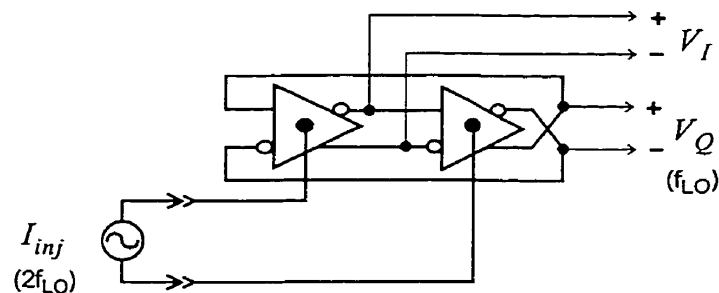


Figure 5.1: 2-Stage frequency halver block diagram.

The block diagram of a frequency halving circuit (shown in Figure 5.1) which was first presented in [26], can use the circuit topology of Figure 3.4 to realize the differential amplifying stages of the ring. Referring to Figure 5.1, a differential ac current source is connected across the emitter-coupled nodes of the ring and is set at a frequency which is twice that of the fundamental frequency of the ring. This causes the doubled-frequency emitter-coupled node voltages of the ring oscillator to synchronize to the injected currents of I_{inj} . This topology is very similar to the regenerative frequency doubler in Figure 4.1 except that the input and output ports are reversed. An important feature of the halver is that the emitter-coupled double-frequency signal injection is symmetric with respect to the topology of the ring since the injected currents affect both amplifying stages of the oscillator identically. The result of this symmetry is that the outputs V_I and V_Q are in precise phase quadrature over the entire locking range of the oscillator. The frequency of the quadrature output is one-half that of the injected current and so the circuit performs a frequency divide-by-2 (or halving) function.

5.2 Simulink Model of the Regenerative Frequency Divider

A Simulink model can also be used to predict the behaviour of the regenerative divider. Using the circuit shown in Figure 3.9b to realize the differential amplifiers of the oscillator in Figure 5.1, the Simulink model of Figure 5.2 is obtained.

I_{EE} is the dc bias current for the emitter-coupled pair Q_1 - Q_2 in Figure 3.4b, and is assumed to be much greater than the amplitude of the differential RF input current I_{inj} (i.e., $I_{EE} \gg \|I_{inj}\|$). The input signal I_{inj} is an ac differential current source and therefore adds with in-phase to the (I_{EE}) bias current for one of the stages and anti-phase to the (I_{EE}) bias current for the other stage.

The result is a pair of differentially-modulated bias currents which are then multiplied by the respective \tanh functions of each diff-pair to obtain differential large-signal transistor output currents I_{odI} and I_{odQ} in the model. The parameters of the oscillator in Figure 5.2 are identical to the model described in Figure 3.5 since the same circuit is being used for the gain stages (Figure 3.4b).

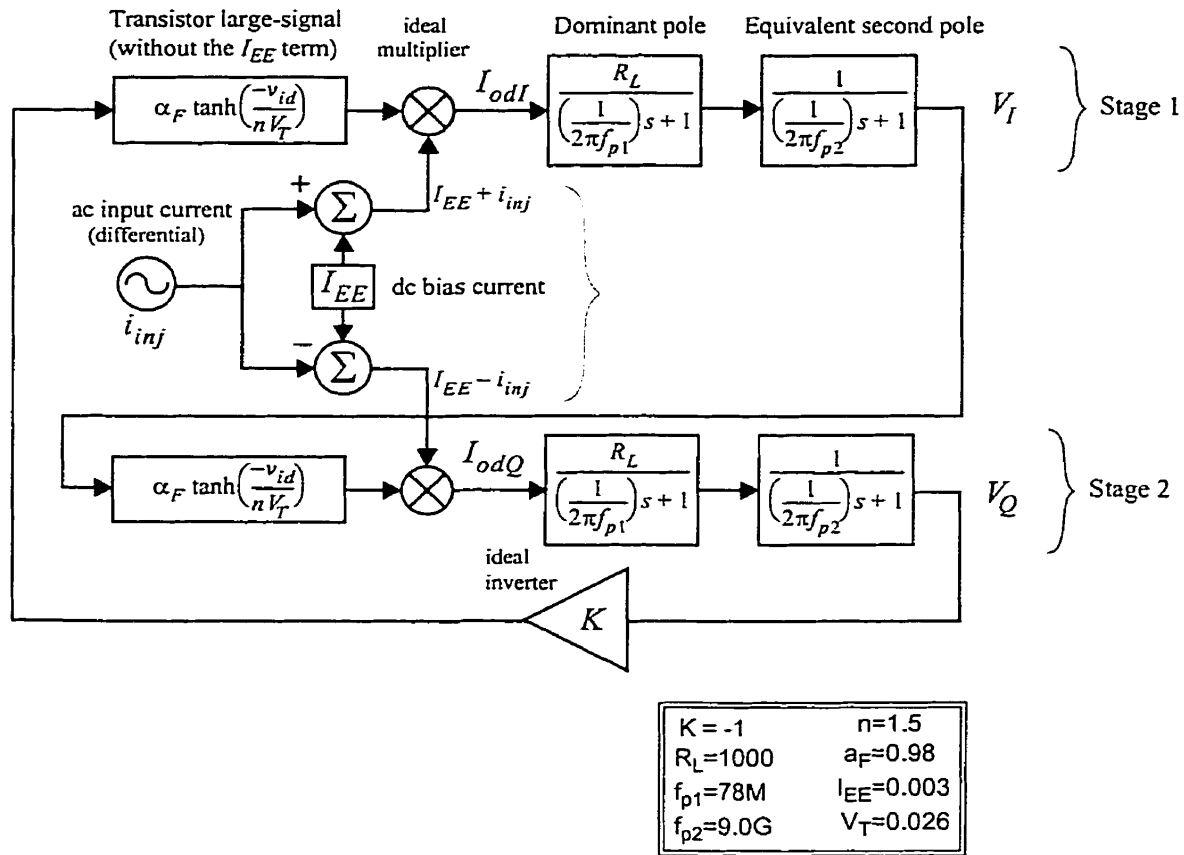


Figure 5.2: Simulink model of the 2-stage regenerative divider.

For an input signal amplitude of 310 μA -peak, HSPICE simulations predict that the oscillator will have a lower frequency locking boundary of 1.38 GHz (injected frequency) which compares favourably to the 1.40 GHz prediction from the Simulink model. Simulink also predicts that the upper locking frequency boundary is 2.30 GHz, whereas HSPICE predicts 2.20 GHz. The error of this Simulink model at the higher frequency end of the range is likely due to higher-order poles in the real circuit that are not accounted for in the model (e.g. C_μ , R_b , etc.)

The model of Figure 5.2 also implies that the quadrature output amplitudes of the frequency halver are defined by Equation 3.25 with a -6 dB/octave response, where ω_{inj} corresponds to the output frequency of the halver.

5.3 Precise Phase Control of Quadrature LO Signals

As was mentioned earlier, the I and Q output phases of the regenerative divider remain in quadrature throughout the locking range of the oscillator. In practice, this can be achieved with a phase error on the order of $< 1^\circ$.

In the realization of Figure 5.3, emitter-followers are not used between amplifying stages to allow for a lower supply voltage and an increased maximum operating frequency. The injected double-frequency signal ($2f_{LO}$) is capacitively coupled to the emitter-coupled nodes for illustration. In a real implementation however, a transconductance stage is used to provide the bias for $Q_1 - Q_4$ and to inject the double frequency input into the ring.

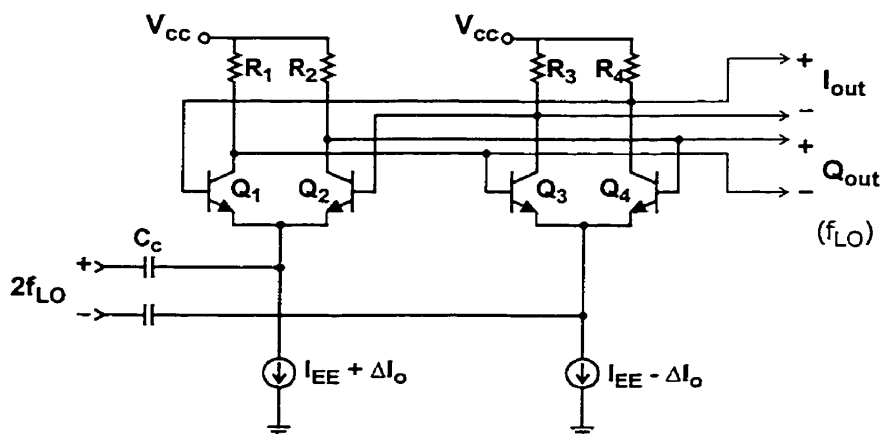


Figure 5.3: Regenerative divider simplified schematic diagram.

Normally, the time delays through each amplifying stage in the ring oscillator are well-matched due to the electrical symmetry of the devices. By intentionally disrupting the symmetry of the ring, the time delay (or phase) through each stage of the ring is altered, resulting in a slight phase shift between the I and Q outputs, away from quadrature.

From a frequency-domain perspective, the frequencies of the higher order poles of each diff-pair are sensitive to the transistor's bias current. By differentially altering the bias current through each stage in the ring, the higher-order poles of each amplifier will shift in opposite

directions, thus intentionally altering the phase relationship between the quadrature outputs of the ring. Figure 5.3 illustrates a small offset current (ΔI_o) being added differentially to the bias currents I_{EE} to perform the phase shift.

There are two important features of this new phase tuning technique: firstly, since the control mechanism for phase shifting is through a dc bias offset, it is relatively easy to make very small phase changes (on the order of $< 0.1^\circ$) between the quadrature outputs of the ring. The smaller the dc offset, the smaller the phase change. Secondly, unlike the frequency-dependent phase shift found in an RC-network for example, the induced phase shift in the oscillator is strongly independent of the frequency of oscillation. This is because the phase shift is a result of the difference between two frequency-dependent time delays in the ring. This implies that if a given phase shift is intentionally calibrated at one frequency, it will not necessarily need to be re-calibrated at other nearby frequencies. It should also be mentioned that the phase noise of the output is expected to be reduced by a factor of 2 (or -6dBc) below the phase noise of the input signal due to the division of phase which occurs in a divider[20].

5.4 Frequency Halver

The frequency halver in Figure 5.1 uses the same oscillator topology and injection-locking principals as the regenerative doubler in Figure 3.4a and therefore shares in many of its benefits and properties. The halver can be designed to operate efficiently at very high frequencies ($> f_T/2$) and has the added feature of providing a means of precise I-Q phase angle adjustment through a simple dc offset bias control. These properties of the halver are exploited in the next chapter for the purpose of accurate quadrature signal generation intended for a 5-6GHz receiver IC.

CHAPTER

6

A Regenerative LO System for a 5-6GHz Integrated Receiver

In this chapter, a complete LO system design is presented for a 5-6GHz integrated receiver implemented in the NT25 process. A discussion of the block diagram of the system is followed by a detailed look at the individual circuits employed for each LO function.

Performance specifications from simulation are included to provide a general idea of the signal levels involved and the power consumption required for each of the various RF stages.

6.1 Local Oscillator System Architecture and Design

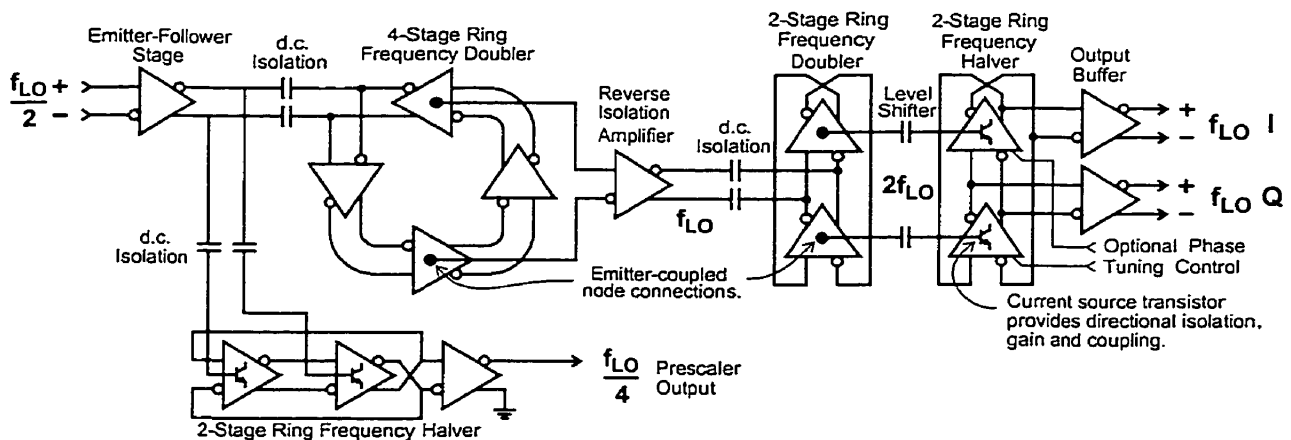


Figure 6.1: Local oscillator subsystem architecture.

Figure 6.1 shows a block level diagram of the complete LO system. The $f_{LO}/2$ input signal is first buffered by a simple emitter-follower stage to ensure that a low on-chip impedance is presented to the oscillators. These emitter-follower devices are implemented by externally biasing the base nodes of transistors Q_1 and Q_2 in Figure 2.7 (and by connecting the emitter nodes of Q_3 and Q_4 to V_{cc}).

The first regenerative doubling stage is a 4-stage ring oscillator which is injection locked in its fundamental mode to the emitter-followed $f_{LO}/2$ input signal. A differential and doubled-frequency signal (f_{LO}) is extracted from two emitter-coupled nodes at opposite (and quadrature) sides of the ring. The f_{LO} differential output signal is then fed to a buffering amplifier (Figure 6.2) to help increase the locking range of the next oscillator and to ensure that injection locking proceeds in one direction (from left to right in Figure 6.1) only.

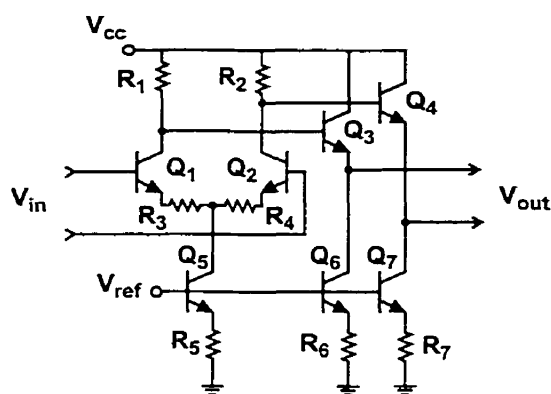


Figure 6.2: General buffer topology.

The second frequency doubler in the chain is implemented using 2-stage differential ring oscillator which is locked in its fundamental mode by input frequency, f_{LO} . Its free-running frequency has been designed to be centred at twice the free-running frequency of the 4-stage ring before it, and therefore provides an output frequency of $2f_{LO}$ (or 4 times the input to the first doubling stage) when both rings are locked.

A 2-stage frequency halver then divides the $2f_{LO}$ signal (by 2) into accurate I and Q signals of frequency, f_{LO} . Another buffering stage (Figure 6.2) is subsequently used to

increase the I and Q output voltage swing and to provide a low impedance for driving the base nodes of the I and Q receive mixers (shown in Figure 2.6).

The 2-stage halver and the 2-stage doubler are virtually identical ring oscillators running at the same fundamental frequency (f_{LO}), however, they are coupled by the doubled-frequency voltages at their emitter-coupled nodes. The halver is symmetrically driven by the $2f_{LO}$ signal, and as a result the I and Q outputs of the halver remain 90° phase shifted with a phase error on the order of less than 1° . A phase tuning control line is also made available to allow for precise phase adjustments of the I and Q-LO outputs.

The LO system also includes a 2-stage halver to produce an $f_{LO}/4$ “prescaler” output. This output is useful as it allows a sub-2 GHz frequency synthesizer to be used with the IC to generate the input $f_{LO}/2$ signal. The prescaler has its own supply pin and can be powered up separately from the rest of the LO system, allowing it to be used as an optional feature. The input to the prescaler is a high-impedance transconductance stage and this provides reverse isolation between the $f_{LO}/4$ output of the prescaler and the $f_{LO}/2$ at input signal. The transconductance stage is shown later in a detailed schematic of the divider circuit.

6.1.1 Selection of Free-Running Frequency

The LO system was initially designed under the assumption that the locking range of an oscillator is symmetric about its free-running frequency. This implies (from Table 2.1), that the center frequency of the LO system should be designed to be,

$$\frac{6.5\text{GHz} - 4.5\text{GHz}}{2} = 5.5\text{GHz} . \quad (6.1)$$

However, simulations of the LO system indicate that the locking ranges of the oscillators are not symmetric. The upper locking boundary for the chain of oscillators is found to be limited by the frequency at which the I-Q divider fails to remain locked to the $2f_{LO}$ output from the second doubling stage. Simulations also show that the $2f_{LO}$ signal becomes severely degraded at the upper end of the range (near 13 GHz) as a result of parasitic loading, low transistor current gain, and the -6 dB/octave characteristic of the ILRO.

As the input frequency to the chain of oscillators is lowered, the output amplitude from each oscillator increases by about +6 dB/octave (as expected from ILRO discussions in Chapter 3). This increases the amplitude of the injection signals between oscillators and leads to an overall extension of the lower end of the locking range.

Manual optimization of the centre frequency was carried out over a series of design iterations using large-signal (HSPICE) simulations to maximize the locking range while considering power dissipation, performance, and process variations. The optimal centre frequency for the design was determined to be 6.25 GHz. This centre frequency is used in the analysis of the 4-stage ring in later sections.

6.1.2 Transistor Sizing

All of the transistors used in the LO system are single-unit $0.5 \times 5.0\mu\text{m}^2$ emitter-area devices. Generally, a reduced emitter-area device offers lower parasitic capacitances and lower current consumption for a negligible increase in transistor noise[21]. Although the NT25 process does offer an emitter length as short as $1.3\mu\text{m}$, there was concern that corner rounding and foreshortening effects of the emitter-window area (as shown in Figure 6.3) could cause the actual transistors parameters to deviate significantly from the simulated models.

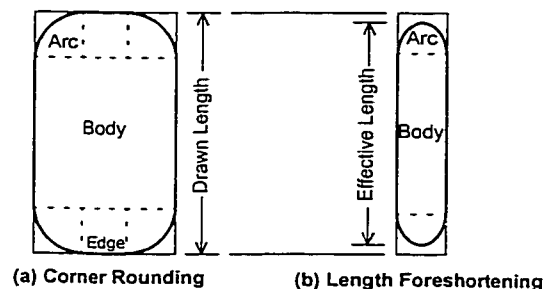


Figure 6.3: Planar Illustration of the emitter window layout and etched areas[44].

A $0.5 \times 5.0\mu\text{m}^2$ device has a length-to-width ratio of 10:1, significantly increasing the “body” to “arc” area (as labeled in the figure) and thus reducing emitter-area sensitivity to window-etching effects.

6.2 First Frequency Doubling Stage

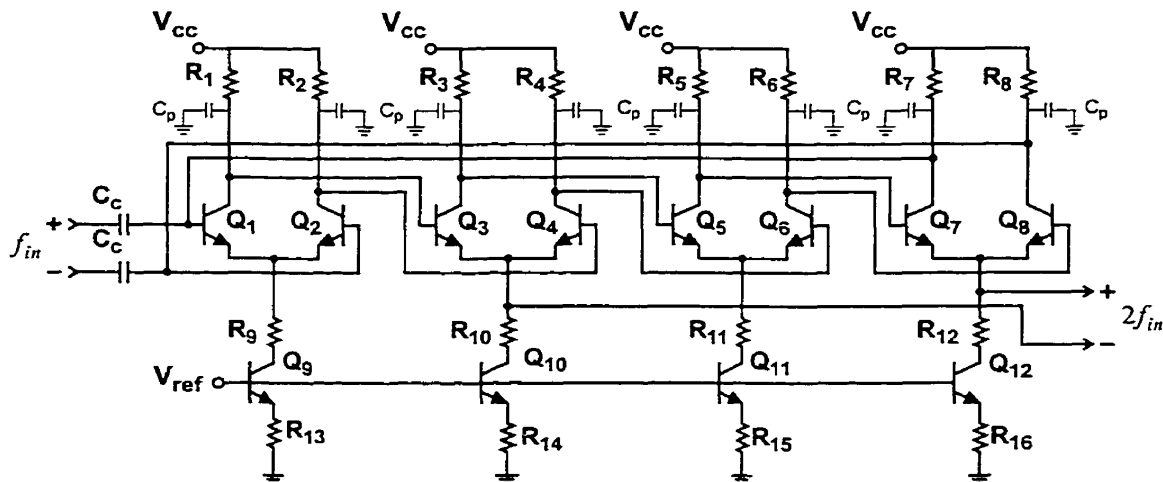


Figure 6.4: 4-Stage ring: (first) frequency doubler.

Figure 6.4 shows a detailed schematic of the first frequency doubling stage of the LO system. The physical areas of the poly-silicon resistor loads R1 through R8 are included in the design to control and make use of their parasitic capacitances (C_p). Since there are four amplifying stages in the ring of Figure 6.4, each stage contributes 45° of phase lag at the free-running frequency and the cross-coupled connection R5 provides the remaining 180° necessary for sustained oscillation.

The use of a 4-stage ring rather than a 2-stage ring allows the doubled-frequency output signal ($2f_{LO}$) to be extracted from the emitter-coupled nodes of Q₃-Q₄ (and opposite pair Q₇-Q₈) rather than directly from the emitter-coupled nodes of the input transistors Q₁-Q₂. This is important if the IC is driven by a single-ended input source, since the common-mode rejection of the input differential-pair improves the suppression of fundamental signal at the output. Resistors R₉ - R₁₂ increase the real part of the output impedance of the current mirror transistors at high frequencies, and thus increase the common-mode rejection of each stage.

In order to conserve current, it is wise to bias the transistors for this stage such that the operating margin (f_T/f_{RF}) is approximately less than 5 at the highest frequency of oscillation (i.e., 3.25 GHz from Table 2.1). This effectively places the margin allocated for this stage on

par with the margin available in subsequent stages, where f_{RF} is higher. Using the data from the curves of Figure 2.9, the current required to bias a $0.5 \times 5.0\mu\text{m}^2$ device for an f_T of 15GHz, is approximately $200\mu\text{A}$.

6.2.1 Setting the Free-Running Frequency and Determining Amplitude

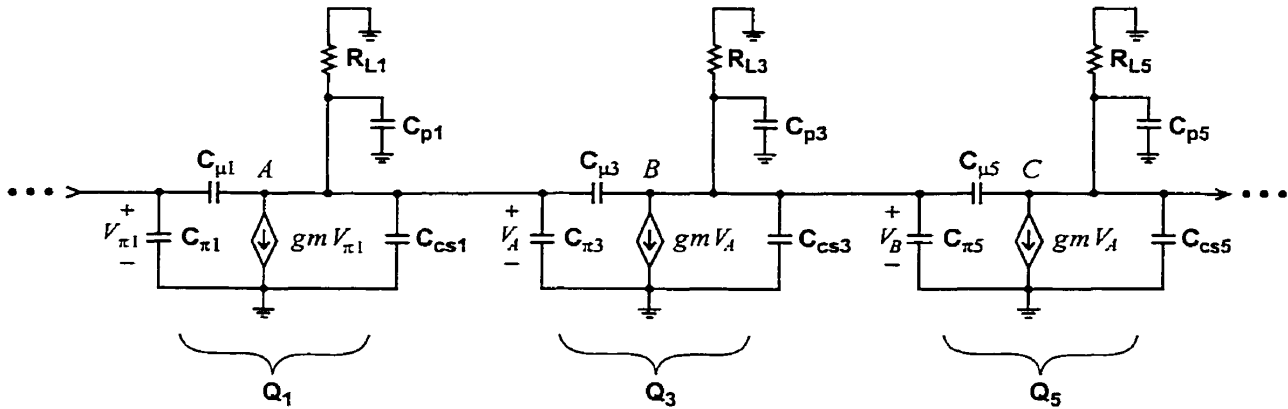


Figure 6.5: AC small-signal half-circuit of an amplifying stage in the ring.

Shown in Figure 6.5 is a simplified, ac small-signal half-circuit of one of the amplifying stages in the ring (Q_3), surrounded by its adjoining transistors (Q_1 and Q_5). Load resistor R_L and parasitic capacitance C_p are related to each other as,

$$R_L = R_{\square} \frac{L}{W}, \quad (6.2)$$

and

$$C_p = \frac{C_{area} WL}{2} + C_w, \quad (6.3)$$

where R_{\square} is the sheet resistance, C_{area} is the capacitance per unit area of the poly layer, and C_w is the metal wiring parasitic capacitance to the substrate. Capacitors C_{μ} , C_{π} , and C_{cs} are the transistor base-emitter, base-collector, and collector-substrate capacitances respectively. The factor of 2 in the denominator of (6.3) defines the parasitic capacitance at each node for a π -type model of the resistor. Based on the circuit topology, one-half of the resistor's parasitic capacitance is shunted to ac ground at the V_{cc} node and can be neglected. In simulations, a more distributed RC model is used for increased accuracy.

In order to simplify the analysis, the small-signal transistor model used in Figure 6.5 assumes that only parasitic capacitances are important at the frequencies of interest and that resistive elements (such as r_{π} and r_b) can be ignored.

The phase shift from transistor to transistor in the half-circuit analysis consists of two parts: the phase inversion provided by each transistor and the additional phase delay due to the load. Since there are 4 transistors in the half-circuit loop, these inversions sum to 360° and cancel out.

The free-running frequency of the oscillator is set by choosing R_L and C_p such that the additional phase delay (due to the load) from V_A to V_B is 45° at $f_o = 3.125\text{GHz}$. This can be done by first determining the total equivalent capacitance from node V_B to ground, and then setting the dominant pole frequency of this node to f_o by an appropriate choice of R_L .

In order to simplify the analysis, it is assumed that the parasitics of the transistors do not change significantly when the oscillator reaches its steady-state solution. In the periodic steady state, the oscillator amplitude is constant and thus the ac voltage at the collector of each transistor in the ring is identical. Voltages V_A and V_B at steady state are 225° apart (i.e., phase delay due to the load plus the inversion) and can be written as phasor quantities related by,

$$V_A = -\frac{V_B}{\sqrt{2}} + j\frac{V_B}{\sqrt{2}}. \quad (6.4)$$

Consider the admittance seen at node B looking into $C_{\mu 3}$ as depicted in Figure 6.6.

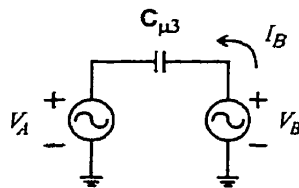


Figure 6.6: Calculating the admittance looking into $C_{\mu 3}$ from node B .

The current through $C_{\mu 3}$ can be written as a function of voltage with the aid of equation 6.4 as,

$$\frac{I_B}{V_B} = \left(1 + \frac{1}{\sqrt{2}}\right)j\omega C_{\mu} + \frac{\omega C_{\mu}}{\sqrt{2}}, \quad (6.5)$$

which is recognized as a shunt RC network with component values as illustrated below.

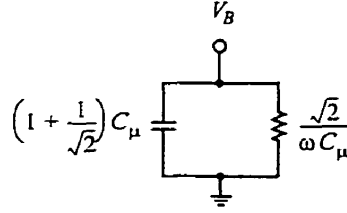


Figure 6.7: Shunt RC equivalent network of $C_{\mu 3}$ from the viewpoint of node V_B .

In a similar way, $C_{\mu 5}$ can also be replaced by the identical network of Figure 6.7 except for a minus sign which appears in front of the resistor equation due to the change in sign of the phase shift. When the equivalent networks for $C_{\mu 5}$ and $C_{\mu 3}$ are placed in parallel, the negative and positive resistances cancel out leaving only the capacitive terms. The total capacitance on node V_B can now be written (dropping the numerical subscripts) as,

$$C_T = C_p + C_{cs} + C_{\pi} + 2\left(1 + \frac{1}{\sqrt{2}}\right)C_{\mu} \quad (6.6)$$

This allows the value of loading resistor R_L to be solved for as a function of it's width (W), wiring capacitance (C_w), and oscillator free-running frequency (f_o) by combining (6.2), (6.3), and (6.6) giving,

$$R_L = \frac{1}{2\pi f_o C_T} = \frac{1}{2\pi f_o \left[\left(\frac{R_L W^2 C_{area}}{2R_{\square}} \right) + C_w + C_{cs} + C_{\pi} + 2\left(1 + \frac{1}{\sqrt{2}}\right)C_{\mu} \right]} \quad (6.7)$$

which simplifies to the quadratic equation,

$$\left[\frac{W^2 C_{area}}{2R_{\square}} \right] R_L^2 + \left[C_w + C_{cs} + C_{\pi} + 2\left(1 + \frac{1}{\sqrt{2}}\right)C_{\mu} \right] R_L - \frac{1}{2\pi f_o} = 0 \quad (6.8)$$

In order to solve equation 6.8, the transistor and resistor parasitic capacitances need to be determined. As a result of the base-to-collector connections of Q_1 to Q_8 (in Figure 6.4), the

base-collector capacitance (C_μ) is simply the zero-bias junction capacitance obtained directly from the SPICE model file for the device. C_π can then be related to the transistor bias via f_T by,

$$f_T \cong \frac{1}{2\pi} \frac{g_m}{(C_\pi + C_\mu)}, \quad (6.9)$$

combined with,

$$g_m = \frac{I_C}{V_T}, \quad (6.10)$$

where I_C is the collector dc bias current and V_T is the thermal voltage[22]. A summary of the parameter values required to solve equation 6.8 are shown in Table 6.1 (for a nominal supply voltage of 2.2 Volts).

Table 6.1: First doubling stage design parameters.

Parameter	Value
f_o	3.125GHz
I_C	200uA
f_T	15GHz
g_m	7.69mA/V
C_μ	10fF
C_π	72fF
C_{cs}	17fF
C_{area}	0.38fF/ μm^2
R_\square	1000
W	12 μm
C_w	10fF

For the last two parameters, a resistor width of 12 μm was chosen based on layout considerations, and laser trimmable 10fF capacitors (effectively dominating C_w) were added to each collector node to provide an option for post-fabrication trimming. Although trimming was not used, this capacitance is included in the design by lumping it with the wiring capacitance.

Substitution of the parameters of Table 6.1 into equation 6.8 results in $R_L = 350\Omega$. A simulation of the oscillator with this load resistance (including resistor layout parasitics) results in a free-running frequency of 3.22GHz. Using the simulator to manually fine-tune the 12 μm wide resistor such that $f_o = 3.125\text{GHz}$ results in a final value of $R_L = 380\Omega$, which correlates reasonably well with the hand analysis. The bias current was also increased slightly to 213 μA per transistor (i.e., +6.5%) to add margin for process variations.

The oscillator's amplitude can now be approximated using equation 3.23 by first substituting,

$$|\alpha_F| \equiv \left| \frac{\omega_T}{\omega_T + j\omega} \right| \cong \frac{f_T}{\sqrt{(f_T)^2 + (f_c)^2}} = \frac{16.5\text{GHz}}{\sqrt{(16.5\text{GHz})^2 + (3.125\text{GHz})^2}} = 0.983 \quad , \quad (6.11)$$

from equation 2.1 (where f_T is appropriate for a 213 μA bias) and by setting the oscillation frequency (ω_i) equal to the dominant pole frequency (ω_{p1})

$$E = \frac{\left(\frac{2\alpha_F I_{ee}}{\pi} \right) 2R_L}{\sqrt{1 + \left(\frac{\omega_i}{\omega_{p1}} \right)^2}} = \frac{\left(\frac{2(0.983)(2(213)\mu\text{A})}{\pi} \right) 2(380)}{\sqrt{1 + (1)^2}} = 143\text{mV} \quad (\text{peak differential}) \quad . \quad (6.12)$$

Table 6.2: Amplitude simulated and approximated values

Frequency in GHz	Simulated Amplitude (mV peak diff.)	Using Eq. (6.12) nominal $f_T = 16.5\text{ GHz}$ (mV peak diff.)	Using Eq. (6.12) fitted $f_{p2} = \omega_{p2}/(2\pi) = 7.94\text{ GHz}$ (mV peak diff.)
2.5	148.8	159.1	150.1
2.75	141.6	152.6	142.3
3.125	130.9	143.2	130.9 (fit ω_{p2} for zero error here)
3.25	127.4	140.2	127.2
3.5	120.4	134.3	120.3
3.75	113.5	128.7	113.8
4.0	106.8	123.3	107.6

Table 6.2 compares the simulated oscillator amplitude to the amplitude obtained using equation 6.12 for $f_T = 16.5\text{GHz}$ and $f_T = 27.6\text{GHz}$. With the nominal selection of f_T , the calculated results are close to simulation but not quite exact. This is expected since the entire analysis of the oscillator is based on small-signal parameters such as f_T and β , in a circuit operating in the large-signal regime. The transistors for example, are being switched through

numerous operating regions during each cycle, and junction capacitances are not static as was assumed, but are dynamically changing as a function of voltage. The third column in Table 6.2 however, illustrates that very close correlation can be obtained to simulation over the entire useful range of the oscillator by adding a second pole ω_{p2} such that the correct amplitude is predicted by

$$E = \frac{\left(\frac{2\alpha_F I_{EE}}{\pi}\right) 2R_L}{\sqrt{1 + \left(\frac{\omega_i}{\omega_{p1}}\right)^2} \sqrt{1 + \left(\frac{\omega_i}{\omega_{p2}}\right)^2}}, \quad (6.13)$$

at the free-running frequency.

Even though ω_{p2} is not derived from transistor parameters, the fitted equation is of the correct form to provide an accurate approximation of the oscillator's output amplitude.

6.2.2 Equivalent Injection-Load Network

In the free-running frequency calculation of equation 6.8, it was assumed that the parasitic loading of the collector node in each stage of the ring is identical. With nothing connected to the terminals labeled f_{in} in Figure 6.4 this is true, but in the actual IC however, these nodes do in fact connect to an emitter-follower stage (included in the block diagram of Figure 6.1, and shown schematically in Figure 2.7).

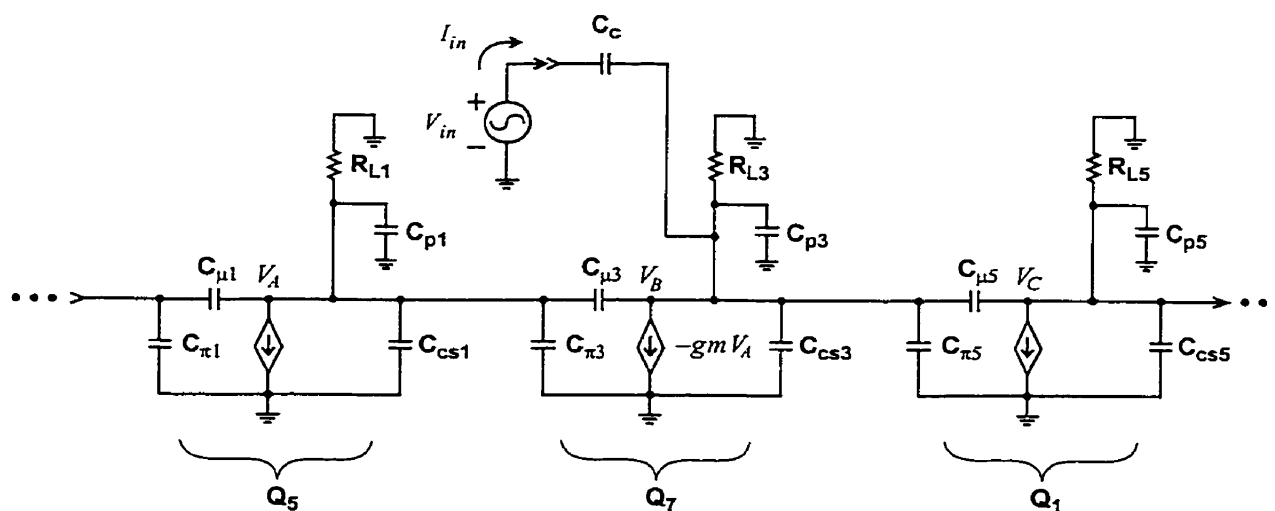


Figure 6.8: Half-circuit showing input signal injection source (V_{in}) and coupling capacitor (C_c).

Figure 6.8 illustrates the half-circuit view of the oscillator with an injection source (V_{in}) and coupling capacitor (C_c).

If V_{in} has the same amplitude, frequency and phase as V_B , ideally no current would flow through the coupling capacitor C_c , and the oscillator would not be aware that an injected signal is present. Now consider what happens when the input signal's frequency, phase, or amplitude is altered.

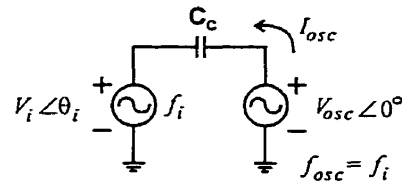


Figure 6.9: Injected signal V_i coupled to the locked oscillator.

Figure 6.9 illustrates the injection network consisting of source V_i and coupling cap C_c with the locked oscillator replaced by the test source (V_{osc}). The equivalent admittance as seen by the oscillator looking towards the coupling cap is calculated by determining $\frac{I_{osc}}{V_{osc}}$. The frequency of the oscillator is set to the frequency of the injection source (f_i) since we are assuming the oscillator is locked, and the phase of the input voltage (θ_i) is referred to the phase of V_{osc} (which, in Figure 6.8, would be the phase of node voltage V_B).

The test current can be expressed as,

$$I_{osc} = \frac{(V_{osc} - V_i(\cos\theta_i + j\sin\theta_i))}{\frac{1}{(j2\pi f_i C_c)}}, \quad (6.14)$$

which simplifies to an admittance equation given by,

$$\frac{I_{osc}}{V_{osc}} = 2\pi f_i C_c \left(\frac{V_i}{V_{osc}} \right) \sin\theta_i + j2\pi f_i C_c \left(1 - \left(\frac{V_i}{V_{osc}} \right) \cos\theta_i \right). \quad (6.15)$$

The real and imaginary terms of equation 6.5 can be identified as a shunt-parallel combination of a capacitance and a resistance (as illustrated in Figure 6.10).

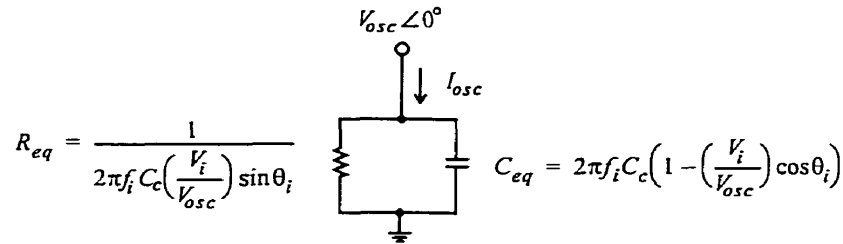


Figure 6.10: Equivalent injection loading network as seen by the oscillator

This implies that the injection source and coupling cap can be replaced by an equivalent parallel RC network if the amplitude and phase of the voltage across the coupling capacitor C_c is known.

It is important to realize that the equivalent resistance or capacitance (R_{eq} or C_{eq}) can become negative valued as the phase of the input and or the ratio of the injection amplitude to the oscillator's amplitude changes. A negative resistance is necessary to account for situations where the injecting source is delivering real power to the oscillator, and a negative capacitance, or essentially an inductance, can result if the injected current leads the oscillator's voltage.

By substituting the equivalent RC network in place of the injection source and coupling cap in Figure 6.8, a new RC product is obtained for the collector node of Q_7 .

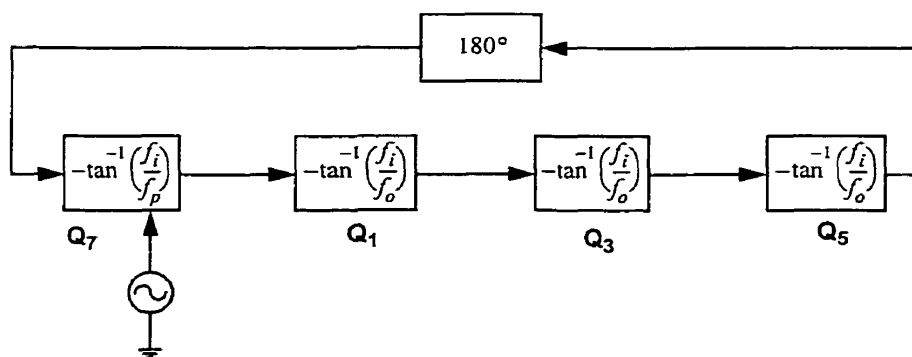


Figure 6.11: Injection locked oscillator phase delays (half-circuit view).

Figure 6.11 illustrates a block diagram representation of the phase shifts through the oscillator half circuit. The phase shift from stage to stage is approximated by a single pole at

f_o (the original free-running frequency), except for the pole of transistor Q_7 which is represented by the “variable pole frequency” (f_p).

The variable pole frequency can be written by summing the total shunt R and C parasitics at the collector of Q_7 and using the equation,

$$f_p = \frac{1}{2\pi R_{Total} C_{Total}} = \frac{1}{2\pi \left(\frac{1}{\frac{1}{R_L} + 2\pi f_i C_c \left(\frac{V_i}{V_{osc}} \right) \sin \theta_i} \right) \left(C_T + 2\pi f_i C_c \left(1 - \left(\frac{V_i}{V_{osc}} \right) \cos \theta_i \right) \right)}, \quad (6.16)$$

where C_T and R_L are the nominal pole components calculated in equations 6.6 and 6.7 respectively. In order to simplify the analysis, it is assumed that the circuit in Figure 6.7 remains a sufficient approximation for the effect of C_μ , even though the phase of the voltages across C_μ will deviate from 225° at frequencies other than f_o .

Employing the Barkhausen criteria for oscillation in Figure 6.11, the phase shifts around the loop are summed and set equal to 0° ,

$$0^\circ = 180 - \text{atan}\left(\frac{f_i}{f_p}\right) - 3 \text{atan}\left(\frac{f_i}{f_o}\right). \quad (6.17)$$

Solving (6.17) for f_p gives,

$$f_p = \frac{(f_i/f_o)}{\tan\left(3 \text{atan}\left(\frac{f_i}{f_o}\right)\right)} \quad (6.18)$$

Equation 6.18 essentially determines what the variable pole frequency of stage Q_7 must be in order to make the oscillator run at a frequency f_i , given that the dominant pole frequency of all other stages remains at f_o and the Barkhausen criteria is satisfied. This relation is plotted in Figure 6.7.

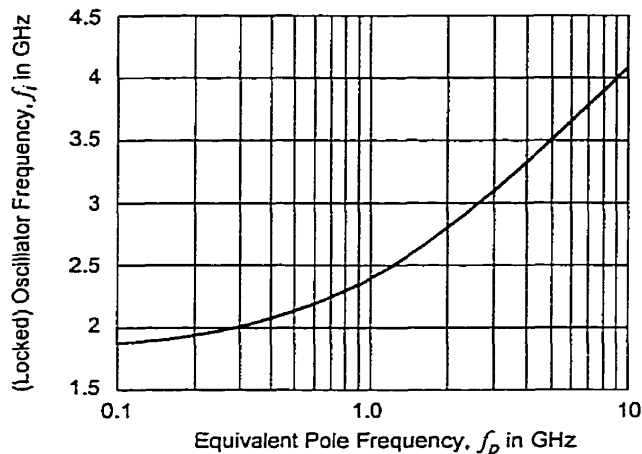


Figure 6.12: Oscillator frequency as a function of the equivalent pole frequency f_p

As expected, the plot shows that the frequency of the oscillator is 3.125GHz only when the variable pole frequency is set to 3.125GHz (the original free-running frequency of the oscillator). It is interesting to note the large range in frequency over which the effective pole frequency of Q_7 must move in order to shift the frequency of the oscillator by an octave (from 2 to 4GHz).

Subtracting equations 6.18 from 6.16 gives,

$$0 = \frac{1}{2\pi \left(\frac{1}{R_L} + 2\pi f_i C_c \left(\frac{V_i}{V_{osc}} \right) \sin\theta_i \right)} \left(C_T + 2\pi f_i C_c \left(1 - \left(\frac{V_i}{V_{osc}} \right) \cos\theta_i \right) \right) - \frac{(f_i/f_o)}{\tan\left(3 \operatorname{atan}\left(\frac{f_i}{f_o}\right)\right)}, \quad (6.19)$$

from which the phase of the input voltage (θ_i) can be determined as a function of input frequency (f_i) and ratio of input-to-oscillator voltage (V_i/V_{osc}). Although an explicit solution for θ_i does not exist, one is able to solve the function numerically using Taylor series approximations for the sine and cosine functions. By substituting equation 6.12 for V_{osc} into equation 6.19, θ_i is solved as a function of injection-locked frequency f_i , for various amplitudes of injection voltage. The results are plotted in Figure 6.13 for comparison with simulated results.

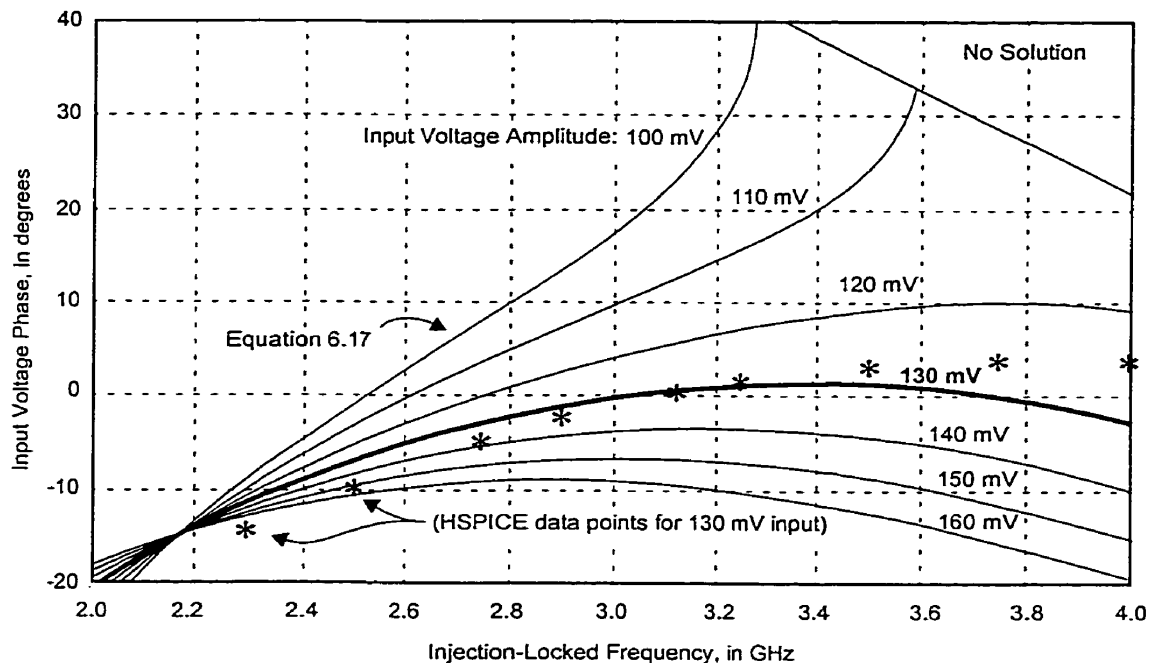


Figure 6.13: Input voltage phase versus frequency for various input amplitudes.

Figure 6.13 compares HSPICE simulated data points against a set of curves obtained from equation 6.19. The correlation obtained suggests that thinking about the injection source as a variable RC load has some intuitive merit in the design process, but that the simplified analysis of the oscillator with an equivalent pole frequency is not sufficiently accurate to be used as a tool in the design of the LO system. For this reason, the simulator is heavily depended upon to correctly optimize the various parameters of the design.

Table 6.3: Circuit design parameters for the 4-stage doubler in Figure 6.4 (2.2 Volt supply).

Parameter	Value	Design Comment
I_C	213 μ A	(426 μ A per diff-pair)
Transistor f_T	16 GHz	
Oscillator Power Dissipation	3.75mW	
Buffer Power Dissipation	2.97mW	(Buffer topology shown in Figure 6.2)
Frec-Running Frequency	3.125 GHz	
Locking Range	1.8-3.8 GHz	From a 130 mV peak differential input voltage.
Fundamental Oscillator Amplitude	130 mV peak differential	
Doubled Frequency Amplitude	40 mV peak differential	Amplitude prior to buffering stage.
C_c	600fF	Designed as large as possible without too big of a layout.
R_7 - R_8	380 Ω , 21 fF	
R_9 - R_{12}	1 k Ω , 14 fF	Value is not critical but capacitance is minimized.
R_{w1} - R_{w8}	0 Ω (nominally), 11 Ω (if cut in), 10 fF (nominally), 0 fF (if cut away).	These are <u>shorted</u> resistors (not shown in the schematic) which are placed in series with each of R_7 - R_8 as a laser trimmable option to either reduce capacitance by 10fF (by cutting them away) or to increase R_L by 11 Ω (by opening the short).
R_{13} - R_{16}	350 Ω , 10 fF	Current source degenerating resistors.
Q_1 - Q_{12}	0.5 x 5.0 μ m ²	

The final design parameters for the first doubler are shown above in Table 6.3. The locking range predicted by the simulator for the circuit is 1.8-3.8 GHz which provides approximately -20% and +17% margin over the required 2.5-3.25 GHz range.

6.3 Second Frequency Doubling Stage

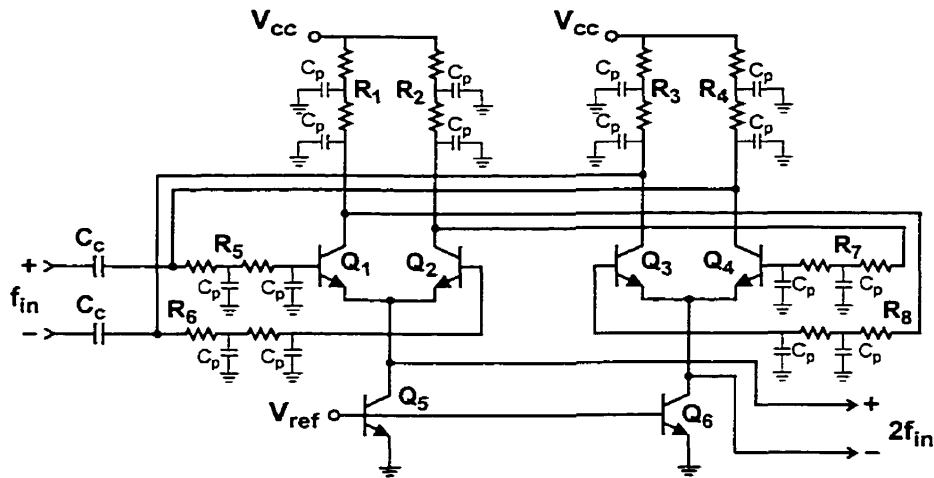


Figure 6.14: 2-stage ring: (second) frequency doubler

Figure 6.14 shows the schematic diagram of the second frequency doubler in the LO system. The function of this circuit is to take the 4.5-6.5 GHz (f_{LO}) output from the first doubling stage and double it to 9-13 GHz (or $2f_{LO}$). Since the free-running frequency of this stage is twice that of the 4-Stage ring (i.e., 6.25 GHz), a 2-stage ring is naturally suited to the design.

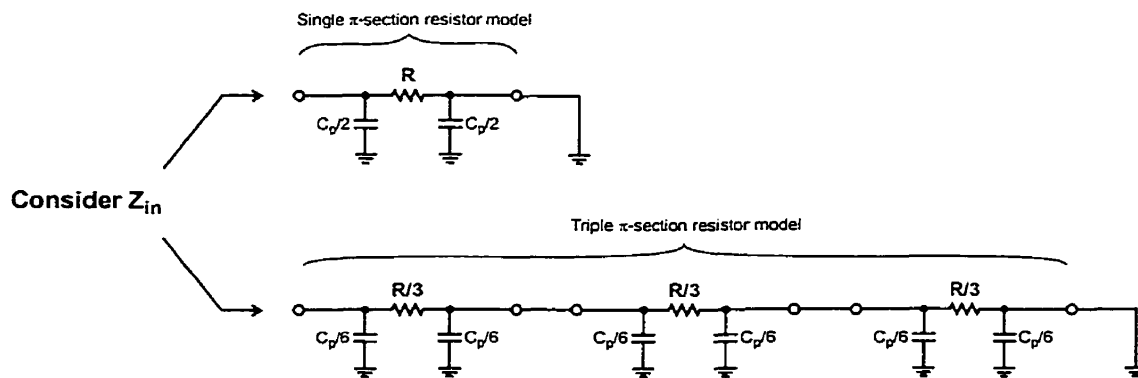


Figure 6.15: Single versus triple p-section resistor model.

In order to accurately simulate the behaviour of the oscillator, the parasitic capacitance of the poly-silicon resistors R_1 - R_8 must be included in the design. The single π -section model

shown in Figure 6.15 is the default model provided by the NT25 design kit for modeling the layout parasitics of a resistor.

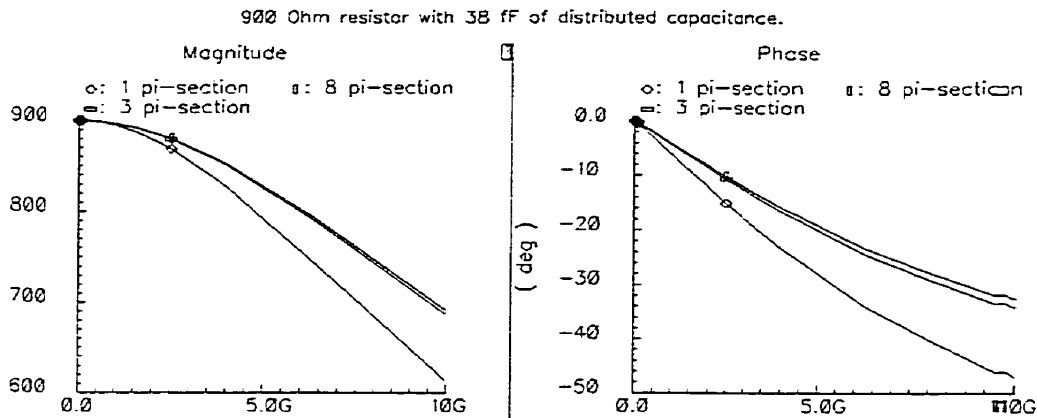


Figure 6.16: Comparison of a 1, 3, and 8 π -sectioned resistor model for a 900 Ohm, 38fF layout.

Figure 6.16 illustrates the magnitude and phase of the impedance looking into a 900 Ω (38fF parasitic capacitance), 13 x 11.7 μm^2 resistor over the range of 1 to 10 GHz (with one end grounded). This is the resistance value and size chosen for R_1 - R_4 in the oscillator, and defines the most sensitive time constant in the LO system. The impedance curves clearly show that simulation accuracy is dramatically improved by using a 3- π model over a 1- π model, and that only an incremental improvement is obtained by extending the model to 8- π sections. All critical resistances in the oscillator are therefore simulated with triple π -section resistor models.

A new element in the design of this oscillator is the use of resistors R_5 - R_8 in series with the base nodes of each transistor. These resistors and their associated parasitic capacitances are employed as phase shifting elements to create a high-frequency non-dominant pole. This non-dominant pole plays the role of the second pole frequency in the Simulink model of Figure 3.5 and is adjusted to set the free-running frequency of the oscillator. The dominant pole is controlled by the selection of R_1 - R_4 and this pole primarily affects the amplitude of the oscillator.

The design of this stage proceeds by attempting an aggressively-low f_T biasing target such as $\frac{f_T}{f_{RF}} = 3.25$ (or $f_T = 21$ GHz), resulting in $I_C = 615\mu\text{A}$ from the f_T curve of Figure 2.9.

If the bias current is set too low, the loop gain of the oscillator can drop below unity and the oscillation will not occur. Since the loop gain is also dependent on parameters other than bias current, designing the amplifier stages for maximum voltage gain will effectively minimize the bias current required for sustained oscillation. The voltage gain is approximated from equation 3.23 as

$$E = \frac{\left(\frac{2\alpha_F I_{EE}}{\pi}\right) \cdot 2R_L}{\sqrt{1 + \left(\frac{\omega_{ini}}{\omega_{p1}}\right)^2}},$$

which implies that the voltage gain can be raised by increasing R_L and ω_{p1} . The maximum value for R_L (or R_1 - R_4 in this case) is determined by voltage headroom constraints. In order to maximize the voltage drop available, emitter degeneration in the current-source transistors (Q_5 - Q_6) is not used. In layout, these devices are placed very close together and immediately adjacent to the mirroring device (not shown) which generates V_{ref} , thus preventing current mismatches. The base-emitter junction voltage (V_{be}) in this technology is approximately 0.825 V, so if a collector-emitter voltage equal to V_{be} is allotted to Q_5 - Q_6 and the same for Q_1 - Q_4 , then the maximum load resistance possible (i.e., R_1 - R_4) is determined by,

$$R_L = \frac{2.2V - 2(0.825)}{615\mu A} = 894\Omega. \quad (6.20)$$

The dominant pole frequency ω_{p1} is raised as high as possible by minimizing the parasitic capacitance of R_1 - R_4 (i.e., by minimizing the resistor area). The trade-off here is that as the area of a resistor is decreased, its process variation grows. Simulation is used here to determine the maximum resistance variation which can be tolerated, thus yielding the minimum allowable area for the device. Simulation is also used to optimize the value of R_5 - R_8 with similar goals of minimizing capacitive loading while correctly setting the free-running frequency of the oscillator.

Table 6.4: Circuit design parameters for the 2-stage doubler in Figure 6.14 (2.2 Volt supply).

Parameter	Value	Design Comment
I_C	616 μ A	(1.23mA per diff-pair).
Transistor f_T	21.5 GHz	Sub-maximum f_T used to minimize power dissipation.
Power Dissipation	5.42mW	
Free-Running Frequency	6.25 GHz	
Locking Range	3.8-7.2 GHz	Embedded in the LO system.
Fundamental Oscillator Amplitude	145 mV peak differential	@ 5.5 GHz
Doubled Frequency Amplitude	49 mV peak differential	@ 5.5 GHz
C_c	600fF	
R_1 - R_4	900 Ω , 38 fF	
R_5 - R_8	22 Ω , 35.2 fF	
R_{w5} - R_{w8}	0 Ω (nominally), 30 Ω (if cut in), 24 fF (nominally), 0 fF (if cut away).	These trimming resistors (not shown explicitly in the schematic) are placed in series with each of R_5 - R_8 . Trimming was not required.
Q_1 - Q_6	0.5 x 5.0 μ m ²	

Table 6.4 summarizes the design parameters of this oscillator. The locking range is 3.8-7.2 GHz which represents a -15% and +11% margin over the required 4.5-6.5 GHz range.

6.4 Quadrature Signal Generator / Frequency Halver

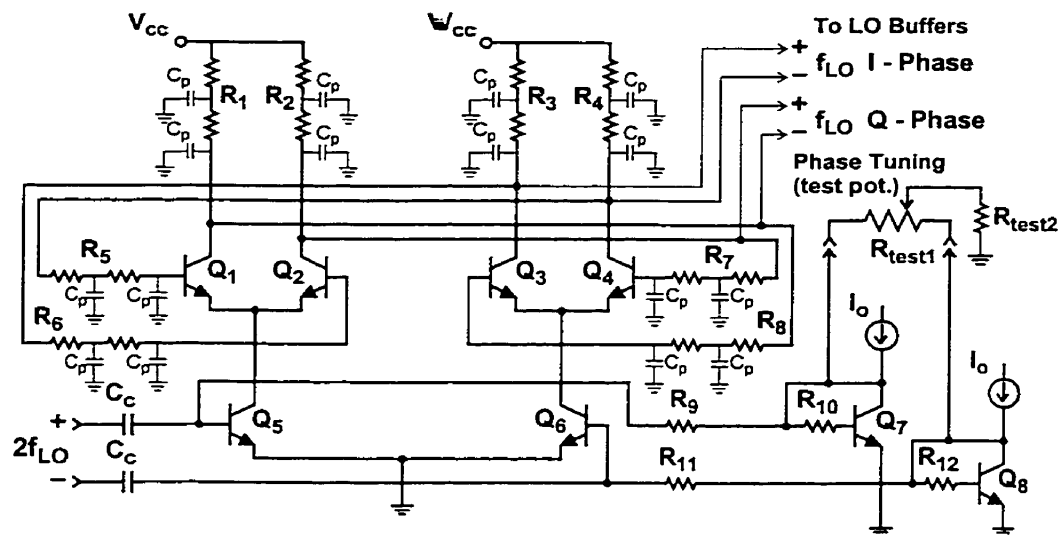


Figure 6.17: 2-Stage Ring: Frequency Halver / I-Q Signal Generator with Phase Tuning

Figure 6.17 shows the schematic diagram of the frequency halver used to generate the I and Q LO signals. Differential pair Q_5 - Q_6 convert the $2f_{LO}$ input voltage to a differential current which synchronizes the fundamental frequency of the oscillator. The input pair provide reverse isolation to prevent the divider from injection locking the preceding stage, and resistors R_9 and R_{11} isolate the RF signal from bias transistors Q_7 and Q_8 . The halver's I and Q (f_{LO}) outputs are buffered by simple amplifiers (of the topology of Figure 6.2) and then capacitively coupled to the inputs of the mixer quads (in Figure 2.6).

Phase tuning is afforded by differentially steering the bias currents of Q_5 and Q_6 . Note that the diode connected transistors Q_7 and Q_8 bias each amplifying stage of the halver independently. The bias currents through transistors Q_5 and Q_6 are therefore isolated from each other but are referred back to a common reference source (I_o). The simple potentiometer shown in Figure 6.17 illustrates how the bias currents can be altered to adjust the phase relationship between the I and (Q-LO) signals for test purposes. It is proposed that a simple current biasing D/A converter could provide a method for digital phase tuning control.

Table 6.5: Circuit design parameters for the frequency halver in Figure 6.17 (2.2 Volt supply).

Parameter	Value	Design Comment
I_C	616 μ A	(1.23mA per diff-pair).
Transistor f_T	21.5 GHz	Sub-maximum f_T used to minimize power dissipation.
Oscillator Power Dissipation	5.42mW	
Buffer Power Dissipation	4.78mW	(Buffer topology shown in Figure 6.2)
Free-Running Frequency	6.25 GHz	
Locking Range (output frequency)	3.8-6.5 GHz	Embedded in the LO system.
I-Q Output Amplitude (unloaded, i.e., no buffer connected)	190 mV peak differential	@ 5.5 GHz.
I-Q Output Amplitude (after buffering)	345 mV peak differential	The buffer also achieves current gain since its output is a low-impedance emitter-follower stage.
C_c	600fF	
R_1 - R_4	900 Ω , 38 fF	
R_5 - R_8	22 Ω , 35.2 fF	
R_9 - R_{10}	1 k Ω , 6 fF	Tolerance not important, minimized capacitance.
R_{11} - R_{12}	4 k Ω , 24 fF	same as above.
R_{w5} - R_{w8}	0 Ω (nominally), 30 Ω (if cut in), 24 fF (nominally), 0 fF (if cut away).	These trimming resistors (not shown explicitly in the schematic) are placed in series with each of R_5 - R_8 . Trimming was not required.
Q_1 - Q_8	0.5 x 5.0 μ m ²	

The design parameters of this oscillator are identical to the values given in Table 6.4 except for the addition of the bias-steering components R_9 - R_{12} and Q_7 - Q_8 which have no impact on the RF path. Performance of the phase tuning control is discussed in the chapter on test and measurement.

Recalling that the desired lock-range for the system is 4.5-6.5 GHz, simulations show that margin exists at the low end of the locking range but none at the high end (see Table 6.5). The centre frequency could have been raised, but simulations show that significant low end range is sacrificed to achieve a small gain in the top end margin and a higher overall power dissipation is necessary. This avenue was not pursued since an LO tuning range of 4.5-6.5 meets our requirements, and achieving 90% of this range is more than satisfactory for a 5-6 GHz receiver application.

6.5 Divide-by-2 Prescaler / Low Frequency Halver

The prescaler topology is identical to that of the frequency halver (as shown in Figure 6.17), except that the values of the components are altered so that the free-running frequency of the oscillator is $f_{LO}/4$ (or 1.56 GHz). The performance achieved by the prescaler is presented with the measured results in the next chapter.

6.6 LO System Design - Summary

Table 6.6: Summary of the simulated LO system performance.

Parameter	Value	Comment
Supply Voltage	2.2 V	
Total Power Dissipation	22.34 mW	(bias circuitry not included).
Locking Range	$f_{LO}/2$: 1.9-3.25 GHz or f_{LO} : 3.8-6.5 GHz	
LO output amplitude	345 mV peak differential	$< 1^\circ$ phase error.
Undesired LO Harmonic Suppression at the I-Q Output	> 35 dBc (differential $f_{LO}/2$ source) > 30 dBc (single-ended $f_{LO}/2$ source)	The IC can accommodate a single-ended or differential source for the $f_{LO}/2$ input.

Table 6.6 summarizes the key operating parameters of the LO system. The main challenge in the design of the system as a whole is to find the optimum amplitude and degree of coupling from stage to stage which achieves the desired locking range, while at the same time minimizing power dissipation and supply voltage. Manual circuit optimization using simulated results is a critical part of the design process since it is difficult to design each stage independently. Each oscillator's free-running frequency, locking range, amplitude and loop-gain is found to be highly dependent on the impedance, amplitude, and coupling from adjacent stages. A more rigorous approach to the hand analysis of coupled ILRO systems is left as a possible topic for future research work.

CHAPTER

7

Layout, Test and Measurement

This chapter discusses the layout of the IC, design of the test fixture, details of the test setup, and measurement results. In addition, conclusions about the phase precision of the tuning technique are drawn from measurements of image rejection and the phase noise of the LO system is inferred from phase noise measurements of the prescaler.

7.1 Layout

A photo-micrograph of the fabricated IC is shown in Figure 7.1 with the main circuit blocks annotated on the figure. Although the overall die size is $1.9 \times 1.2 \text{mm}^2$ (including the bond pads), the active area for the design is considerably smaller and can be reduced further by removing all test bond pads and laser trim options. Substrate coupling between the multiplier, divider, mixer and LNA circuits is minimized through component separation, separate supply bussing and the use of grounded p+ diffusion guard rings to isolate the various blocks. In addition, the use of fully differential RF, LO, and IF signal paths also helps to maximize sub-circuit isolation.

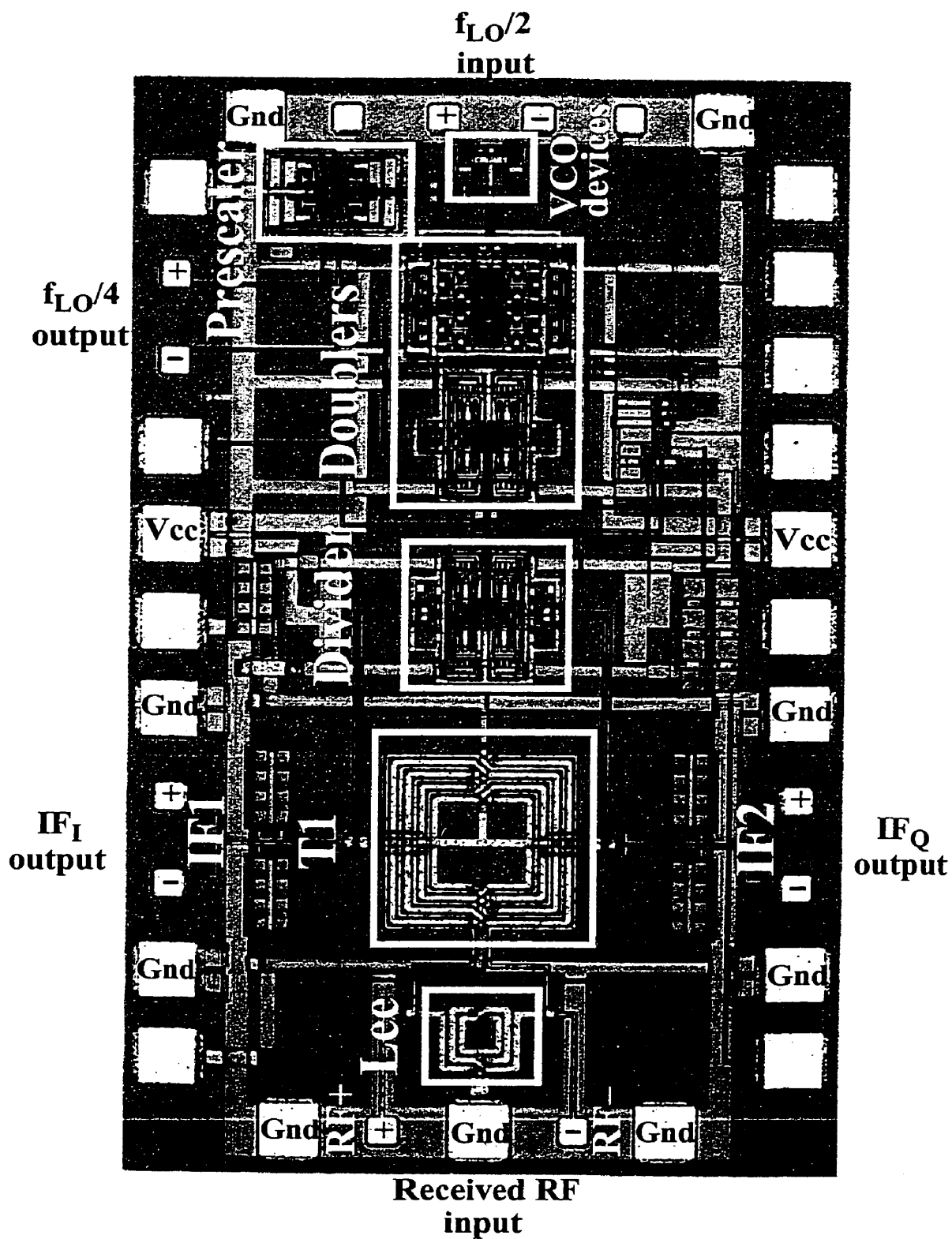


Figure 7.1: Photo-micrograph of the 5-6GHz receiver IC with regenerative LO system.

7.2 Test Fixture and Setup

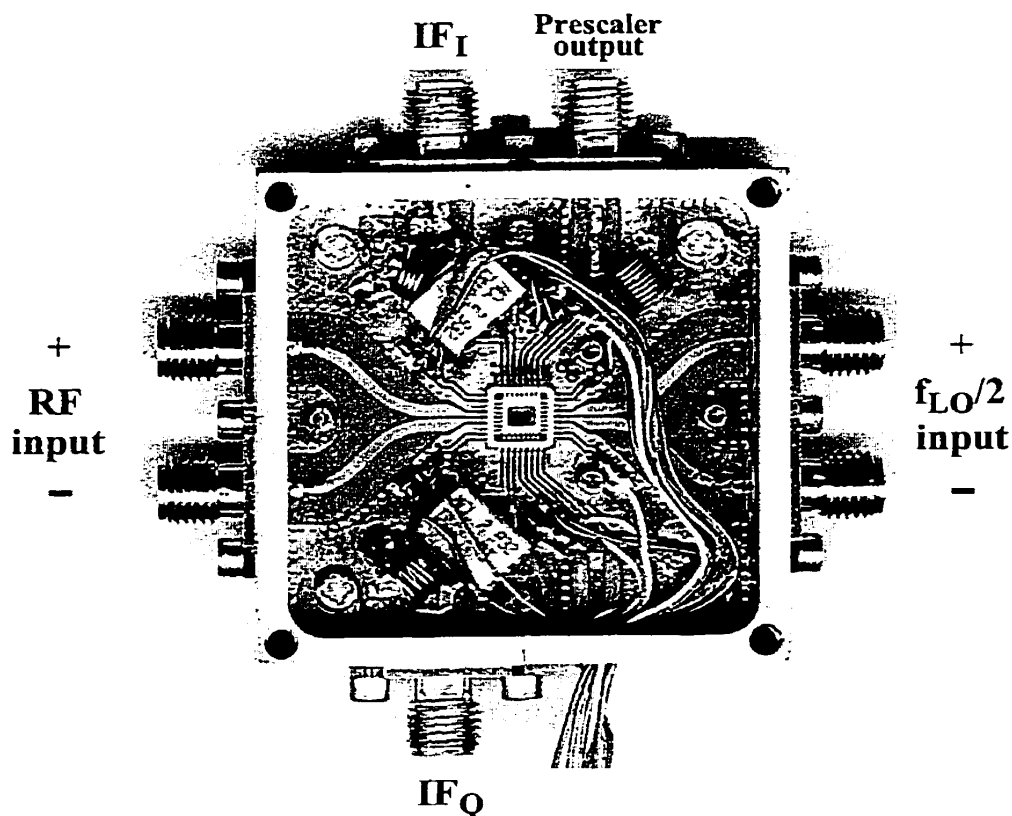


Figure 7.2: Test fixture created to evaluate the IC.

The test IC is packaged in a standard 32-pin ceramic quad flatpack (CQFP) and mounted in a custom designed test fixture for evaluation (shown in Figure 7.2). The printed circuit board layout and IF port matching networks of the fixture are designed using Hewlett Packard's Libra Series-IV circuit simulator.

As can be seen in the figure, the RF and LO signals are delivered differentially to the IC via 50 Ohm microstrip lines, where losses for the RF input signals (including connectors in the fixture) are approximately less than 1dB. The biasing lines are raised above the LO microstrip lines to prevent interference and are decoupled to ground using surface mount capacitors on the board.

Discrete IF transformers (or baluns) with a 4:1 turns ratio (seen as white cubes in the picture), are used to present a differential impedance of approximately 800 Ohms at the open-collector mixer outputs of the test-chip. The IF baluns have a minimum loss of 1.3dB at

75MHz, which degrades severely above 90MHz and prevents a higher IF from being used. To compensate for parasitic losses and mismatches, a three-element matching network was designed to match the balun's secondary winding to the 50 Ohm IF port impedance. Hand-wound inductors were found to have lower loss (i.e., a higher Q -factor) than commercially available discrete components.

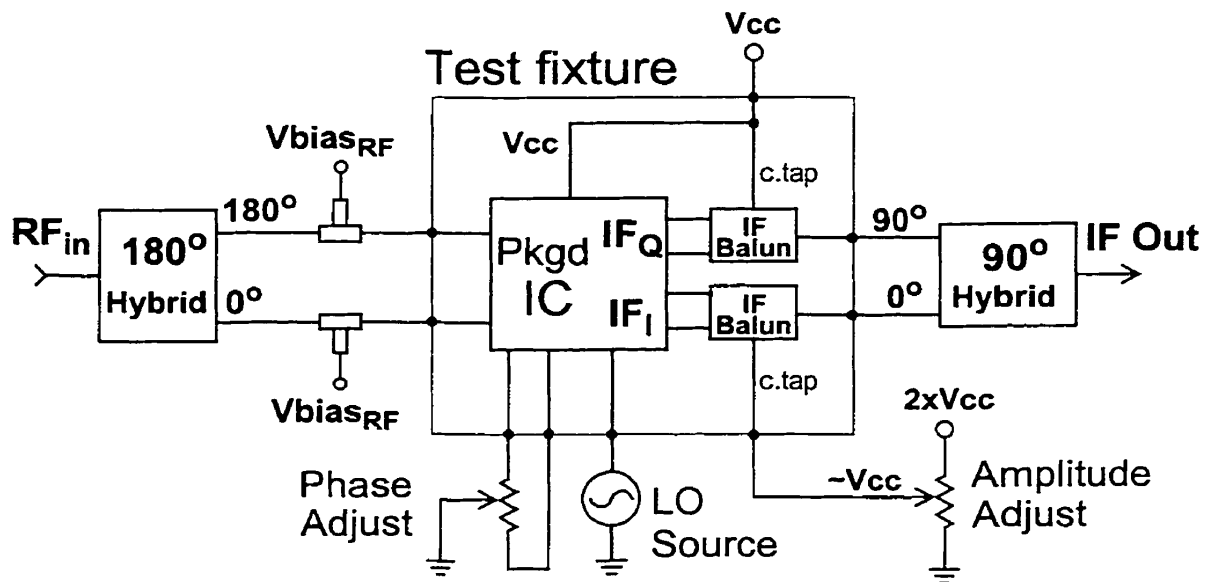


Figure 7.3: Test setup block diagram.

Figure 7.3 shows a block diagram of the test setup used to evaluate the IC. Simple potentiometers are used to adjust the relative amplitudes and phases of the I and Q IF output signals via the supply voltage of one of the mixers and the bias currents of the frequency halver respectively. These pots are manually tuned to maximize the image rejection.

It is proposed that in a real application, these controls could be set during a self-calibration period upon start-up or during idle times. A digital or analog tau-dither[45] type of feedback circuit could alternately adjust phase and amplitude controls to achieve maximum rejection of an internally generated, image test carrier. It is proposed that the test carrier be generated by the transceiver's up-converter, and that the received signal strength indicator (or

RSSI) found in most demodulator systems be used to measure the image-rejection during the calibration.

7.3 Measured LO System Performance

A summary of the measured LO system performance is presented in Table 7.1.

Table 7.1: Measured LO system performance.

Parameter	Value	Comment
Supply Voltage	2.2	Oscillators remain locked down to 1.8V but output level to mixers is degraded.
LO System Power Dissipation	22.4 mW	Not including optional prescaler.
Input ($f_{LO}/2$) Drive Level	-18 dBm to +10 dBm	LO system performance is insensitive to the input level over this range.
System Locking Range	Input $f_{LO}/2$: 1.9-3.2 GHz, or Output f_{LO} : 3.8-6.4 GHz	Represents a 51% relative locking range.
I-Q Phase Tuning Precision	< 0.01°	80 dB image-rejection measured.
Prescaler Lock Range	Input $f_{LO}/2$: 0.6-4.0 GHz Prescaler output ($f_{LO}/4$): 0.3-2.0 GHz	Range specified for a -6dBm input level to the IC.
Prescaler Power Dissipation	1.5 mW	1.5V supply
Prescaler Phase Noise Floor	< -140 dBc	With prescaler dissipating 4.3mW.

The LO system is observed to remain locked to a -18 dBm input (LO) signal source over the frequency range of 1.9-3.2 GHz, which in turn generates I and Q output signals for the mixers in the range from 3.8-6.4 GHz (representing a 51% relative locking bandwidth).

The measured power dissipation of the entire LO subsystem (excluding the optional LO prescaler) is 22.4 mW from a 2.2 V supply. This power dissipation does not include the bias circuitry which generated the reference voltages in each of the oscillators (i.e., V_{ref}) since the bias circuitry employed in this version of the IC was not designed to be power efficient but rather to provide flexibility during the testing phase. To avoid confusion, it should be noted that the IC presented in this thesis is an improved version of the one in reported in [19] (which achieved a smaller locking range, but which included the bias circuitry in its power dissipation totals).

The prescaler dissipates 1.5mW from a (minimum) 1.5V supply and remains locked over an input frequency range of 600MHz to 4.0GHz (for a -6dBm LO input signal to the IC). It should be noted that this type of regenerative divider does not have any other dominant modes of division (other than divide-by-2) and so unpredictable mode locking to unwanted harmonics is not a concern.

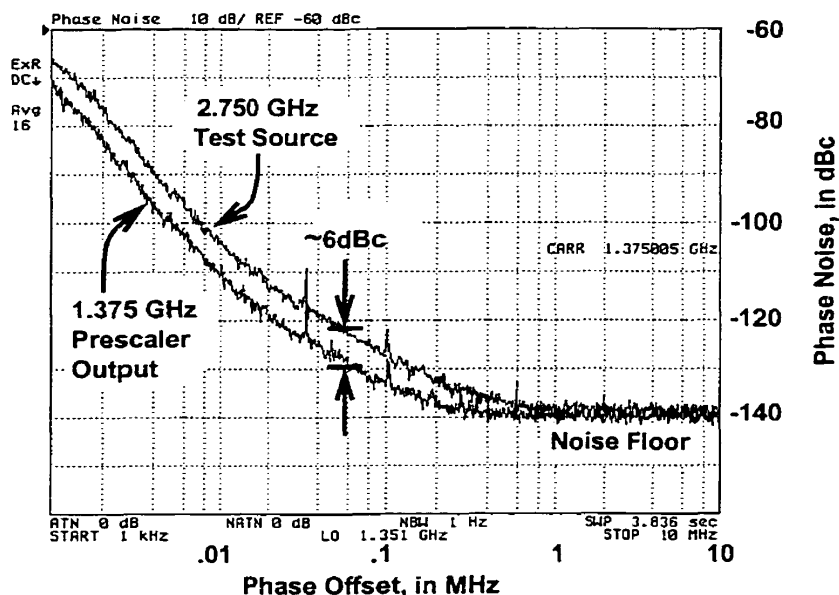


Figure 7.4: SSB phase noise of the prescaler output.

The single sideband phase noise of the prescaler output is plotted in Figure 7.4 for a supply voltage of 2.2V (and 4.3mW power dissipation). A high current bias is used for this measurement in order to be consistent with the bias conditions of the other injection-locked oscillators in the LO system. The output phase noise of the prescaler near the carrier is observed to nearly achieve the theoretical -6 dB noise power improvement expected from a divide-by-two function[20]. Far away from the carrier (i.e., at greater than 1 MHz offset), the phase noise of the prescaler is measured to be better than -140 dBc (which is the noise floor of the test setup) with no detectable spurious components. From this result, it is inferred that the phase noise of the I and Q outputs is approximately 6 dB worse than the phase noise of the $f_{LO}/2$ input source due to the net multiply by 2 function of the LO system (i.e., the reverse effect of an ideal divide-by-2). This follows from the observation that frequency halving in the

prescaler and frequency doubling in the LO chain are simply different methods of injection locking the same oscillator, and therefore similar phase noise performances are expected.

7.4 Measured Image-Rejection Performance

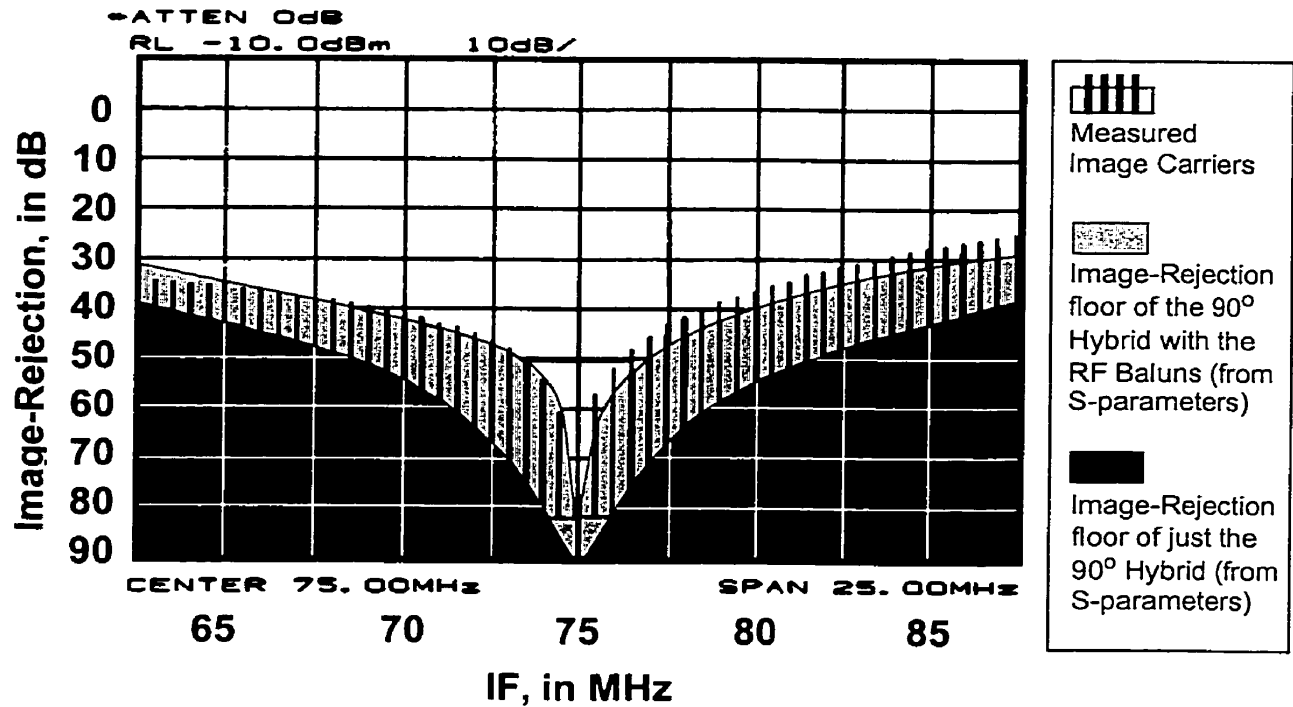


Figure 7.5: Wideband image rejection using a discrete quadrature hybrid.

The measured image rejection (IR) of the receiver over a ± 12.5 MHz frequency band using a discrete 90° quadrature IF combiner centred at 75MHz is plotted in Figure 7.5. The black-shaded IR floor (i.e., lower bound on image rejection) shows the lowest possible IR for the 90° external IF combiner employed in the test setup. This floor was calculated from s-parameter measurements of the combiner which characterize its frequency dependent phase and amplitude variations. Prior to computing the maximum IR, systematic phase and amplitude offset errors are subtracted from the measured parameters to centre the maximum rejection at 75MHz, thereby simulating an ideal trim of phase and amplitude errors. The grey-shaded region in Figure 7.5 shows the lowest possible image rejection when the s-parameters

of the IF combiner, transformer baluns, and matching stages are cascaded together. The vertical lines are actual measurements of the image suppression, showing the performance which was achieved experimentally.

A maximum image-rejection of approximately 80dB is obtained at the 75MHz centre frequency, which implies (from the curves of Figure 2.4b) that a phase tuning precision of better than 0.01° is achieved through adjusting the I-Q phase relationship via the frequency divider stage. The measured IR is also found to be within ± 5 dB of the maximum IR predicted for this test setup (i.e., the grey shaded region). Discrepancies between the measured and expected results are likely due to discrete component variations since the grey-shaded region is derived from the s-parameters of a single transformer balun and does not account for variations between the two IF baluns and the matching networks actually used in the test fixture.

A measurement of the image rejection was also performed with a constant IF of 75MHz. The purpose of this test is to measure the phase and amplitude variations of the I and Q LO outputs driving the mixers as a function of the LO frequency. In order to do this, the RF and LO frequencies are swept together across the 5-6GHz band, maintaining a constant frequency difference of 75MHz between them. The phase and amplitude of the LO is trimmed only once for maximum IR at the centre of the 5-6GHz band (i.e., 5.5GHz) prior to beginning the sweep.

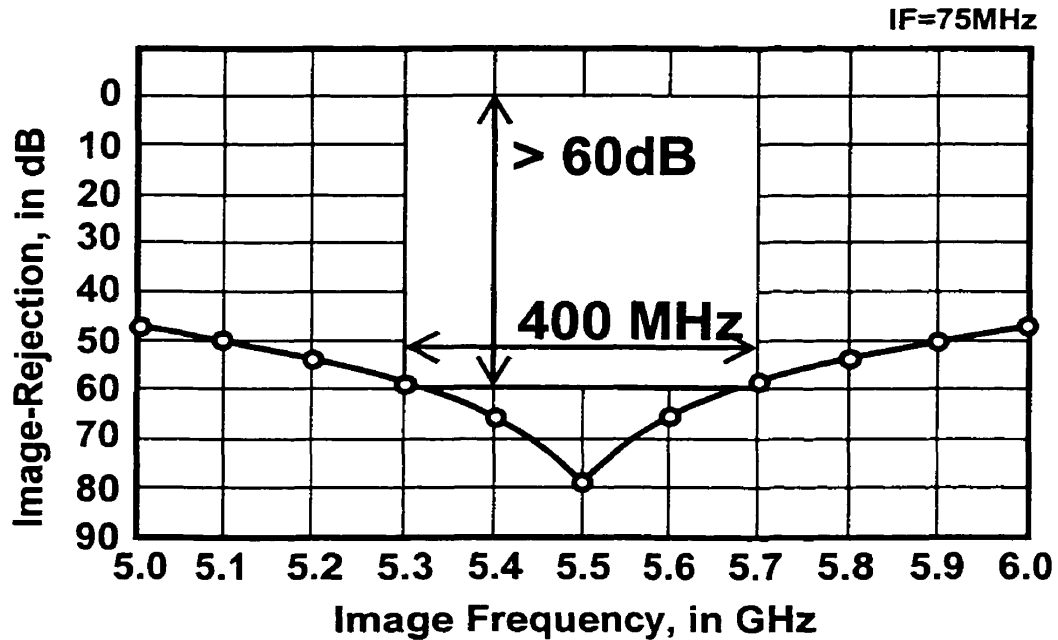


Figure 7.6: RF-LO sweep test.

Referring to Figure 7.6, as the test image frequency is swept away from the 5.5GHz IR-calibrated frequency, the image rejection degrades as a result of increasing phase and amplitude errors in the quadrature LO. Between 5.1-5.8GHz however, the image rejection is maintained at better than 50dB without re-tuning, which implies that the phase variations of the LO are less than 0.064° over a 1GHz sweep. In other words, if phase tuning used to set a specific phase relation between the I and Q outputs at a given LO frequency, then the frequency of the LO can be swept to other nearby frequencies without significantly altering the original quadrature phase relationship.

7.5 Overall Receiver Performance and Benchmark

Table 7.2: Measured Receiver Performance and Benchmark Comparison.

Parameter	Measured Performance		Ref. [46]	Ref. [47]	Ref. [18]	Ref. [27]
Technology f_T , GHz	25		20, (0.4 μ m BiCMOS)	45	45	(0.25 μ m CMOS)
RF input, GHz	5.3	5.8	5.1-5.4	5.15 - 5.35	5.8	5.25
LO input frequency, GHz	2.6875	2.9375	2.15 - 2.35	4.85 - 5.05	5.5	5.26
IF, MHz	75		400	300	250	10
Conversion Gain, dB	15.1	14.9 dB	18	11.7	14.2	8.7
RF input return loss, dB	14	14.6	-	8.6	(wafer probe)	-9.4
SSB Noise Figure (50 Ω), dB	5.1	5.1	7 (SSB?)	7.5 (DSB)	6.8	3
Input IP3, dBm	-9.43	-10.48	-16	-18.5	-5.9	-11.3
fundamental LO to RF isolation, dB	60	60.5	-	53.5	63	-60
Doubled LO to RF isolation, dB	75	74	-	no doubler	no doubler	no doubler
RF to IF isolation, dB	67	68	-	63.5	-	-
Supply Voltage, V	2.2		3.0	3.3	1.8	3.0
Power Dissipation, mW	44.37 (22 front end only)		55.5	122	18.5 (front end only)	114
Chip Area, mm ²	1.9 x 1.2		3.0 x 2.4 (TX and RX)	2.07 x 2.77	1.0 x 0.9 (LNA and mixers)	2.1 x 1.9
Image Rejection	> 80 dB (phase and amplitude balance tuned for maximum rejection at centre of IF)		off chip image reject filtering required.	21.3 (setup limited)	36.5	-

Table 7.2 compares the measured performance of this receiver to other image-reject receivers designed for operation in the 5-6GHz band. The IC presented in this work was measured to have an input return loss of greater than -14 dB and a minimum conversion gain of 15 dB

across the 5.3-5.8 GHz band. A relatively low overall single sideband noise figure of 5.1 dB was measured along with a third-order input intercept point (IIP_3) of -9.5 dBm, giving the receiver a wide dynamic range despite the low supply voltage (2.2V) and bias current (10mA) used for the LNA and mixers.

Also, a significant improvement in both gain and linearity of this receiver is realized when the supply voltage is raised from 2.2 to 2.34V. This is due to the larger LO signal drive presented to the mixer quads as a result of increased voltage headroom. At 2.34V, the conversion gain rises to 17dB and the IIP_3 improves by 5 dB to -4.5 dBm, while the noise figure is unchanged.

Measurement results of the receiver testchip compare very favorably with those reported for other 5-6GHz designs, as listed in the table. Careful attention to the design of the test fixture has played an important role in making accurate measurements of the receiver's performance.

CHAPTER

8

Conclusions

8.1 Summary and Conclusions

In this thesis, the design of a local oscillator sub-system for a monolithic 5-6 GHz band receiver was presented. The LO system was realized in a mature 25 GHz f_T bipolar technology and designed to operate from a 2.2 V supply. It consists of a pair of cascaded regenerative frequency doublers, a quadrature divider, and a prescaler to allow an external sub-2 GHz PLL synthesizer to be used with the IC.

The regenerative frequency doubling technique employed in the LO system uses an injection locked ring oscillator (ILRO) circuit to generate a differential and doubled frequency output. The doubling circuits were shown to remain locked over a wide operating range (of up to 50% of the oscillator's free-running frequency), and are able to multiply signals to frequencies in excess of $f_T/2$.

An ILRO based frequency halver (or quadrature signal generator) with a phase tuning control feature, was also implemented in the LO system design. An I-Q phase tuning precision of $< 0.01^\circ$ was measured and shown to remain static to within $< 0.064^\circ$ of an initially calibrated value over a 1 GHz frequency sweep (or ± 500 MHz deviation).

Measured results of the IC showed that excellent performance was achieved using the regenerative LO system concept and that the system is able to generate an accurate pair of phase-adjustable quadrature LO signals over the frequency range of 3.8-6.4GHz from an external 1.9-3.4GHz source.

The receiver design used to test this LO system realizes over 45 dB of image-rejection with a conversion gain of 15 dB and an IP_3 of -4.5 dBm. The power dissipation of the complete receiver IC was 44.4mW from a 2.2V supply.

8.2 Future Work

There are numerous avenues for future work on injection locked ring oscillator circuits. A few variations on frequency doublers were already suggested at the end of Chapter 4. One idea which would merit further investigation is the design of a multi-band LO system. In an application where radio operation is needed over multiple frequency bands, an LO system with the capability to bypass or add doubling stages could allow the generation of quadrature LO signals over octaves of frequency range without the need to have multiple VCO designs in an IC. In a CMOS process, digitally switched capacitors or resistors could be used to re-tune the center frequency of the oscillators to the intended band. Since the locked oscillators would preserve the phase noise of the injecting source, the resistive losses of the MOS switches would not be a significant concern to the performance.

Appendix A

Adler's Theory of Injection Locking

The full mathematical analysis of a non-linear injection locked oscillator can be extremely complicated and many modern day microwave circuit simulators are evaluated by their ability to solve such systems. Fortunately, a very simple approach can be applied to the topology used in this thesis with sufficient accuracy to gain valuable insight into the operation and properties of an injection locked ring oscillator. The paper from which this theory is borrowed is famous for it's clarity of explanation and therefore much of the discussion below follows very closely to the style and presentation from that reference.

A.1 Adler's Theory of Injection Locking

In 1946, Robert Adler presented a simplified theory for describing the injection locked behaviour of a triode oscillator[38]. The relevant portion of his theory will be described here with reference to a FET based oscillator having a similar topology:

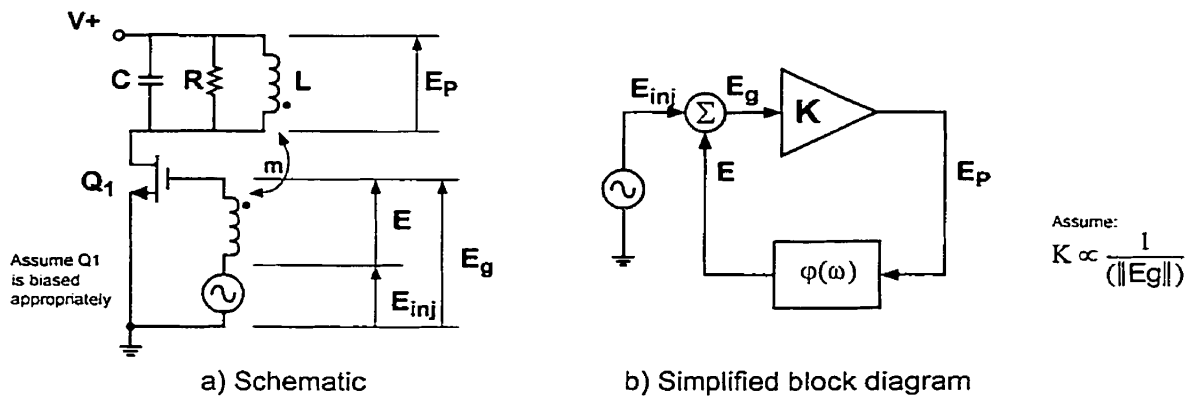


Figure A.1: Basic oscillator circuit

Voltages:

E_p = voltage across the tank
 E = voltage induced in the gate coil
 E_{inj} = voltage of injected signal
 E_g = resultant gate voltage
 Q = figure of merit of the tank L, C, R.

Angular Frequencies:

ω_o = free-running frequency
 ω_{inj} = frequency of injected signal
 $\Delta\omega_o$ = $\omega_o - \omega_{inj}$ = "undisturbed" beat frequency
 ω = instantaneous frequency of oscillation
 $\Delta\omega$ = $\omega - \omega_{inj}$ = instantaneous beat frequency

Figure A.1 shows a simplified schematic and block diagram of a FET oscillator circuit coupled to an external injection source (E_{inj}). In order to simplify the analysis, the following assumptions are made:

It will be assumed that the oscillator is memoryless, and that instantaneous phase and amplitude information can fully describe the state of the oscillator at any given point in time. The frequency of the externally injected signal will be relatively near the center of the pass band of the resonator such that,

$$\frac{\omega_o}{2Q} \gg \Delta\omega_o \quad (\text{A.1})$$

is satisfied. Since a linear system model is being used to describe the non-linear behaviour of an oscillator, it must also be assumed that the time constant of the amplitude limiting mechanism of the oscillator is short compared to one beat cycle, as defined by,

$$\tau_{limit} \ll \frac{1}{\Delta\omega_o} \quad (\text{A.2})$$

In addition we will further assume that the injected signal is weak compared to the oscillator so that the AM variations of E will also be small compared to E itself,

$$E_{inj} \ll E \quad (\text{A.3})$$

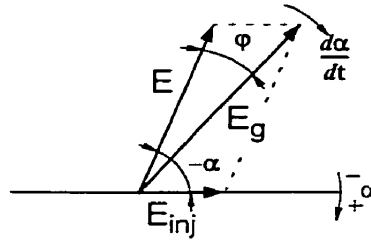


Figure A.2 Vector diagram of instantaneous voltages

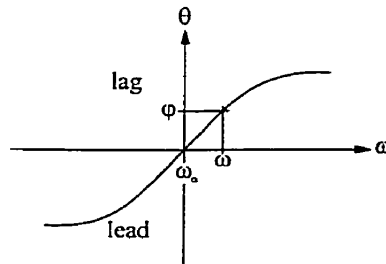


Figure A.3 Phase versus frequency for a simple tuned circuit

Let Figure A.2 be a vector representation of the voltages in the oscillator at a given instance. The injected signal E_{inj} is held stationary with respect to our eyes such that any other stationary vectors in the diagram also symbolize voltages of angular frequency ω_1 . A vector which is rotating in the diagram with an angular velocity of $\left(\frac{d\alpha}{dt}\right)$ represents an actual angular frequency of $\left(\frac{d\alpha}{dt}\right) + \omega_{inj}$, or an angular beat frequency of

$$\Delta\omega = \frac{d\alpha}{dt}. \quad (\text{A.4})$$

The vector diagram therefore shows both beat frequency and phase. It should also be noted that $\frac{d\alpha}{dt}$ is an instantaneous angular frequency which can vary during the synchronization process such that a complete beat cycle may never happen; the oscillator may become locked or synchronized first.

With no injected signal, $E_g = E$, and in this situation, that the feedback circuit can only return E in phase with E_p at one frequency, the free-running frequency ω_o . Figure A.3 shows a typical phase versus frequency curve for a single-tuned resonant circuit where the reference vector is the current through the tank and the phase being plotted is the resultant voltage (E_p) across it.

The loop in Figure A.1b is inherently unstable and thus oscillations begin to grow rapidly at the free-running frequency until amplitude limiting effects in the amplifier itself causes the gain of the loop decrease to unity. At this point the oscillator is stable in a cyclostationary sense and has a constant amplitude output. Now let an externally injected signal E_{inj} be introduced at frequency ω_1 to the oscillator. Assume Figure A.2 shows an accurate representation of the voltage vectors at a given instance in the beat cycle. Feedback vector E lags behind E_g by a phase angle ϕ which implies that the oscillator is no longer operating at its free-running frequency but actually exceeds ω_o by an amount which results in a phase shift of ϕ in the tank. A locked condition can exist only because the oscillator is able to adjust its phase relationship with respect to E_{inj} such that vector summation of E with E_{inj} causes the overall phase shift around the loop to once again be 360° ; just as it would have been without the injected signal and running at frequency ω_o .

The phase shift ϕ in Figure A.2 is a result of the summation element in Figure A.1b can be approximated by the equation,

$$\phi \cong \frac{E_{inj} \sin(-\alpha)}{E} = -\frac{E_{inj}}{E} \sin \alpha, \quad (\text{A.5})$$

(which is valid to within 4° for $|\alpha| \leq 50^\circ$ and $\frac{E_{inj}}{E} \leq 0.4$). Under the assumption of equation A.1, it can also be assumed that the locked oscillator will operate in the linear region of the ϕ versus ω curve with slope

$$A = \frac{d\phi}{d\omega}. \quad (\text{A.6})$$

Thus the phase angle for frequencies ω close to ω_o can be approximated by,

$$\varphi = A(\omega - \omega_o), \quad (\text{A.7})$$

which can also be expressed as,

$$\varphi = A(\omega - \omega_o) = A[(\omega - \omega_{inj}) - (\omega_o - \omega_{inj})] = A[\Delta\omega - \Delta\omega_o]. \quad (\text{A.8})$$

Subbing (A.5) on the left and (A.4) on the right, we have

$$-\frac{E_{inj}}{E} \sin \alpha = A \left[\frac{d\alpha}{dt} - \Delta\omega_o \right]. \quad (\text{A.9})$$

Using the substitution,

$$B = \frac{E_{inj}}{E} \cdot \frac{1}{A}, \quad (\text{A.9a})$$

results in,

$$\frac{d\alpha}{dt} = -B \sin \alpha + \Delta\omega_o. \quad (\text{A.9b})$$

Adding the injected frequency ω_{inj} to both sides, we can also state

$$\omega = -B \sin \alpha + \omega_o. \quad (\text{A.9c})$$

This equation suggests that the oscillator's instantaneous frequency is shifted from the oscillator's free-running frequency by an amount proportional to the sine of the angle between the oscillator and the injected signal (multiplied by the factors in B).

The phase shift in a single tuned resonator can be expressed as,

$$\tan \varphi = 2Q \frac{\omega - \omega_o}{\omega_o}, \quad (\text{A.10a})$$

which for small angles approximates to

$$\varphi = 2Q \frac{\omega - \omega_o}{\omega_o}. \quad (\text{A.10b})$$

Substitution into (A.6) gives,

$$A = \frac{2Q}{\omega_o}, \quad (\text{A.10c})$$

leading to,

$$B = \frac{E_{inj}}{E} \cdot \frac{\omega_o}{2Q}. \quad (\text{A.10d})$$

Equation (A.9b) can then be generalized for an oscillator with a single-tuned resonator as

$$\frac{d\alpha}{dt} = -\frac{E_{inj}}{E} \frac{\omega_o}{2Q} \sin\alpha + \Delta\omega_o \quad (\text{A.11})$$

An oscillator is said to be locked when the oscillator's phase is synchronized to that of the injection source such that their relative phases can be different, but not slipping with respect to one another; i.e. $\left(\frac{d\alpha}{dt}\right) = 0$ which means that all the vectors in Figure A.2 are stationary with respect to our reference E_{inj} . In a locked state then,

$$0 = -\frac{E_{inj}}{E} \frac{\omega_o}{2Q} \sin\alpha + \Delta\omega_o, \quad (\text{A.12a})$$

or,

$$\sin\alpha = 2Q \frac{E}{E_{inj}} \cdot \frac{\Delta\omega_o}{\omega_o}. \quad (\text{A.12b})$$

(A.12b) describes the stationary phase angle between the injected signal (E_{inj}) and the oscillator's voltage (E). Clearly, as the injected signal amplitude increases, the phase of the oscillator moves towards lining up with the injected signal (i.e., α decreases towards zero). Since $\sin\alpha$ can only assume values between +1 and -1, we can define the condition required for synchronization as

$$\left| 2Q \frac{E}{E_{inj}} \cdot \frac{\Delta\omega_o}{\omega_o} \right| < 1, \quad (\text{A.13a})$$

or,

$$\frac{E_{inj}}{E} > 2Q \left| \frac{\Delta\omega_o}{\omega_o} \right|. \quad (\text{A.13b})$$

For a more general type of oscillator, with a different type of resonator, the criteria for synchronization can be described as,

$$\frac{E_{inj}}{E} > |A\Delta\omega_o|, \quad (\text{A.13c})$$

where $A = (d\phi / d\omega)$ for the particular type of load employed. In this case, equation A.12b can also be written more generally as

$$\sin\alpha = \frac{E}{E_{inj}} A\Delta\omega_o. \quad (\text{A.14})$$

Using the above set of equations, the fundamental characteristics of many different types of injection locked oscillators can be quantified.

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