Radio Frequency Direct-Digital QPSK Modulators in CMOS Technology

by

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Abstract

In this thesis, novel direct-digital Quadrature Phase Shift Keying (QPSK) modulators are proposed in low-cost Complimentary Metal Oxide Semiconductor (CMOS) technology for radio frequency (RF) wireless applications. Direct-digital architectures have attracted much attention recently as they potentially offer significant cost savings and performance benefits. A new direct-digital QPSK modulator concept is introduced where the carrier is modulated directly by digital data using Pass-Transistor Logic (PTL) circuits for a small size and low power consumption. The concept is demonstrated through the design of an L-band modulator followed by an enhanced tunable S-band version.

The proposed L-band modulator first generates all four quadrature phases of the carrier by using a 90° resistor-capacitor, capacitor-resistor (RC-CR) phase shifter followed by two 180° active baluns. One signal from the in-phase components and another from the quadrature-phase components are later selected by two PTL circuits according to the in-phase (I) and quadrature-phase (Q) digital data respectively. Finally the chosen signals are subtracted by a differential amplifier. The circuit has been experimentally demonstrated in a standard 0.18μm CMOS process, showing good performance at 1.7GHz with the data transmission rate and carrier rejection exceeding 20Mbps and 40dB respectively. The integrated circuit (IC) measures only 425μm by 850μm and consumes less than 43mW of power.

A new S-band direct-digital QPSK modulator is introduced that offers even better performance and requires fewer components. An active balun first splits the carrier into a pair of balanced signals, which are then fed to a 90° RC polyphase network generating all four differential quadrature signals. Voltage-controlled NMOS resistors are used in the RC polyphase network to fine-tune it after fabrication for the lowest possible phase error. Finally, only one of the four differential quadrature signals is selected by a PTL circuit consisting of six NMOS switches, according to both I and Q digital data values. The circuit has been experimentally demonstrated in a standard 0.18μm CMOS process showing very good performance at 2.4GHz, with the data transmission rate exceeding 56Mbps. The IC measures 720μm by 888μm with an active area of only 505μm by 610μm, and consumes less than 33mW of power.

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List of Abbreviations and Symbols

AC	Alternate Current
ADS	Advanced Design System
ASK	Amplitude Shift Keying
BER	Bit Error Rate
BPF	Bandpass Filter
BPSK	Binary Phase Shift Keying
CG-CS	Common-Gate, Common-Source
CMOS	Complimentary Metal Oxide Semiconductor
CPW	Coplanar Waveguide
DC	Direct Current
DTC	Divide-by-Two Circuit
FET	Field-Effect Transistor
FSK	Frequency Shift Keying
gnd, GND	Ground
GPS	Global Positioning System
I	In-phase
IC	Integrated Circuit

IEEE	Institute of Electrical and Electronic Engineers
IF	Intermediate Frequency
ISI	Intersymbol Interference
LC	Inductor-Capacitor
LNA	Low Noise Amplifier
LO	Local Oscillator
MEMS	Microelectromechanical Systems
NF	Noise Figure
NRZ	Non-Return-to-Zero
PA	Power Amplifier
PRBS	Pseudo-Random Binary Sequence
PSK	Phase Shift Keying
PTL	Pass-Transistor Logic
Q	Quadrature-phase
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RC	Resistor-Capacitor
RC-CR	Resistor-Capacitor, Capacitor-Resistor
RF	Radio Frequency
SoC	System-on-Chip
SPDT	Single-Pole Double-Throw
TSMC	Taiwan Semiconductor Manufacturing Company
WLAN	Wireless Local Area Network

μ_n	Electron mobility
A_{RF}	RF carrier amplitude
A_v	Voltage conversion gain
BW	Null-to-null bandwidth
C	Capacitance
C_{cb}	Channel-to-body capacitance
C_{gc}	Gate-to-channel capacitance
C_{gd}	Gate-to-drain capacitance
C_{gs}	Gate-to-source capacitance
C_{jdb}	Drain-body junction capacitance
C_{jsb}	Source-body junction capacitance
C_{ov}	Overlap capacitance
C_{ox}	Gate oxide capacitance per unit area
E/N	Energy to noise ratio
E_s	Symbol energy
E_{sat}	Velocity saturation electric field
f_{MOD}	Modulation frequency
G	Amplitude ratio
g_m	Transconductance
I_D	Bias current
I_{DS}	Drain-to-source current
L	Inductance
L	FET length

L_D	Diffusion overlap length
L_{eff}	Effective channel length
Q	Quality factor
R	Resistance
R_b	Bit rate
R_{bias}	Biasing resistance
R_d	Drain resistor
R_{DS}	Switch on-resistance
R_G	Gate resistor
R_L	Load resistance
R_{NET}	Net switch on-resistance
R_s	Source resistor
T	Time period
T_b	Bit period
V_-	Negative voltage
V_+	Positive voltage
V_{DD}	Supply voltage
V_{DS}	Drain-to-source voltage
V_{GS}	Gate-to-source voltage
V_I	In-phase voltage
V_{in}	Input voltage
V_{LO}	LO voltage signal
V_{out}	Output voltage

V_Q	Quadrature-phase voltage
V_{QPSK}	QPSK output signal
V_{RL}	Voltage across load resistance
V_T	Threshold voltage
V_{TUNE}	Tuning Voltage
W	FET width
Z_0	System impedance
Z_{in}	Input impedance
θ	Phase difference
λ	Wavelength
ω_c	Cutoff frequency
ω_{RF}	RF carrier frequency

Chapter 1

Introduction

1.1 General Introduction

The demand for light and low-power wireless communications devices such as cellular phones, Wireless Local Area Networks (WLAN) and Global Positioning Systems (GPS) has been growing rapidly in recent years with a relentless push for higher speeds and increased functionality. Shown in Figure 1.1 is a block diagram of a typical digital wireless transceiver. It employs a duplexer to connect either the transmitter or receiver to the shared antenna. In the transmitter, data is modulated and upconverted to a radio frequency (RF) signal suitable for wireless transmission, where as in the receiver downconversion and demodulation are performed to retrieve the original digital data. For sufficient communication range, the transmitter usually includes an RF power amplifier (PA) to boost the transmitted signal to the required power level. A bandpass filter (BPF) is then used to remove any harmonics or spurious signals generated by the PA. Similarly, the receiver includes a BPF to remove unwanted signals followed by a low noise amplifier (LNA) to amplify the weak RF signal while adding as minimum noise as possible for reliable data detection.

The highly competitive market of personal communication products drives manufacturers to constantly reduce costs. One possible solution is to integrate the RF

front-end including the PA, LNA and up- and down-converters with digital circuits on the same chip. Not only does this reduce cost, but reliability and power consumption are also improved compared to using discrete components. Complimentary Metal Oxide Semiconductors (CMOS) has been the mainstream technology for digital circuits since the 1970s [1]. With continuous technology scaling and decreasing transistor gate length over time, CMOS has become a feasible means for analog applications extending to the millimeter-wave frequency range [2], [3]. Thus it is naturally suited for implementing monolithic system-on-chip (SoC) transceivers. However, as both digital and analog/RF portions of the transceiver are being closely packed on the same Integrated Circuit (IC), new device and circuit structures are needed [4].

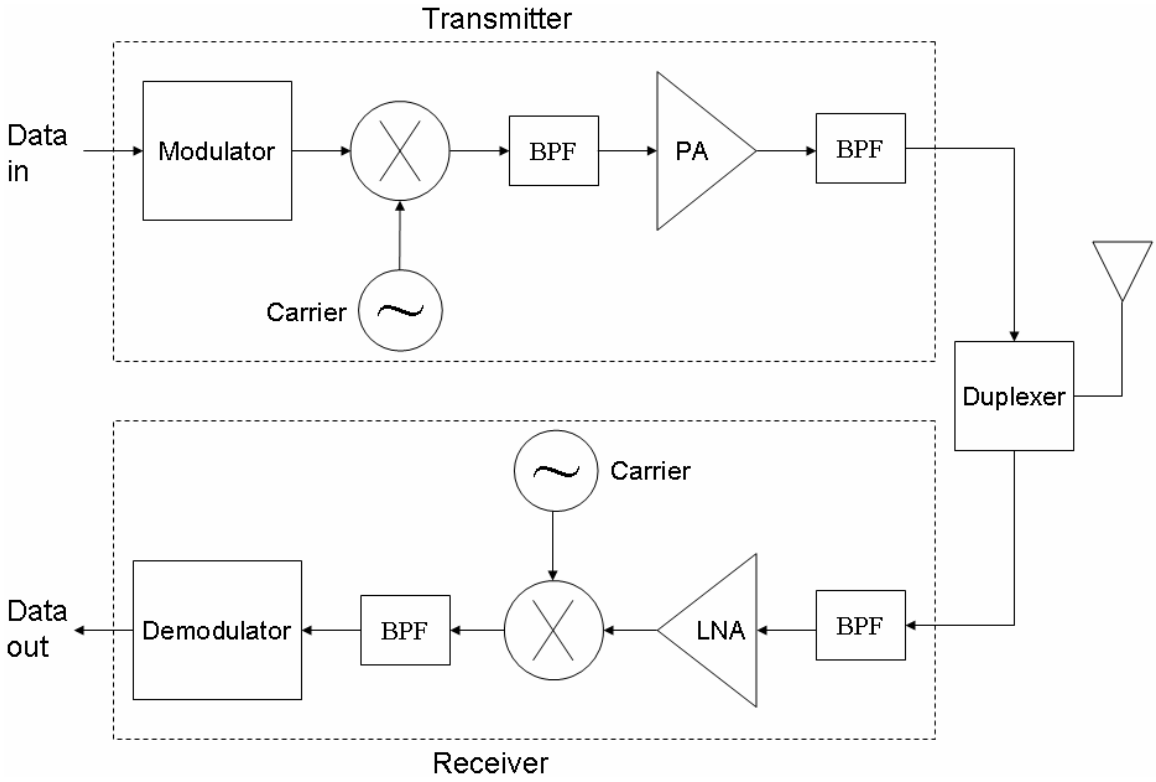

Figure 1.1: Block diagram of a typical wireless transceiver.

High-speed digital communications have flourished over the last few decades with modern wireless systems (e.g. IEEE 802.11a/g/n WLANs) employing complex vector modulation such as Quadrature Phase Shift Keying (QPSK) and Quadrature Amplitude Modulation (QAM) for increased bandwidth and spectrum efficiency. Such modulation schemes have been traditionally implemented using heterodyne modulators since it was difficult to design direct-digital RF modulators with adequate modulation accuracy for low bit error rates (BER) and reliable data transmission. However continuous scaling and developments in monolithic technologies such as CMOS make it now possible to realize direct-digital modulators with improved performance in terms of conversion efficiency and data throughput, potentially leading to new wireless standards in the future [5].

Direct-digital modulators have attracted much attention recently due to their significant advantages over their traditional heterodyne counterparts. Several components in the heterodyne architecture are not needed in a direct modulator including the intermediate frequency (IF) oscillator, IF bandpass filter and the RF upconverter. This greatly reduces the size of the system and facilitates integration with existing digital CMOS circuits. In addition, higher data transmission rates are possible since the modulation bandwidth is no longer limited by a relatively low IF frequency, as in heterodyne systems. However, having said that, direct-digital modulators and transmitters suffer from one important drawback: corruption of the carrier local oscillator (LO) by the power amplifier (PA) output through a mechanism widely known as “injection pulling” or “injection locking”. Such a problem can be alleviated nevertheless

by various shielding techniques to isolate the carrier LO or by offsetting the LO frequency [6].

In this thesis, novel direct-digital QPSK modulators are proposed with new RF components and circuits devised in low-cost CMOS technology. A new direct-digital QPSK modulator concept is introduced where the carrier is modulated directly by digital data using Pass-Transistor Logic (PTL) circuits. The main advantage of this approach is its relative simplicity in terms of size and power consumption compared to most other direct-digital QPSK modulators. The concept is demonstrated through the design of an L-band modulator that we first published in [7] followed by an enhanced tunable S-band version showing very good performance with high data transmission rates. These modulators offer compact yet effective solutions enabling high-speed and low-power data transmission for portable wireless applications. In particular:

- The L-band modulator circuit is experimentally demonstrated in 0.18μm CMOS process, showing good performance at 1.7GHz with the data transmission rate and carrier rejection exceeding 20Mbps and 40dB respectively. The IC measures only 425μm by 850μm and consumes less than 43mW from a 1.8V supply.
- The enhanced S-band modulator is also demonstrated in 0.18μm CMOS process showing very good performance at 2.4GHz. An accurate QPSK signal constellation was achieved after tuning the circuit, with the phase and amplitude errors being less than 1.4° and 0.3dB respectively. The supported data rates go well beyond 56Mbps, while the carrier rejection achieved is more than 32dB. The IC measures 720μm by 888μm with an active area of only 505μm by 610μm, and consumes less than 33mW from a 1.8V supply.

1.2 Thesis Organization

The thesis is organized as follows:

Chapter 2 explores direct-digital modulation and its benefits over traditional heterodyne architectures. It also reviews the QPSK modulation scheme, outlining its main characteristics such as signal constellation and power spectral density. A literature review of recently published work on direct QPSK modulators is performed next. As the performance of a direct quadrature modulator strongly depends on the accuracy of obtaining a 90° phase shift, commonly reported techniques to design an accurate 90° phase shifter are studied. Finally, widely used methods for modulating the quadrature carriers are discussed with a summary of their advantages and drawbacks.

Chapter 3 introduces and discusses the new QPSK modulator concept. It later describes the design of an L-band direct-digital QPSK modulator in CMOS that demonstrates this new concept. The components involved are analyzed in detail while stressing their important design considerations. This includes an investigation of commonly used circuit techniques for implementing the baluns and summing junctions required by the modulator, followed by the design of new circuits applicable to our needs. The chapter concludes with simulations and measurement results of the fabricated IC.

An enhanced version of the direct-digital QPSK modulator for S-band applications is presented in Chapter 4. Modified circuit designs to achieve tunable operation and a more compact size are described. Finally, simulation and experimental results of the S-band modulator indicating improved performance over the original modulator are presented and discussed.

Chapter 5 concludes the thesis with a summary of the performance features and benefits offered by the proposed QPSK modulator architecture. Recommendations for additional enhancements and feature extensions of the modulators are also given for future work.

Chapter 2

Literature Review

2.1 Introduction

This chapter explores two modulator architectures widely used in digital wireless transmission, namely heterodyne and direct-digital modulators, demonstrating the benefits of the latter. A general background on common digital modulation techniques including Quadrature Phase Shift Keying (QPSK) is also given. Ultimately, a literature review of recently published work on direct QPSK modulators is performed, evaluating common techniques to generate quadrature carriers and discussing conventional methods used for mixing.

2.2 Direct-digital and Heterodyne Modulators

In heterodyne modulators, digital data is converted in two (or more) steps to the desired RF signal for transmission as shown in Figure 2.1. The data first undergoes modulation at a lower IF frequency before its upconverted to the RF frequency. This is usually performed in a quadrature fashion by mixing 90° out-of-phase IF carriers with in-phase (I) and quadrature-phase (Q) data channels to suppress the undesired sideband. The resulting IF signal is then filtered to remove spurious harmonics generated by the mixers. The modulated IF signal is later upconverted to an RF signal using another mixer and filtered to remove the unwanted sideband and spurious harmonics. Because simple

upconversion generates the wanted and unwanted sidebands with equal magnitudes, the bandpass filter (BPF) must reject the unwanted sideband by a large factor, typically 50 to 60dB [6]. Such stringent specifications at high frequencies require a high quality (Q) filter, which is usually passive, off-chip and expensive. The RF signal is then boosted to the needed power level by a power amplifier (PA) and finally filtered to remove out-of-band components resulting from the nonlinearities of the PA.

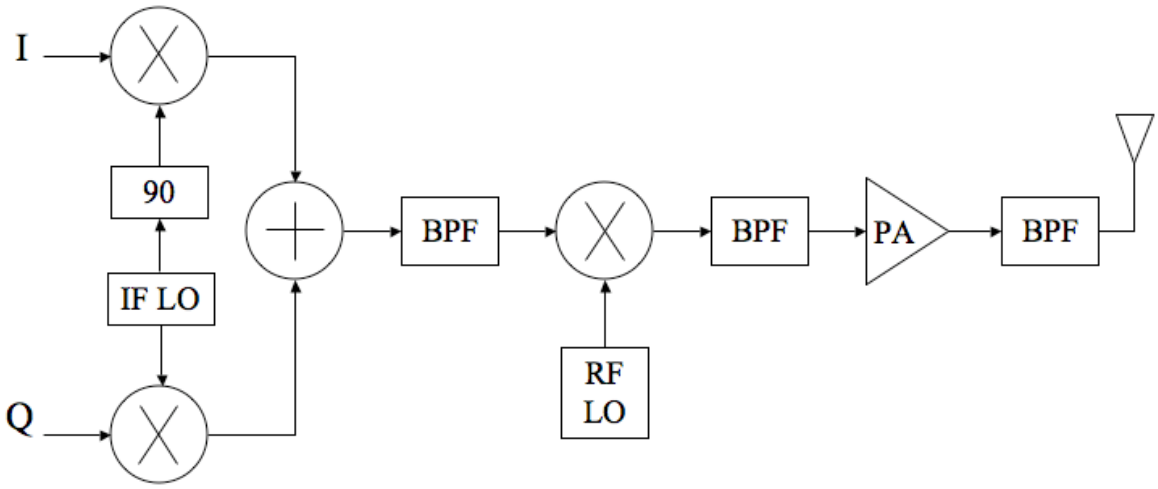

Figure 2.1: Heterodyne transmitter architecture.

In contrast, direct-digital modulators convert digital data directly to the desired RF frequency as shown in Figure 2.2. Data is both modulated and upconverted to an RF signal in the same quadrature modulator. A filter then removes harmonics generated by the mixers before amplification as in the heterodyne case. This simplifies the transmitter considerably, requiring no IF filters, RF upconverters and only one local oscillator (LO). Ultimately, the size and power consumption of the system are significantly reduced. Furthermore, filtering requirements and nonlinearities associated with the second upconversion stage are no longer present, facilitating IC integration to reduce costs and

improving the system's dynamic range. Finally, as modulation occurs at a high RF frequency as opposed to a low IF frequency, more modulation bandwidth is available for higher data rates.

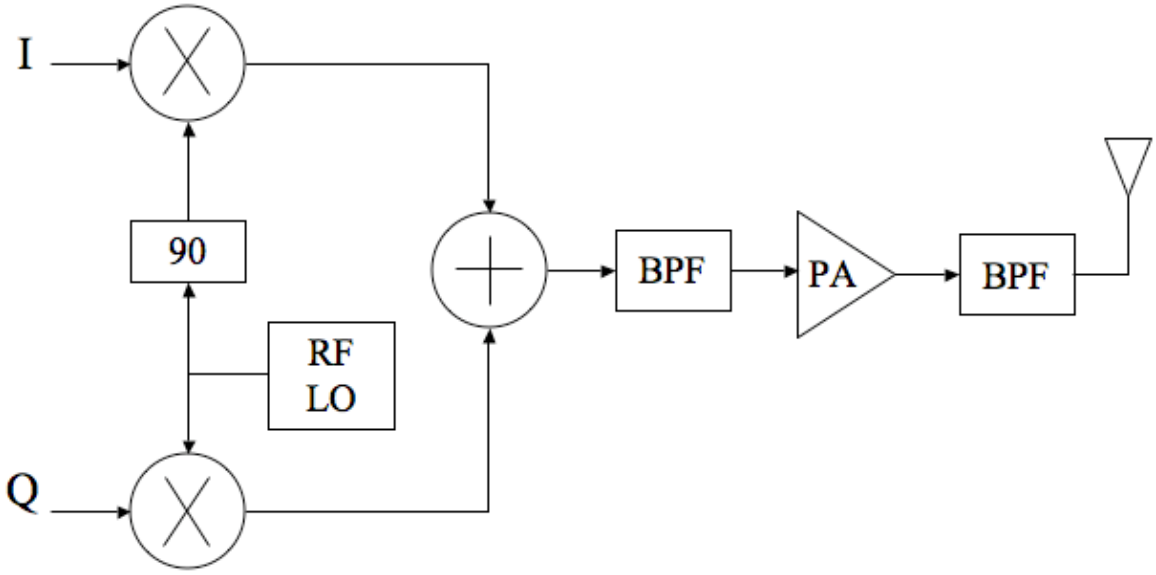

Figure 2.2: Direct-digital transmitter architecture.

Despite the various advantages mentioned above, direct-digital transmitters suffer from one important drawback: disturbance of the RF local oscillator (LO) by the power amplifier (PA) [6]. This issue arises because the PA output is a modulated waveform with a high signal power and a spectrum centered around the LO frequency. As illustrated in Figure 2.3 [8], the "noisy" output of the PA could leak to the local oscillator through parasitic coupling in the IC and corrupt the oscillator's spectrum. This usually occurs through a mechanism called "injection pulling" where the LO frequency tends to shift towards the noise frequency and eventually locks to it as the noise level increases. Such a process is illustrated in Figure 2.4 [8]. Nevertheless, various shielding techniques exist to isolate the LO and alleviate this problem such as buffering the LO output, placing guard rings around the LO [9], [10] and keeping the PA off-chip [11]. A more effective

approach is to offset the LO frequency by a significant factor (typically a half) so that it is sufficiently far away from the PA output spectrum. This is usually achieved by mixing the LO signal with another oscillator signal and then filtering the result, or by using subharmonic mixing techniques [8].

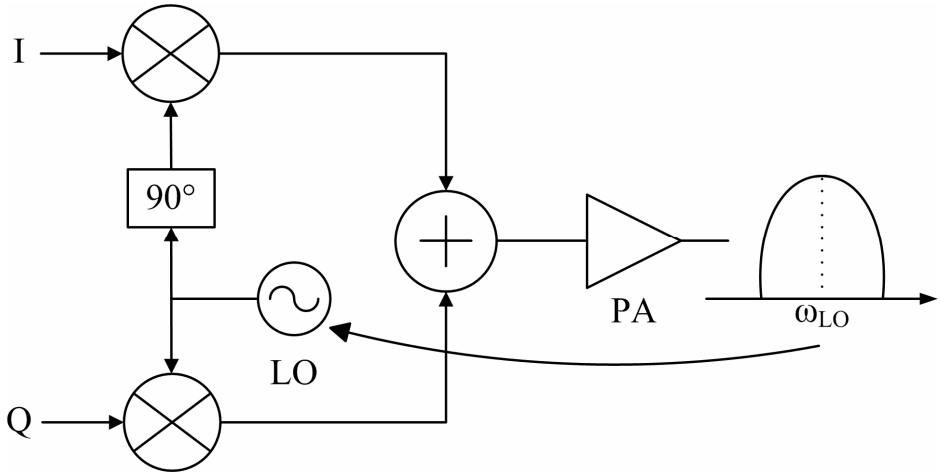

Figure 2.3: Leakage of PA output to the local oscillator.

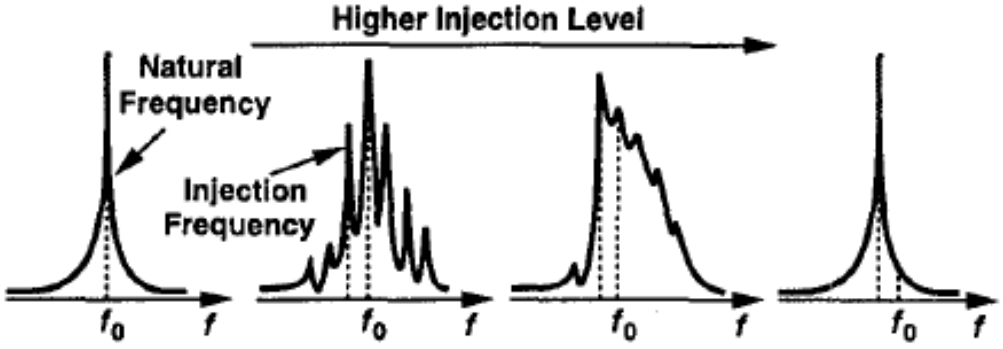

Figure 2.4: Injection pulling as the noise power increases [8].

2.3 Digital Modulation

2.3.1 Introduction

In digital communications, the modulating wave usually consists of non-return-to-zero (NRZ) binary encoded data while the carrier is a continuous-wave (CW) sinusoid. To distinguish one data value from the next a step change in the amplitude, frequency, or

phase of the carrier is made. In the more general case of *M*-ary signaling, 2^m distinct steps are needed to represent *m* bits of data sent at a time. The result of this process is Amplitude Shift Keying (ASK), Frequency Shift Keying (FSK) and Phase Shift Keying (PSK) respectively which are illustrated in Figure 2.5 [12]. As PSK and FSK modulated signals ideally have constant envelopes, they are less sensitive to amplitude nonlinearities in the transmitter's power amplifier (PA) that lead to spectral spreading [6], relaxing the PA's linearity requirements for higher power efficiency. For this reason, they are used much more widely than ASK in a variety of RF applications, including cellular phones, WLANs and GPS. There are many different possible types of PSK and FSK modulation available, each providing tradeoffs in quality, bandwidth, power efficiency and hardware complexity. Therefore, we will focus only on two popular PSK schemes that are relevant for this thesis, namely binary and quadrature PSK.

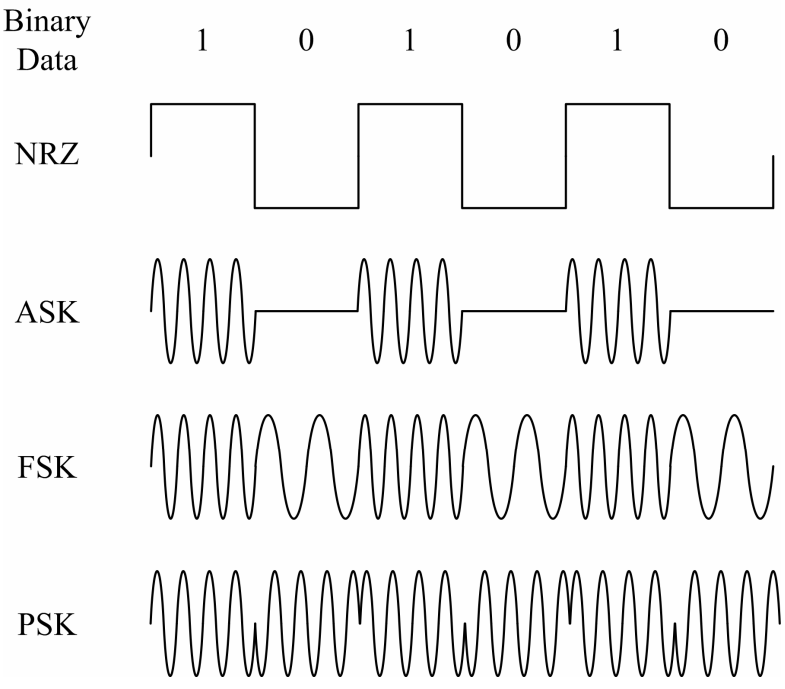

Figure 2.5: ASK, FSK and PSK modulation waveforms.

2.3.2 Binary and Quadrature Phase Shift Keying

Binary Phase Shift Keying (BPSK) modulation is a special case of the general *M*-ary phase shift keying with $M = 2$. In particular, the binary data selects one of the two opposite phases of the carrier. Shown in Figure 2.6 [12], the modulated signal can be written mathematically as:

$$BPSK(t) = A_{RF}\cos(\omega_{RF}t + \phi(t)), \tag{2.1}$$

where A_{RF} is the amplitude and ω_{RF} is the angular frequency of the RF carrier. The phase shift $\phi(t)$ is given by:

$$\phi(t) = i\pi, \tag{2.2}$$

with $i = 0$ or 1 corresponding to the binary data value. This is equivalent to writing:

$$BPSK(t) = B(t)\cos(\omega_{RF}t), \tag{2.3}$$

where $B(t)$ represents the input bit stream with a value of $-A_{RF}$ for logic 0 and $+A_{RF}$ for logic 1. Therefore, a BPSK system is characterized by a signal constellation that is one-dimensional with two message points at $\pm A_{RF}$ as shown in Figure 2.7 [13]. A block diagram of the simplest BPSK modulator is also shown in Figure 2.8, where the NRZ digital data and the carrier signal enter a mixer with the generated output being the desired BPSK signal.

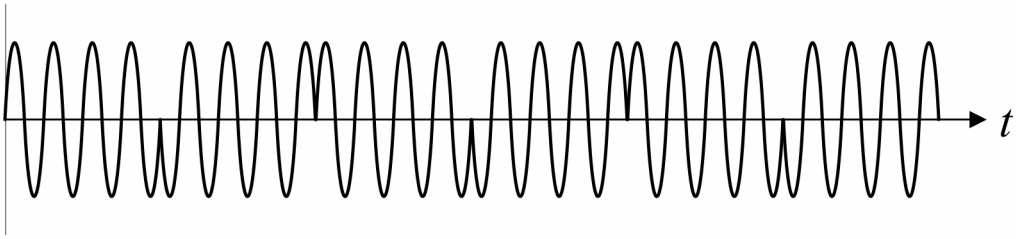

Figure 2.6: BPSK modulated waveform.

The power spectrum of a BPSK signal for random input binary data with logic 0 and 1 equally likely and the values transmitted in different time slots being statistically independent is known to have a sinc squared shape centered around the carrier frequency [13]. This is mainly due to employing rectangular pulses for the binary waveform in time domain, generating a wide sinc response in frequency domain. Mathematically, the power spectral density $S_{BPSK}(\omega)$ of a BPSK signal is [6]:

$$S_{BPSK}(\omega) = \frac{{A_{RF}}^2 T_b}{4} \frac{\sin^2\left[(\omega+\omega_{RF})T_b/2\right]}{\left[(\omega+\omega_{RF})T_b/2\right]^2} + \frac{{A_{RF}}^2 T_b}{4} \frac{\sin^2\left[(\omega-\omega_{RF})T_b/2\right]}{\left[(\omega-\omega_{RF})T_b/2\right]^2}, \tag{2.4}$$

where T_b is the bit period. This power spectrum falls off as the inverse of square of frequency as illustrated in Figure 2.9 [14]. From the plot, the power spectrum features a main lobe bounded by well-defined nulls. The width of this main lobe is referred to as the null-to-null bandwidth and is found to be twice the bit rate R_b:

$$BW = 2R_b = \frac{2}{T_b}. \tag{2.5}$$

As the null-to-null bandwidth encompasses the dominant lobe of the spectrum, it contains most of the BPSK signal energy. In fact, it can be shown that it carries more than 90% of the total energy [14].

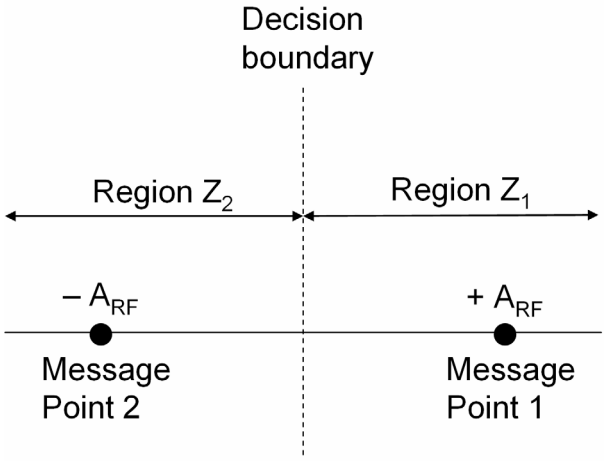

Figure 2.7: Signal constellation diagram of BPSK system.

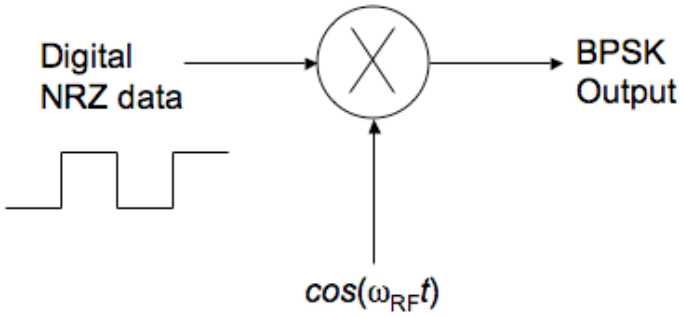

Figure 2.8: Block diagram of BPSK modulator.

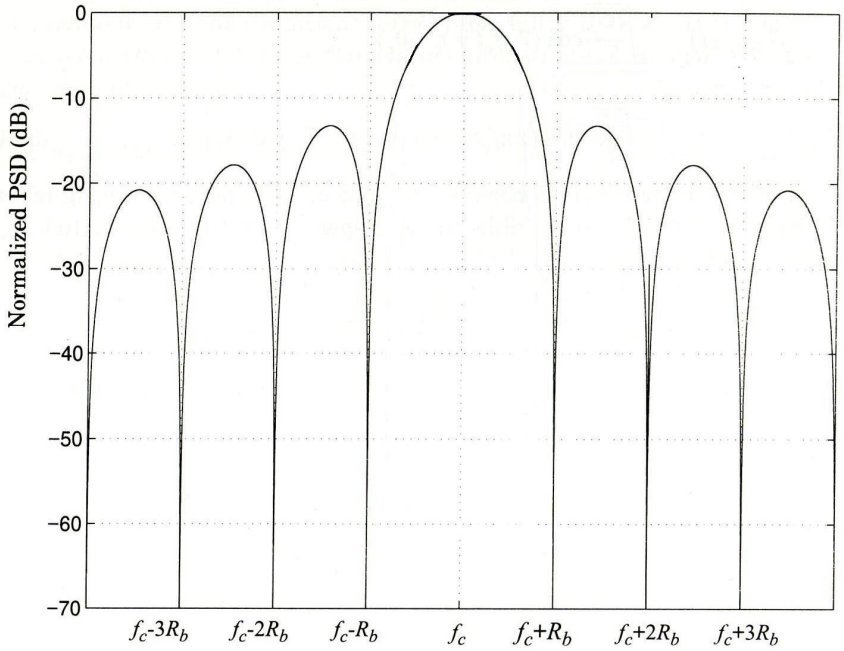

Figure 2.9: Power spectral density of BPSK signal [14].

An important goal in the design of an RF communication system is the efficient use of the frequency spectrum to arrive at the narrowest channel bandwidth for a given data rate. This is especially critical for limited-bandwidth applications in crowded frequency bands such as WLANs. Quadrature-carrier multiplexing systems have proven to be effective for this purpose [6] [13]. In such systems, the input binary data stream is divided into two separate streams that modulate a pair of quadrature carriers. The modulated output signals are then combined before transmission. A widely used example

of this is Quadrature Phase Shift Keying (QPSK), which is the next level up from BPSK. In QPSK, the binary data stream is subdivided into pairs of two bits or dibits each constituting a symbol. One of four equally spaced phases of the carrier, such as 45°, 135°, 225° and 315°, is then selected according to the symbol value. The modulated signal is shown in Figure 2.10 [13] and can be written mathematically as:

$$QPSK(t) = A_{RF}\cos(\omega_{RF}t + \phi(t)), \tag{2.6}$$

where the phase shift $\phi(t)$ is given by:

$$\phi(t) = (2i+1)\frac{\pi}{4}, \tag{2.7}$$

with i = 0, 1, 2, 3 corresponding to a unique symbol value. This is equivalent to writing:

$$QPSK(t) = I(t)\cos(\omega_{RF}t) + Q(t)\sin(\omega_{RF}t), \tag{2.8}$$

where $I(t)$ and $Q(t)$ represent the in-phase (I) and quadrature-phase (Q) bit streams in time with a value of $-A_{RF}/\sqrt{2}$ for logic 0 and $+A_{RF}/\sqrt{2}$ for logic 1. It is important to note that the arithmetic operation in (2.8) is merely inconsequential, i.e. either an addition or subtraction can be chosen as long as it is performed using complex vector arithmetic. Therefore, a QPSK system is characterized by a signal constellation that is two-dimensional with four message points as shown in Figure 2.11 [13]. A block diagram of the simplest QPSK modulator is also shown in Figure 2.12 where I and Q NRZ digital signals are mixed with quadrature phases of the carrier and then summed at the output.

Since a QPSK signal can be seen as the summation of two BPSK signals in quadrature, its power spectrum is similar to that of its BPSK constituents. However, for the same overall data rate, the QPSK symbol (dibit) rate only needs to be half of the

BPSK bit rate. Thus the power spectral density $S_{QPSK}(\omega)$ of a QPSK signal can be derived from (2.4) by substituting $2T_b$ for T_b [6]:

$$S_{QPSK}(\omega) = \frac{{A_{RF}}^2 T_b}{2} \frac{\sin^2\left[(\omega+\omega_{RF})T_b\right]}{\left[(\omega+\omega_{RF})T_b\right]^2} + \frac{{A_{RF}}^2 T_b}{2} \frac{\sin^2\left[(\omega-\omega_{RF})T_b\right]}{\left[(\omega-\omega_{RF})T_b\right]^2}. \tag{2.9}$$

This power spectrum has the same sinc squared shape as in Figure 2.9 and is plotted separately in Figure 2.13 [14] below. The null-to-null bandwidth of the main lobe is found to be the bit rate R_b:

$$BW = 2\left(\frac{R_b}{2}\right) = R_b = \frac{1}{T_b}, \tag{2.10}$$

which is half of that shown in Figure 2.9 for BPSK. Therefore QPSK requires only half the bandwidth of BPSK for the same data rate. It should be pointed out that this significant improvement in bandwidth efficiency comes at the relatively small cost of increased hardware complexity as shown in Figures 2.8 and 2.12. In addition, as illustrated in Figures 2.7 and 2.11, there are more adjacent points in the signal constellation for QPSK than BPSK with a smaller minimum distance between them, suggesting a higher probability of error in the presence of noise which adversely affects the system's quality. However, a more careful analysis reveals that the symbol energy (E_s) in QPSK given by [6]:

$$E_s = \frac{{A_{RF}}^2}{2}(2T_b) = {A_{RF}}^2 T_b, \tag{2.11}$$

is twice as large as the bit energy in BPSK. With this observation it can be proved that BPSK and QPSK have approximately the same probability of error especially at higher energy to noise (E/N) ratios [13].

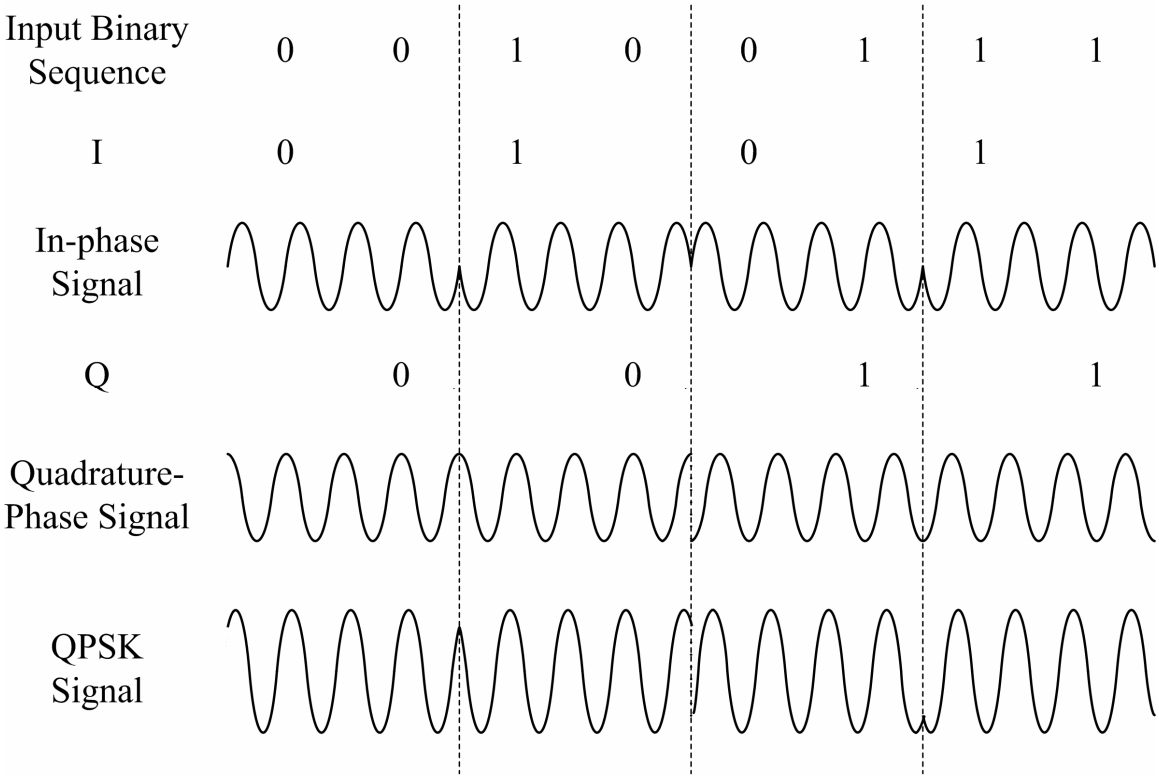

Figure 2.10: QPSK modulation signals.

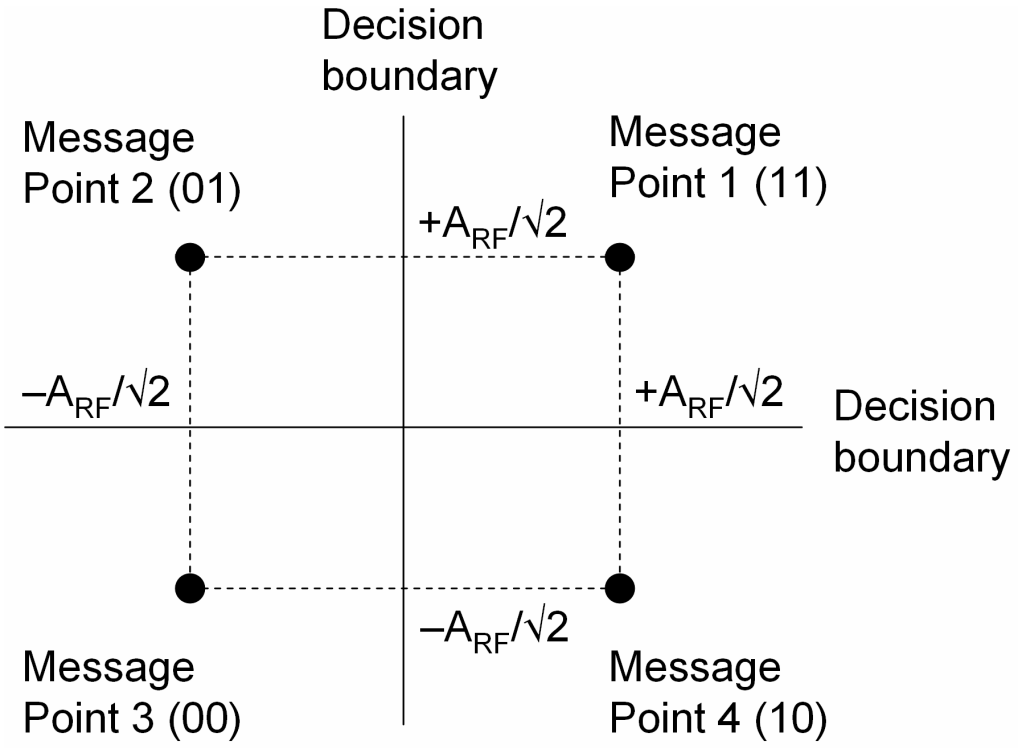

Figure 2.11: Signal constellation diagram of QPSK system.

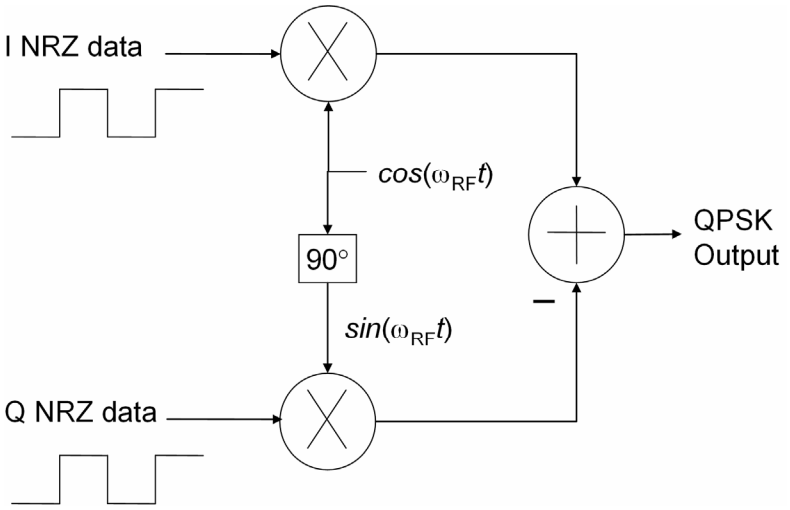

Figure 2.12 Block diagram of QPSK modulator.

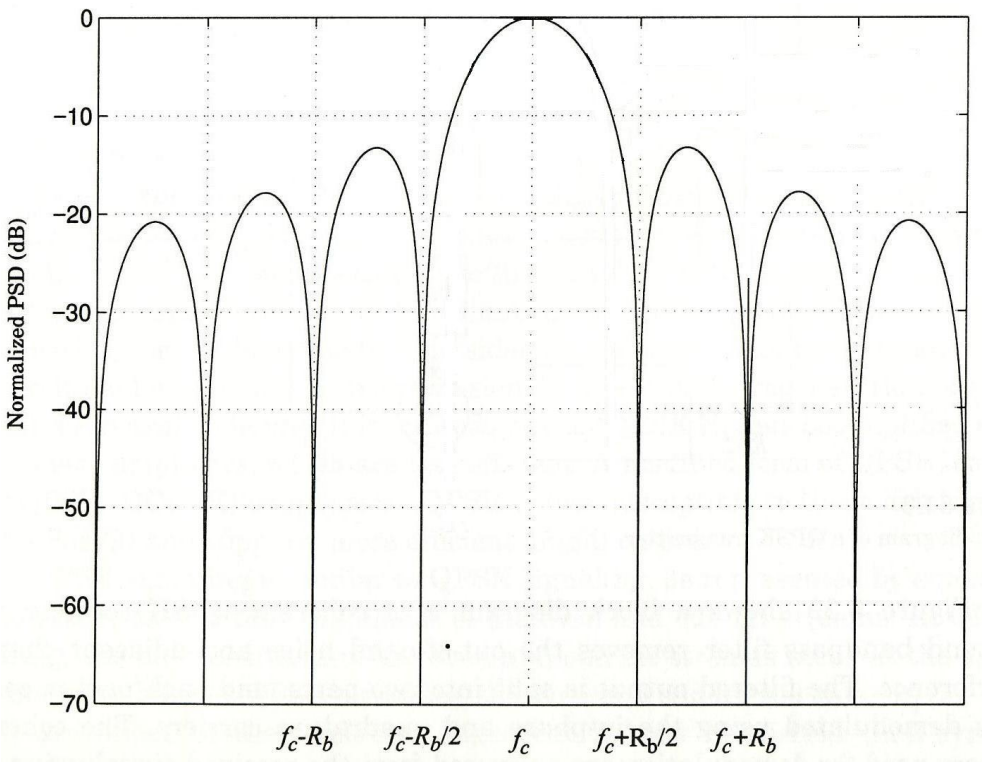

Figure 2.13: Power spectral density of QPSK signal [14].

In our treatment of BPSK and QPSK modulators, we have assumed that the data bits were represented by time-limited rectangular pulses which gave rise to sinc shaped frequency spectra extending out to infinity as shown in Figures 2.9 and 2.13. It is

therefore important to discuss methods to limit the width of the generated spectrum to reduce interference with neighboring channels in crowded frequency bands. In practice, the transmitter includes a few bandwidth-limiting components such as lowpass and bandpass filters that serve towards this goal. However, such filtering attenuates and delays the high and low frequency components differently, dispersing the rectangular pulse and extending its duration beyond the allocated period [13]. Therefore when a sequence of symbols is transmitted through the system the dispersed pulses will interfere with each other leading to a destructive phenomenon called intersymbol interference (ISI) as shown in Figure 2.14 [6]. This increases the probability of error especially when transmitting random data in narrowband channels, further degrading the system's quality. To mitigate this problem, different pulse-shaping techniques can be used for the digital data to sharply reduce its spectrum content beyond the specified channel. A sinc shaped pulse is ideally suited for this purpose according to Nyquist's theorem, but due to practical difficulties in its implementation a raised-cosine shape is usually used [8] [13].

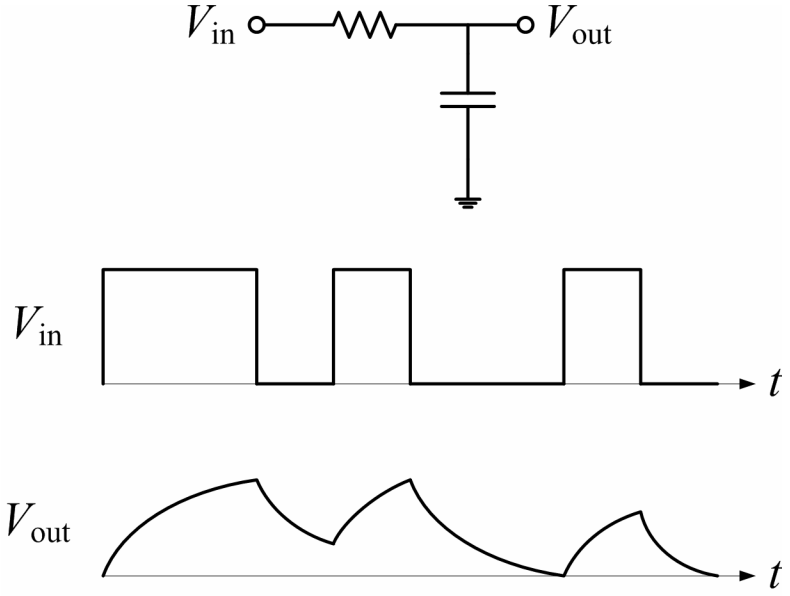

Figure 2.14: Dispersion of rectangular pulses through a low pass filter.

2.4 QPSK Modulator Circuit Techniques

There are several direct-digital QPSK modulator designs that have been developed over time with different circuit topologies for each component in Figure 2.12, particularly the 90° phase shifter and modulating mixer. In this section, the most common circuits will be discussed with their advantages and limitations to give an overview of the various alternatives available in the design of QPSK modulators.

2.4.1 Quadrature Signal Generation

The performance of any direct-conversion quadrature modulator including its signal constellation accuracy, bit error rate (BER) and modulation bandwidth depends highly on the accuracy of generating quadrature carriers. For this reason, several techniques have been designed to generate accurate 90º phase shifters with low amplitude and phase errors [15]. These include: 1) frequency divide-by-two circuits [16]-[18]; 2) microwave distributed couplers [19]-[22]; 3) resistor-capacitor (RC) all-pass filters [23], [24]; 4) resistor-capacitor, capacitor-resistor (RC-CR) networks [25]-[27]; 5) inductor-capacitor (LC) high and low pass filters [28], [29]; and 6) RC polyphase filters [30]-[34]. In frequency divide-by-two circuits (DTCs), two latches are cascaded in a negative feedback loop to form a master-slave flip-flop with each stage exhibiting a 90° phase shift for the required loop total of 180°, as shown in Figure 2.15 [6]. The outputs of the latches are thus in quadrature but only when the inputs are precisely complementary and the two latches match perfectly. In practice, device mismatches result in phase imbalances and additional imbalances occur as the input differential signals are not exactly 180° out of phase especially at high frequencies. Despite efforts for overcoming these problems to generate an accurate 90° phase shift, the latches usually consume a

significant amount of DC power. In addition, generating an oscillator signal at twice the frequency could entail more DC power or might be impractical altogether if the desired LO frequency is very high, for example 60GHz [6].

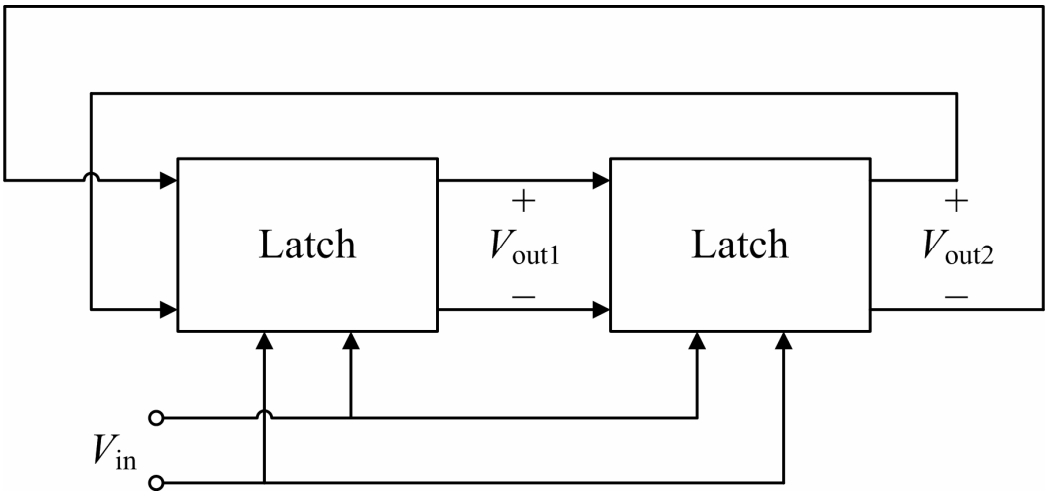

Figure 2.15: Divide-by-two circuit as a quadrature generator.

Microwave distributed networks such as the branch-line, Lange and parallel line couplers that use planar transmission lines (e.g. microstrip or coplanar waveguides) can provide a very precise 90° phase shift over a wide band of frequencies [20], [21]. They are also well established and can be readily designed with excellent model-to-hardware correlation [22], [35]. However, they tend to be prohibitively large for monolithic IC integration especially at lower RF and microwave frequencies where the wavelength is on the order of centimeters. For this reason, they are not often used in IC designs and will not be further discussed here.

RC all-pass phase shifters consist of a pair of RC networks and differential amplifiers with component values chosen to yield a transfer function that has constant magnitude for all frequencies, i.e. an all-pass response. Figure 2.16 [23] below is an example of an RC all-pass phase shifter. The relative RC time constants between the two

networks are designed in such a manner that the phase difference between their output signals is 90° at the center frequency [24]. Second and higher order RC networks (Figure 2.16) are usually employed to achieve this 90° phase shift over a broader range of frequencies. An interesting property of these networks is that most of the design parameters depend on ratios between component values as opposed to their absolute values [23]. This makes them less sensitive to process variations, albeit the centre frequency still shifts with any change in component value. While the broadband performance of RC all-pass filters is a definite plus, they are particularly large and complicated to design [24].

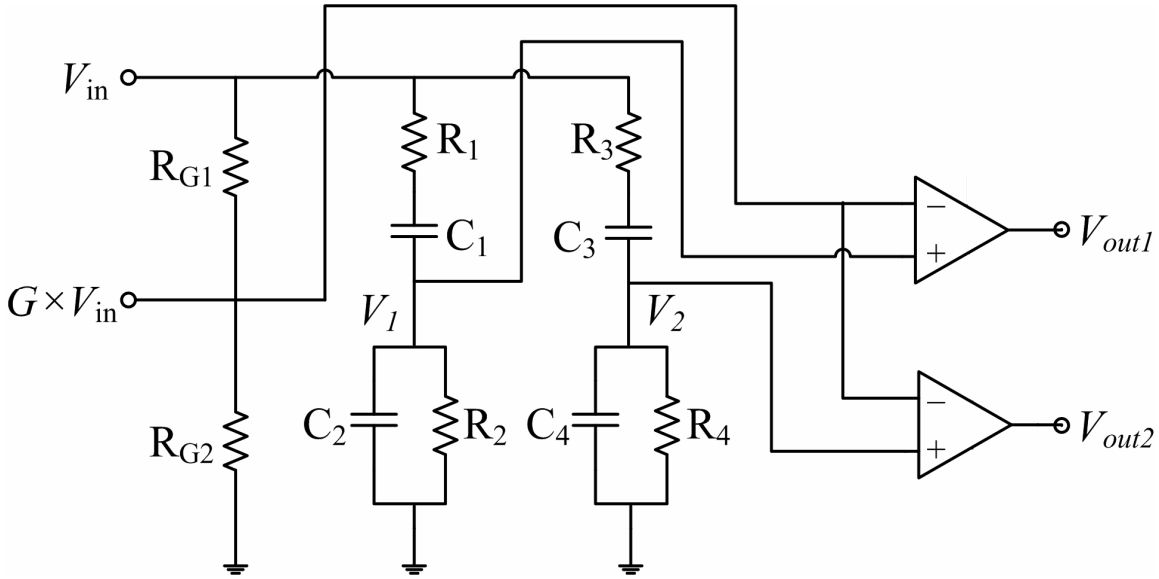

Figure 2.16: RC all-pass phase shifter schematic.

RC-CR networks shown in Figure 2.17 [6] provide a simple technique to shift the signal by ±45°. The phase difference between the two outputs is 90° for all frequencies which is desirable, but the amplitudes are equal only at the cutoff frequency $\omega = 1/(RC)$, where R and C are the resistor and capacitor values. Therefore, the phase difference is not

sensitive to process variations but the amplitude match certainly is. If the value of either *R* or *C* changes, so does the frequency at which equal-magnitude signals exist [6]. Much effort has been made to achieve an amplitude match over a wide frequency range by using limiters (e.g. differential amplifiers), but several stages need to be cascaded which consumes a lot of DC power, diminishing the main advantage of RC-CR networks [25], [36]. As depicted in Figure 2.17, the circuit is entirely passive and therefore consumes zero DC power, a definite plus in portable low-power applications. Nevertheless careful circuit and device layout techniques, such as common-centroid layout for example, are available to reduce component mismatch and tolerances for satisfactory model-to-hardware correlation. Furthermore, an additional design cycle may be used to adjust the performance if deemed feasible.

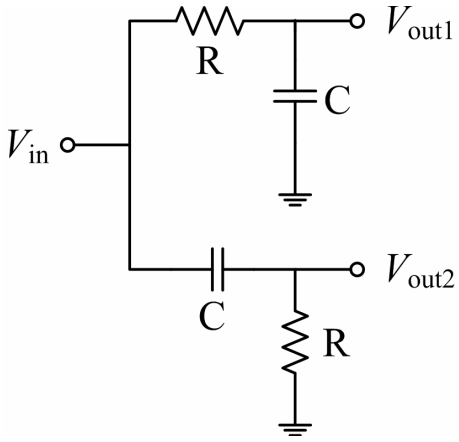

Figure 2.17: Circuit schematic of RC-CR network.

LC high and lowpass filters (Figure 2.18 [28]) also provide a simple method to shift the signal by ±45° and are similar to RC-CR networks with the resistors essentially replaced by inductors. Doing so provides a lower signal loss than RC-CR networks but at the cost of significantly increased footprint, possibly reaching prohibitive levels for monolithic integration. For this reason, they are not widely used as the other alternatives.

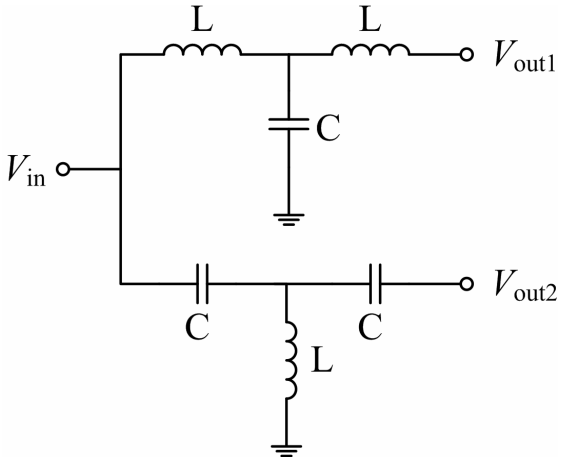

Figure 2.18: LC high and low pass phase shifter.

An RC polyphase filter is a symmetric RC network with inputs and outputs connected in relative phases as shown in Figure 2.19 [31] below. Each RC (CR) branch leads to a -45° (+45°) phase shift at the cutoff frequency of $1/(RC)$. Therefore the differential inputs are shifted ±45° towards each other at this cutoff frequency and combined at the outputs (with 0dB gain) to form the differential quadrature signals.

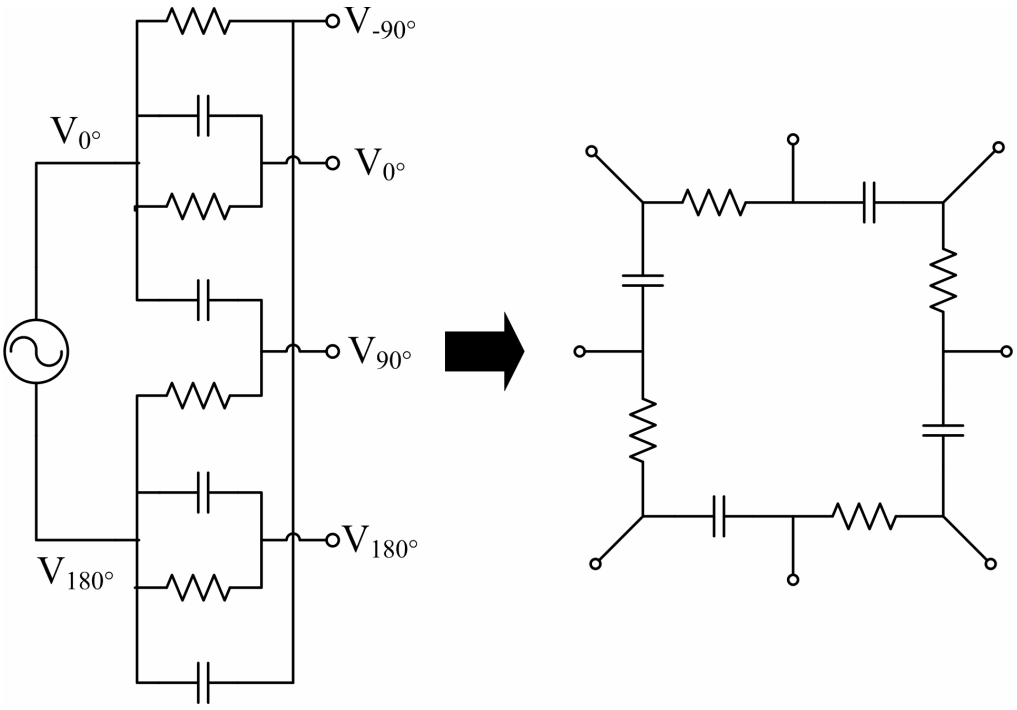

Figure 2.19: RC polyphase network as a symmetric RC network.

The RC polyphase network can be viewed as low-pass (RC) and high-pass (CR) filter sections connected together at the outputs, with their low and high pass frequency responses combining together for an overall all-pass response. Thus, in contrast to the RC-CR network, a 90° phase difference only appears at the cut-off frequency $1/(RC)$ while the amplitudes are matched irrespective of frequency. A result of this is that the phase difference is now sensitive to process variations and the frequency at which quadrature signals exist will shift if the value of R or C changes. Most efforts to counter this problem have focused on cascading several stagger-tuned stages of the polyphase filter whose cut-off frequencies are logarithmically spaced out for a wideband equiripple response [31]-[34]. Doing so gives rise to a large footprint and possibly substantial signal loss as each stage loads the previous one. Careful circuit and device layout techniques, such as common-centroid layout for example, may nonetheless by used to reduce component mismatch and tolerances for satisfactory predictability. Furthermore, an additional design cycle may be employed to adjust the performance if possible.

2.4.2 Modulation Mixers

There are many ways to implement the mixers shown in Figure 2.12 for QPSK modulation, each providing tradeoffs in performance such as conversion gain, linearity, noise, port-to-port isolation and input matching.

2.4.2.1 Gilbert Cell Mixers

The Gilbert cell [37] is a very common mixer architecture that lends itself particularly well to monolithic integration and has several advantages including high conversion gain, high port-to-port isolation and spurious signal cancellation due to its double-balanced structure. Figure 2.20 shows a circuit schematic of the Gilbert cell implemented in CMOS technology using field-effect transistors (FETs). It consists of a

differential transconductor pair (M1-M2) that converts the input voltages into complimentary current signals. Two switching cores (M3-M4 and M5-M6) driven by large LO signals alternately steer (commutate) these currents from one output side to the other. The final output is then taken differentially between the two sides. In effect, the input currents are multiplied by a square wave whose frequency is that of the carrier LO, generating the desired mixing product at the output.

The transconductor pair (M1-M2) should ideally produce current signals that are perfectly proportional to the input voltage, but in practice imperfections will give rise to spurious unwanted signals. Hence an important design challenge is to maximize the linearity of the transconductor. The most common solution is to use source degeneration to provide negative feedback and linearize the transfer characteristic. Resistive degeneration may be adequate for this goal but the generated thermal noise degrades the noise figure (NF). In addition, the DC voltage drop across the resistors reduces the supply headroom, which is particularly important for low-voltage applications, as shown later. For these reasons inductive degeneration (Figure 2.21) is preferable, as the increasing reactance of an inductor with increasing frequency also helps to attenuate high frequency harmonic and intermodulation components [38]. A drawback of using inductors of course is the additional area consumed on-chip, which increases the cost of the IC. Another possible technique is to remove the tail current source and connect the source terminals of M1 and M2 to ground, either directly or through degeneration as in Figure 2.22 [36]. Not only does this relax the supply voltage headroom, but it also eliminates interaction between the two devices through their once common source node, which reduces third-order non-linearities and associated intermodulation products [39].

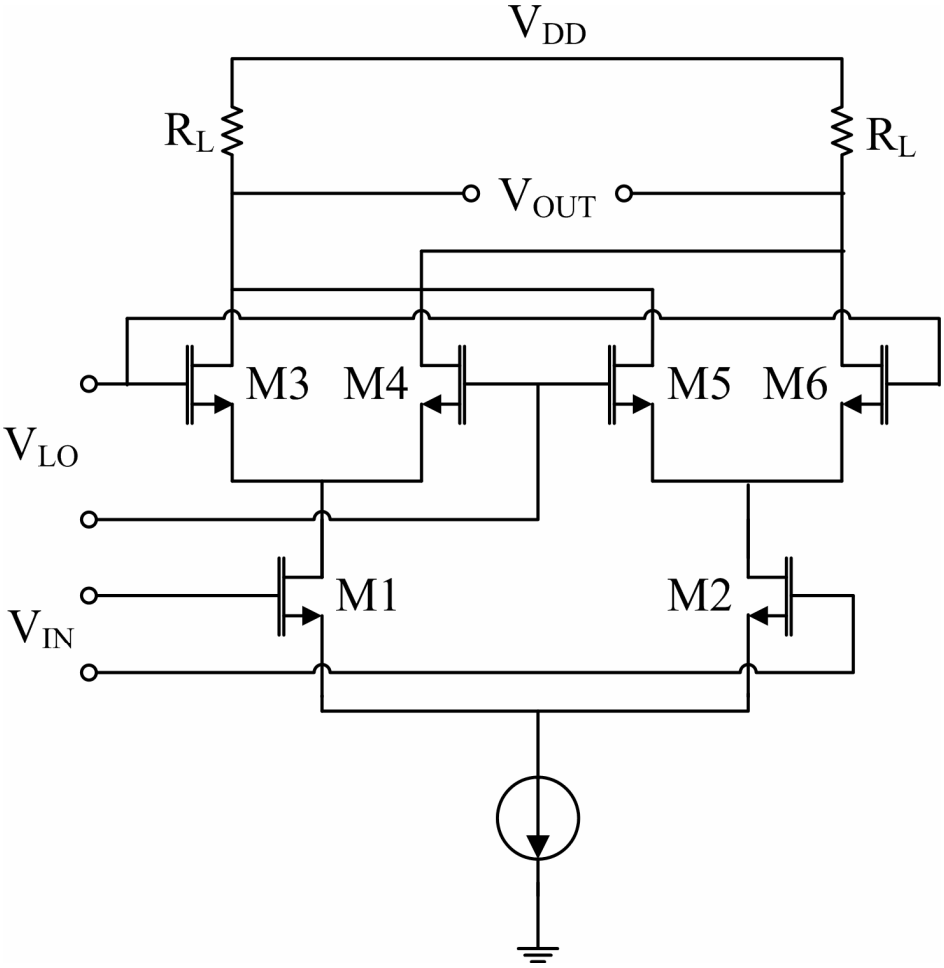

Figure 2.20: Double-balanced Gilbert cell mixer in CMOS.

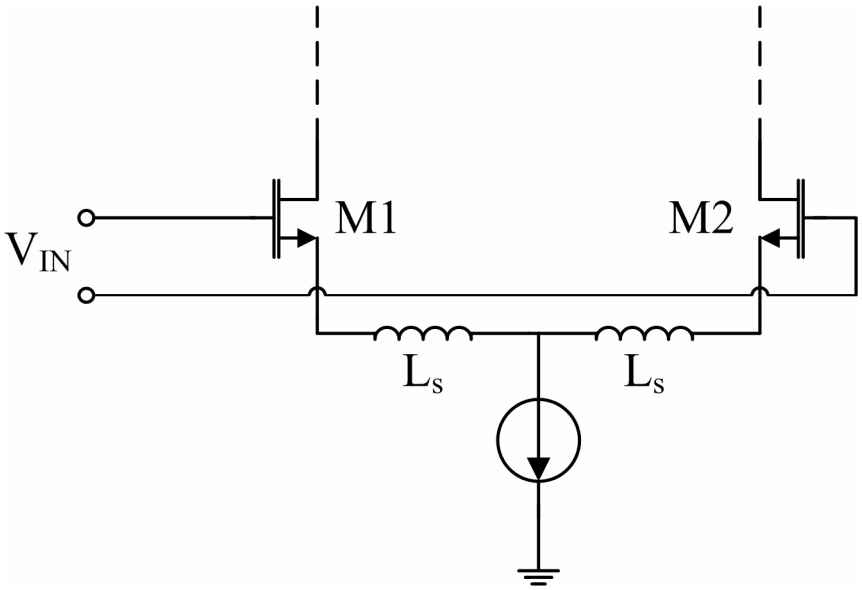

Figure 2.21: Inductive degeneration to linearize transconductor for Gilbert mixer.

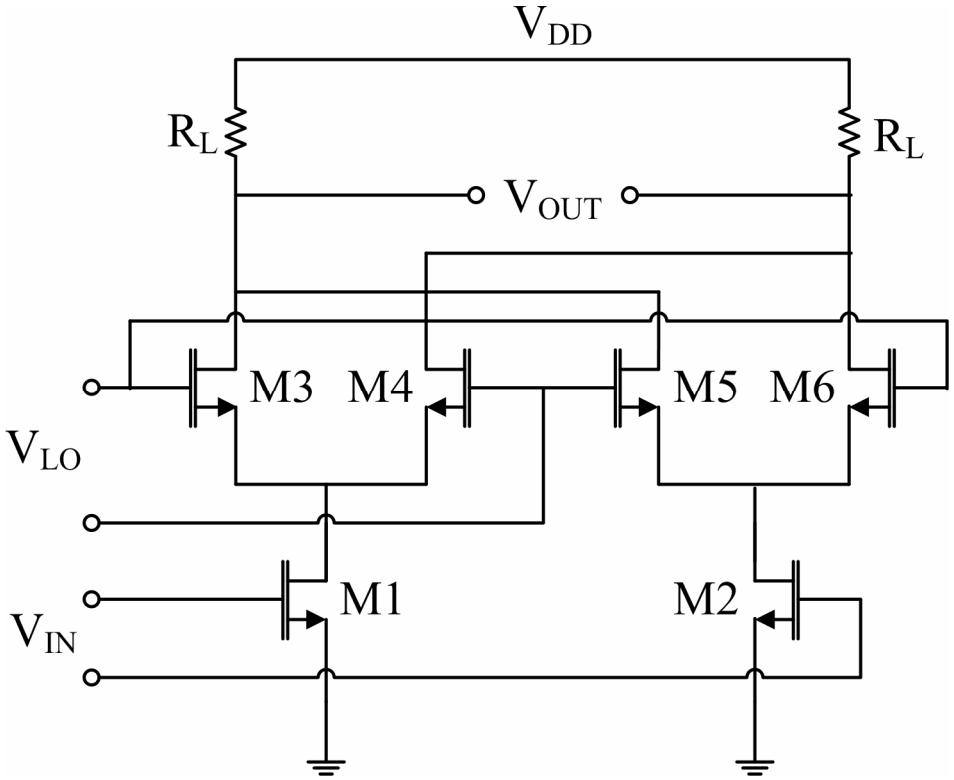

Figure 2.22: Gilbert cell mixer with grounded-source transconductor.

The power consumption of the Gilbert cell can be somewhat high depending on the biasing conditions required for the desired performance. Since the Gilbert cell has at least two stacked levels of transistors, its use with a low supply voltage can be quite challenging as the tradeoff between gain and linearity becomes problematic. This can be quantified by writing a simple expression for the voltage conversion gain (A_v) as [40]:

$$A_v = g_m R_L = \frac{2I_D}{V_{GS} - V_T} \frac{V_{RL}}{I_D} = \frac{2V_{RL}}{V_{GS} - V_T}, \tag{2.12}$$

where g_m is the transconductance of M1-M2, R_L is the output load resistance, I_D is the bias current, $V_{GS} - V_T$ is the gate-source overdrive voltage of M1-M2, and V_{RL} is the voltage drop across the load resistors R_L. This clearly depicts the tradeoff between gain ($g_m R_D$) and linearity ($V_{GS} - V_T$) for limited voltage headroom (V_{RL}). With a fixed supply voltage depending on the technology node, low-power Gilbert mixer design has focused

on decreasing the bias current while keeping the same gain and linearity [41]. The transistor widths are decreased in proportion to keep their gate overdrive ($V_{GS} - V_T$) and linearity intact. As the transconductance is now rather low due to the small gate width and current, the output load resistance is also increased to achieve the same voltage conversion gain.

The noise figure (NF) of Gilbert cell mixers can be somewhat high as there are at least six active devices contributing noise, as well as possibly four or more resistors. One noise source is definitely the transconductor pair with its NF establishing a lower bound on the overall mixer NF [38]. This may be computed readily using the same approach as calculating the NF of a low noise amplifier (LNA) [38], [42]. The switching cores also degrade the noise performance in a number of ways. In practice, the switches are lossy and have poor isolation, which attenuates the signal current and increases the NF. Another NF contribution arises from the interval of time in which both switches are simultaneously on for part of the LO period. During this time the two transistors amplify and inject their noise (thermal gate resistance and channel noise) to the output. To minimize this, large LO signals are employed to make the switches switch practically instantaneously, which is becoming more and more of a challenge as the supply voltage is reduced. In contrast to the transconductor noise, the noise contributed by the switches is usually difficult to calculate, as their operation is time-variant with frequency translation present [6]. Nevertheless, practical Gilbert mixers generally exhibit a noise figure of around 15dB or more.

Finally, the input impedance to a Gilbert cell mixer is relatively high and predominantly imaginary due to the small capacitance presented by the gates of the FET,

which is far from being matched to the system's real impedance (50Ω standard). Thus a matching network is typically required that can be implemented on-chip using inductors and/or capacitors. A potential problem with this is that the matching network may occupy a very large area, increasing the cost of the IC considerably. Another solution would be to implement the matching network off-chip using packaged lumped elements or distributed networks with transmission lines. This requires taking the signal off-chip and then back on which often results in losses along with added noise.

2.4.2.2 Passive Mixers

While active mixers such as the Gilbert cell are most commonly used for their high conversion gain and port-to-port isolation, passive mixers may also be realized with other attractive properties such as small IC footprint and zero DC power consumption. In the Gilbert cell, representations of the input signal in the form of currents are multiplied by the local oscillator (LO) signal. To avoid linearity and noise problems associated with the voltage-to-current (V-I) conversion, the input signal can be switched directly in the voltage domain. As CMOS is highly tailored for digital circuits, high-performance multipliers based on switching are naturally implemented in this technology. A simple CMOS passive mixer is shown in Figure 2.23, which consists of only two FET switches (M1 and M2) driven by complimentary phases of the LO. As this mixer is only single-balanced, it suffers from low isolation between the LO port and the output port. Figure 2.24 [38] shows a double-balanced passive commutating mixer that offers high port-to-port isolation and thus relaxes the filtering requirements at the output. It consists of four FET switches (M1, M2, M3 and M4) in a "ring" or "bridge" configuration driven by large LO signals in complementary phases so that one diagonal pair is conducting at any given time. When M1 and M4 are switched on, the differential output signal is equal to

the input signal. But when M2 and M3 are conducting, the output signal is equal to the negative of the input. In effect, the input signal is multiplied by a square wave with the frequency of the LO.

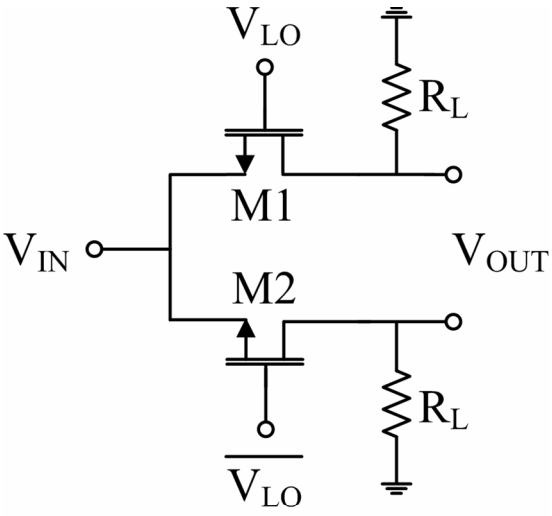

Figure 2.23: Single-balanced passive mixer in CMOS.

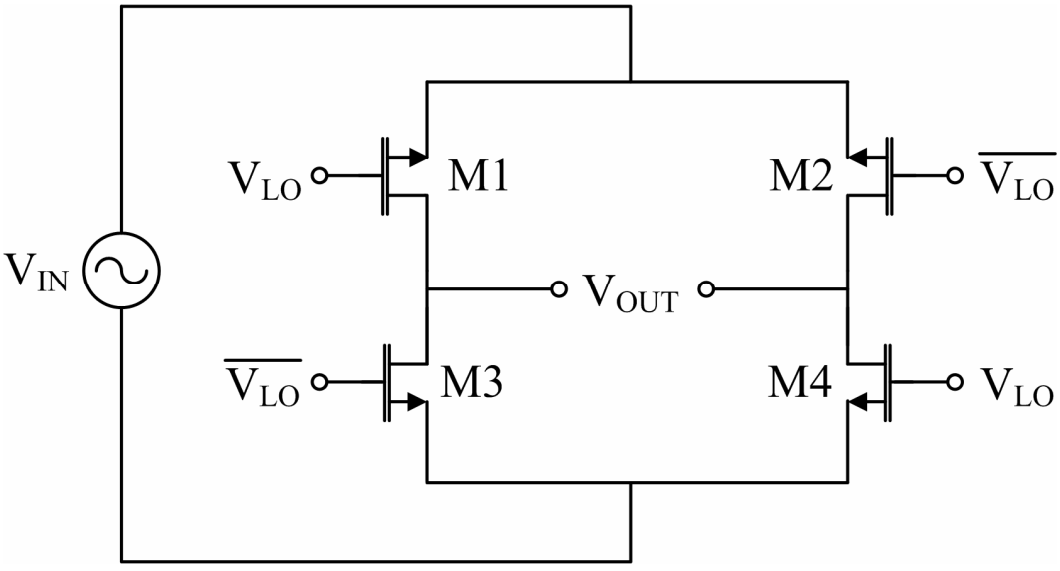

Figure 2.24: Double-balanced passive mixer in CMOS.

The passive mixer of Figure 2.24 generally has a high linearity [43] if the transistors experience a large gate-to-source overdrive voltage in the on state so that their on-resistance does not vary significantly with the input voltage. This can be quantified

by writing the following expression for the switch's on-resistance R_{DS}, which will be discussed in more detail in later chapters as well:

$$R_{DS} \approx \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)}, \tag{2.13}$$

where μ_n is the electron mobility, C_{ox} is the gate oxide capacitance per unit area, W and L are the width and length of the FET, V_{GS} is the gate-to-source voltage and V_T is the threshold voltage. The applied gate-to-source voltage V_{GS} is equal to the difference between the local oscillator (V_{LO}) and input (V_{IN}) voltages in this case:

$$R_{DS} \approx \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{LO} - V_{IN} - V_T)}. \tag{2.14}$$

Equation (2.14) clearly shows that the on-resistance R_{DS} is inversely proportional to the gate-to-source overdrive voltage ($V_{LO}-V_{IN}-V_T$), with only small variations in its value at large voltage levels. This linearity advantage may diminish however as the voltage is scaled down with technology generation. As illustrated in Figure 2.25 using a sinusoidal LO signal V_{LO}, the switch gate-to-source overdrive voltage can be relatively small over a considerable part of the LO period. Therefore, the input voltage V_{IN} varies the switches' on-resistance significantly during this time, introducing nonlinear distortion [36].

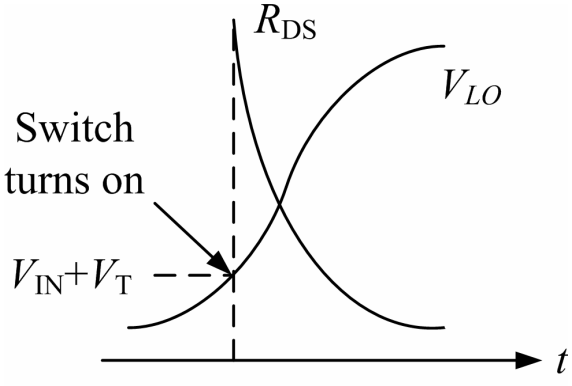

Figure 2.25: Variation of switch on-resistance.

The noise figure (NF) of passive CMOS mixers can be relatively low (~10dB), at least when compared to that of Gilbert cell mixers [44]. This is because the need for a transconductance stage is eliminated in the passive mixer, which usually sets a lower bound on the overall Gilbert cell mixer NF. The noise contributed by the switches is usually difficult to calculate, as their operation is time-variant with frequency translation present [6]. Nevertheless, as can be seen from Figure 2.24, either the on-resistance of transistor M1 (M4) or M3 (M2) is connected to one of the outputs at any given time. In effect, the on-resistance R_{DS} given by (2.14) is always connected to the output. Therefore, the LO drive (V_{LO}) and device width (W) can be increased as much as possible to minimize this resistance and its associated thermal noise for a low NF. Another NF contribution arises from the interval of time in which both complimentary switches M1 and M3 (M2 and M4) are simultaneously on for part of the LO period. During this time the net on-resistance R_{NET} of the two switches in parallel (as seen from the output) remains roughly constant at a value given by [45]:

$$R_{NET} = R_{DS} \| R_{DS} = \frac{R_{DS}}{2} \approx \frac{1}{2\mu_n C_{ox} \frac{W}{L}(V_{LO} - V_{IN} - V_T)}, \tag{2.15}$$

which also generates thermal noise at the output degrading the NF. To minimize this, sufficiently large LO signals are needed to make the switches switch almost instantaneously. However large LO signals are becoming more and more difficult to achieve as the voltage is reduced from one technology generation to the next. Finally, the absence of a DC biasing current eliminates transistor flicker ($1/f$) noise which would otherwise be translated to high frequencies upon mixing [27]. This property is also valuable in direct-digital receivers where $1/f$ noise is particularly dominant [46].

Passive mixers nonetheless suffer from a number of drawbacks including conversion loss. Their conversion loss can be readily estimated if we assume that the transistors behave as ideal, instantaneous switches. Then the differential output voltage may be regarded as the result of multiplying the input voltage by a unit amplitude square wave. Since the fundamental component of the square wave has a magnitude of $4/\pi$, we may write the following expression for the voltage conversion gain (A_v) [38]:

$$A_v = \frac{2}{\pi}, \tag{2.16}$$

where the desired mixing product is divided evenly between the sum and difference frequency components and hence the factor of $2/\pi$ is present as opposed to $4/\pi$. In practice, the actual voltage conversion gain will drop further from $2/\pi$ (≈ -4dB) as the transistors do not switch instantaneously and have a non-negligible loss. Also for sinusoidal LO signals, transistors M1 (M4) and M3 (M2) are simultaneously on for a considerable part of the period making the gain even lower. These effects can be mitigated nonetheless by using a large LO drive (V_{LO}) and FET width (W). However as the width W of the device is made larger, its intrinsic parasitic capacitances increase leading to more capacitive coupling and less isolation between ports, especially at higher frequencies. Such an effect will be discussed in more detail in chapters 3 and 4. Nevertheless, as this circuit exhibits a loss of several decibels, the noise of the following stage is "amplified" when referred to the input. This may require a low-noise stage after the mixer to limit the overall NF of the transmitter at the cost of increased power consumption and area [36], [46].

Finally, the overall performance of CMOS passive mixers in terms of conversion gain, linearity and noise figure strongly depends on the available LO drive as discussed

above, which emphasizes the need for good LO buffers with adequate driving ability. This is typically achieved using large FETs with a high current consumption to yield a relatively high transconductance g_m. Thus to reduce the power consumed by the LO buffers, the gate capacitance of the switches can be resonated with an inductor to generate a higher loading impedance for a larger voltage swing. A potential problem with this however is that the inductors may occupy a very large area especially at low LO frequencies, increasing the cost of the IC considerably. Furthermore, the narrowband resonant behavior of the loading impedance will adversely affect the broadband operation of the LO buffers and the overall mixer [38].

2.5 Conclusions

In this chapter, direct-digital modulators were explored in detail demonstrating their benefits over the traditional heterodyne counterparts. For instance, the IF components and the RF upconverter are no longer needed, simplifying the transmitter and facilitating integration with existing digital CMOS circuits for a reduced size, cost and power consumption. Common digital modulation techniques including PSK were also reviewed as necessary background for this thesis. In particular, quadrature-carrier multiplexing systems such as QPSK were shown to be effective in increasing the bandwidth efficiency by a factor of two compared to BPSK, which is critical in crowded frequency bands. Finally, the most common circuits for the 90° phase shifter and modulating mixers were evaluated to give an overview of the various alternatives available in the design of QPSK modulators. Passive circuits such as RC networks and CMOS passive mixers are generally more suitable for portable wireless applications, as they offer small footprint and zero DC power consumption.

Chapter 3

L-Band Direct-Digital QPSK Modulator

3.1 Introduction

This chapter discusses the new direct-digital QPSK modulator concept developed for this work and describes the design of an L-band modulator in CMOS technology that demonstrates this concept [7]. It also investigates new and commonly used circuit techniques for implementing the baluns and summing junctions required by the modulator. Finally the chapter concludes with simulations and measurement results of the fabricated IC, along with suggestions for further improvements.

3.2 Direct-Digital QPSK Modulator Concept

The concept of the proposed QPSK modulator is based on our previous work on direct-digital BPSK modulators using hybrid microwave circuits and MEMS single-pole double-throw (SPDT) switches [47], [48]. A block diagram of the direct-digital QPSK modulator is shown in Figure 3.1. It consists of: 1) a 90° phase shifter, 2) two baluns, 3) two pairs of complementary switches, and 4) a summing junction. A major advantage of this topology is its relative simplicity in terms of size and power consumption compared to most other QPSK modulators. This potentially yields a compact modulator IC with

significant savings in size and cost of the transmitter. It is also possible to attain a relatively low DC power consumption with this architecture if passive phase shifters are used, making it attractive for portable communication devices as it prolongs their battery life. Furthermore, since digital modulation is performed directly at the high carrier frequency, more signal bandwidth is potentially available for higher data rates. Therefore as CMOS technology continues to provide faster switching transistors, increasingly high transmission rates are possible for future high-speed wireless applications.

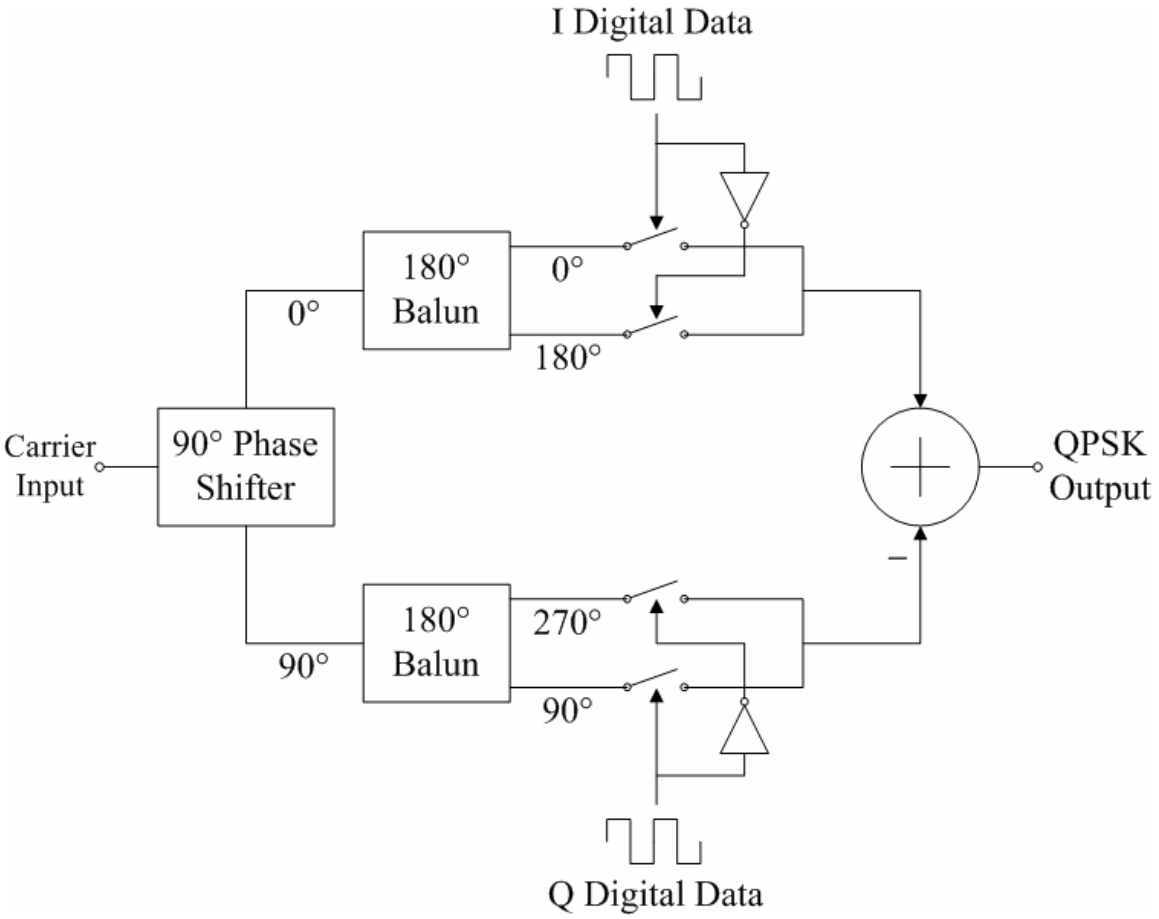

Figure 3.1: QPSK modulator concept.

As shown in Figure 3.1, the 90° phase shifter first creates two quadrature signals from the input RF carrier: $\cos(\omega_{RF}t)$ and $\sin(\omega_{RF}t)$. Each quadrature signal is then split in

the baluns into balanced signals, yielding differential quadrature phases of the carrier: $\pm\cos(\omega_{RF}t)$ and $\pm\sin(\omega_{RF}t)$. One signal from each differential quadrature pair, $\pm\cos(\omega_{RF}t)$ and $\pm\sin(\omega_{RF}t)$, is later selected in the complimentary switch networks according to the in-phase (I) and quadrature-phase (Q) digital data values respectively. Finally, the chosen signals are subtracted in the summing junction at the output. In effect, the circuit implements the following QPSK function:

$$QPSK(t) = I(t)\cos(\omega_{RF}t) - Q(t)\sin(\omega_{RF}t), \tag{3.1}$$

where $I(t)$ and $Q(t)$ represent the in-phase (I) and quadrature-phase (Q) bit streams in time with a value of -1 for logic 0 and +1 for logic 1. It is important to note that the arithmetic operation in (3.1) is merely inconsequential, i.e. either an addition or subtraction can be chosen as long as it is performed using complex vector arithmetic. The reason for choosing the subtraction is that it is very easily accomplished using a differential pair of transistors.

3.3 Direct-Digital QPSK Modulator Design

In this section, the design of the L-band QPSK modulator in CMOS will be described with detailed analysis of its various components including the 90° phase shifter, the baluns, the complimentary switch networks and the summing junction. In addition, important design considerations will be stressed wherever appropriate.

3.3.1 Quadrature Phase Shifter

The resistor-capacitor, capacitor-resistor (RC-CR) network is chosen for generating quadrature carriers due to its simple design, small IC footprint and zero DC power consumption. It is also useful for overcoming phase errors caused by fabrication

tolerances as explained later. Figure 3.2 [25] shows the integrating (RC) and differentiating (CR) circuits involved. In this figure, Z_{01} and Z_{02} are the impedances of the input and output networks, while R and C are the resistance and capacitance of the integrating and differentiating circuits. The in-phase (V_I) and quadrature-phase (V_Q) outputs are given by [25]:

$$\frac{V_I}{V_{IN}} = \frac{1}{\left(1 + \frac{R}{Z_{02}} + \frac{Z_{01}}{Z_{02}}\right) + j\omega C\left(R + Z_{01}\right)} \tag{3.2}$$

$$\frac{V_Q}{V_{IN}} = \frac{1}{\left(1 + \frac{Z_{01}}{R} + \frac{Z_{01}}{Z_{02}}\right) + \frac{1}{j\omega C}\left(\frac{1}{R} + \frac{1}{Z_{02}}\right)}. \tag{3.3}$$

If the loading impedance Z_{02} is made significantly larger than both the resistance R and the source impedance Z_{01} i.e. $Z_{02} >> (R, Z_{01})$, then the phase difference θ between the two output signals V_I and V_Q is given by:

$$\begin{aligned} \theta &= \angle V_Q - \angle V_I \\ &\approx 90° - \tan^{-1}\left(\omega C\left(R + Z_{01}\right)\right) + \tan^{-1}\left(\omega C\left(R + Z_{01}\right)\right) \\ &= 90° \end{aligned} \tag{3.4}$$

as required. This equation shows that the phase difference is at a constant 90° with no frequency dependence, allowing this phase shifter to operate over a wide bandwidth. Furthermore, it is independent of the resistance R or capacitance C making it insensitive to tolerances of the fabrication process. However it should be noted that any mismatch in resistors or capacitors between the two circuits will introduce phase errors as can be seen from (3.4). In addition, capacitive coupling between the two networks will contribute

further to these phase errors. Therefore careful layout is required to minimize these effects [6].

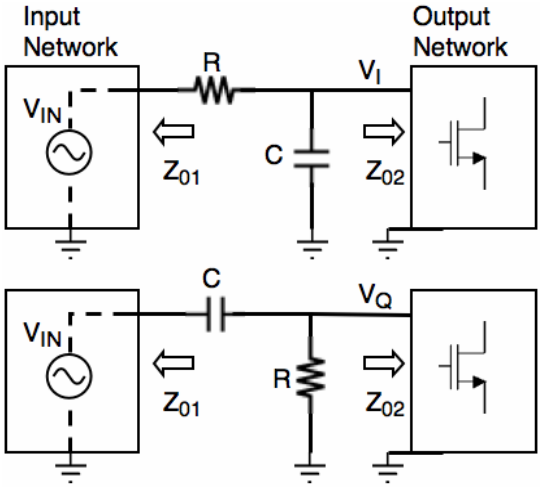

Figure 3.2: Integrating and differentiating RC networks of the phase shifter.

While a 90° phase difference can be readily achieved with this network over a wide bandwidth, it is important to consider the amplitudes of the output signals V_I and V_Q. The amplitude ratio G is given by:

$$G = \left|\frac{V_Q}{V_I}\right| \approx \frac{\sqrt{1+(\omega C(R+Z_{01}))^2}}{\sqrt{\left(1+\frac{Z_{01}}{R}\right)^2+\left(\frac{1}{\omega CR}\right)^2}} \qquad (3.5)$$

$$= \omega CR$$

where the same assumption is made that $Z_{02} >> (R, Z_{01})$. This equation shows that amplitude balance (G = 1) can only achieved at the cutoff frequency of ω = 1/(RC), which is inherently dependent on the resistance R and capacitance C. Therefore the amplitude match of the two outputs is sensitive to component tolerances in the fabrication process, further emphasizing the need for careful layout.

The two outputs V_I and V_Q of the *RC-CR* network are buffered using active FETs in a common-drain (source follower) configuration as shown in Figure 3.3. Large AC

coupling capacitors are used to block the DC bias from the input and output, and the biasing resistor R_G is also large enough not to attenuate the input signal significantly. The input impedance looking into the gate of the common-drain circuit is typically very high, presenting a large loading impedance Z_{02} to reduce the insertion loss through the 90° phase shifter. The buffers are also necessary to sufficiently drive the following low input impedance baluns, which are discussed next.

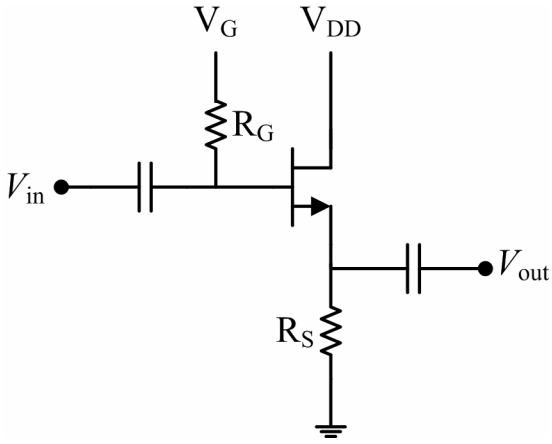

Figure 3.3: Common-drain (source-follower) FET as a buffer.

3.3.2 Baluns

The proposed QPSK modulator requires a balun to generate 180° out-of-phase signals from each quadrature carrier as shown in Figure 3.1. The accuracy of this 180° phase split will affect the modulator's performance including its modulation bandwidth. Many baluns have been reported in the literature to convert an unbalanced, single-ended signal to a pair of balanced, differential signals that are needed for a variety of applications including modulators and mixers. These include: 1) centre-tapped transformers, 2) microwave distributed networks and 3) active circuits using transistors. Each of these approaches has respective advantages making it more appropriate for the application at hand based on the frequency of operation, available area, cost, and power

consumption. Centre-tapped transformers illustrated in Figure 3.4 operate on the principle of magnetic induction and are commonly used at lower RF frequencies up to a few GHz [49]-[52]. The centre of the secondary coil is tapped and grounded so that the input voltage V_1 is split evenly between the output voltages V_2 and V_3 with a 180º phase difference between them. Although these passive transformers consume zero DC power, they can be physically large and generally have high losses. Nevertheless they can be made smaller by using ferrite iron cores, which raises the cost and requires packaging.

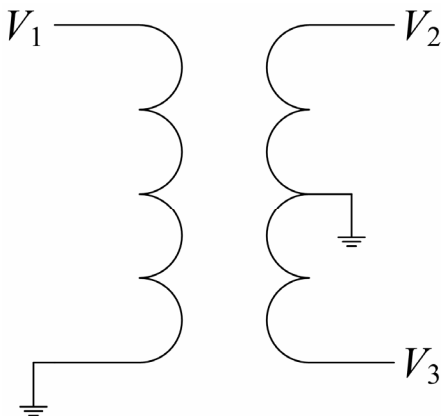

Figure 3.4: Centre-tapped transformer balun.

Microwave distributed networks such as the classic [35] and tapered coupled line 180° ring hybrids [35] using planar transmission lines (e.g. microstrip or coplanar waveguides) can provide a very precise 180° phase shift over a wide frequency range [35]. A typical 180° ring hybrid is shown in Figure 3.5, which consists of four ports matched to the system impedance Z_0 around a ring of characteristic impedance $(\sqrt{2})Z_0$. The input is applied to port 4 so that the signal is split equally into two components with a 180° phase difference between them at ports 2 and 3, while port 1 is isolated. As the input power is divided evenly (i.e. by a factor of ½) between the two output signals, the voltage conversion loss of this network is at least $1/\sqrt{2}$ or 3dB. Although a thorough

quantitative analysis may be carried out to find the S-parameters and verify the network's operation, the procedure can be easily found in any text such as [35]. Here an intuitive explanation will suffice. As the input signal enters port 4, it travels a distance of 3λ/4 to reach port 2 whereas it travels only λ/4 to reach port 3. Therefore the phase difference between the two signals appearing at ports 2 and 3 is λ/2 or 180° as required. For port 1, the signal at port 4 is divided into two components that traverse two different paths around the ring, one of length λ/2 and the other of length λ. The phase difference between these two components is again λ/2 or 180°, canceling each other out when they combine at port 1 and therefore isolating it. An advantage of 180° ring hybrids and microwave distributed networks in general is that they are well established theoretically and can be readily designed with excellent model-to-hardware correlation. However, these hybrids are large for monolithic IC integration especially at lower RF and microwave frequencies where the wavelength λ is in the order of centimeters. For this reason, they are not often used in IC designs.

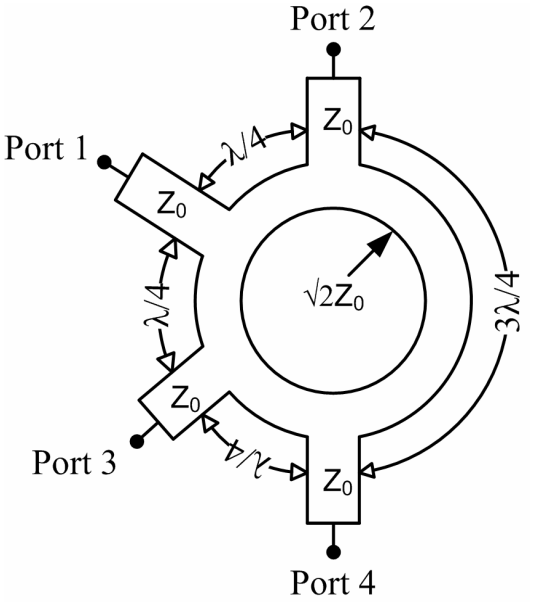

Figure 3.5: 180° ring hybrid in microstrip form.

Active baluns employ field-effect transistors (FETs) in a certain configuration to create 180° out-of-phase signals from a single-ended input. A major advantage of active baluns is one of conversion gain, reduced area and ease of IC integration. Compared to transformer and transmission line baluns, they can be very compact especially at low RF frequencies where passive structures can be quite large. However, the FETs will inherently add thermal and 1/f noise to the output signals. They will draw DC current as well contributing to the power consumption of the modulator and the overall transmitter. Nonetheless they allow the modulator to be integrated on-chip serving towards a fully integrated direct-digital transmitter that is very compact and inexpensive. The simplest single-transistor balun is shown in Figure 3.6 [53]. It consists of a FET with load resistors connected to the source and drain and the input applied to the gate. The input signal V_{in} is transferred in-phase to the source but 180° out-of-phase to the drain. At low frequencies, the hybrid-π model shown in Figure 3.7 is adequate to perform a small signal analysis and derive the following tractable expressions for the output voltages V_{out1} and V_{out2}:

$$\frac{V_{out1}}{V_{in}} \approx g_m\left(R_s \| \frac{1}{g_m}\right) = \frac{R_s}{R_s + \frac{1}{g_m}} \tag{3.6}$$

$$\frac{V_{out2}}{V_{in}} \approx \frac{\frac{1}{g_m}}{R_s + \frac{1}{g_m}}\left(-g_m R_d\right) = -\frac{R_d}{R_s + \frac{1}{g_m}} \tag{3.7}$$

where g_m is the transconductance of the FET, R_s is the resistance at the source and R_d is the resistance at the drain. These equations show that the output signals will indeed be

180° out of phase independent of component values, but for them to have equal amplitudes, i.e. $|V_{out1}| = |V_{out2}|$, the following condition must to be satisfied:

$$R_s = R_d \tag{3.8}$$

In addition, to reduce the conversion loss as much as possible towards unity-gain, i.e. $|V_{out1}/V_{in}| = |V_{out2}/V_{in}| \approx 1$, the transconductance g_m of the FET should be increased so that $R_s >> 1/g_m$ or $g_m >> 1/R_s$. This is typically achieved using a larger FET width W with high current consumption, I_{DS}. However for higher frequencies a more careful analysis is needed that includes the parasitic capacitances of a physical MOSFET illustrated in Figure 3.8 [54]. A high-frequency hybrid-π model can then be derived based on this as shown in Figure 3.9. It is clear that as the frequency increases, the impedance of the gate-drain capacitance C_{gd} decreases, allowing part of the input signal to pass directly to the drain. This causes the phase reversal of V_{out2} to deviate appreciably from 180°. Such a discrepancy will degrade the performance of the balun and the proposed modulator. Moreover, there are other parasitics in the FET that can contribute further to this phase imbalance. In conclusion, the balun in Figure 3.6 is an attractive solution at low to moderate RF frequencies below 1GHz or so, depending on the device technology.

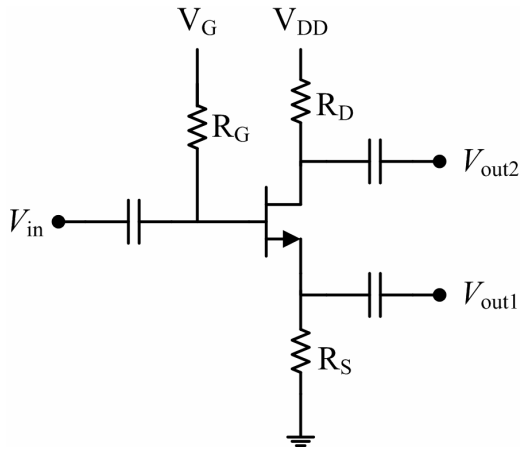

Figure 3.6: Circuit schematic of single-transistor balun.

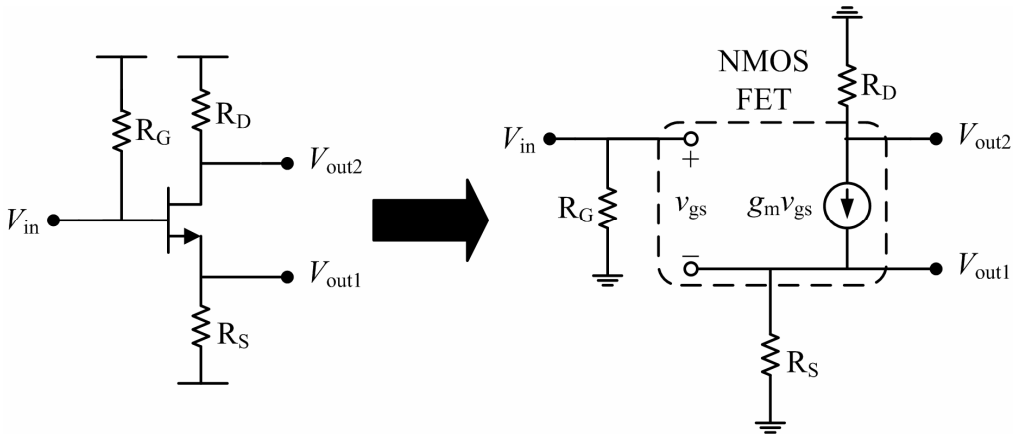

Figure 3.7: FET hybrid-π model.

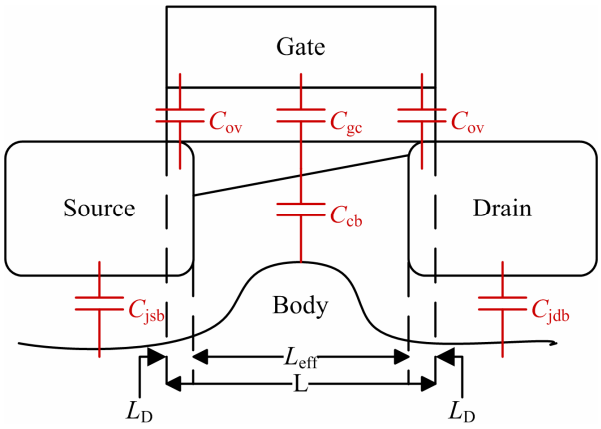

Figure 3.8: Intrinsic parasitic capacitances of a physical FET.

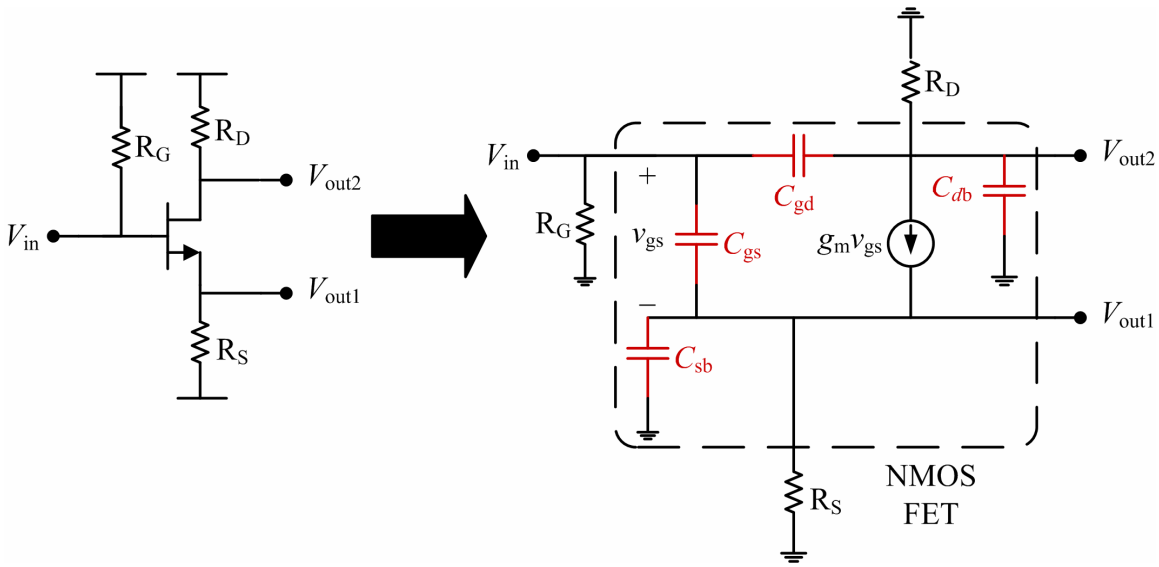

Figure 3.9: FET high-frequency model with parasitic capacitances.

More common active baluns that have better performance than single-transistor circuits take on the form of a common-gate, common-source (CG-CS) pair or a differential pair with one input AC grounded [55], [56]. In the CG-CS configuration, the common-gate transistor amplifies the input signal in-phase while the common-source one amplifies it with a phase reversal. By matching the gain of these amplifiers, the two outputs can have equal amplitudes. A schematic of a CG-CS pair designed in previous work [57] and used in this QPSK modulator is shown in Figure 3.10 below.

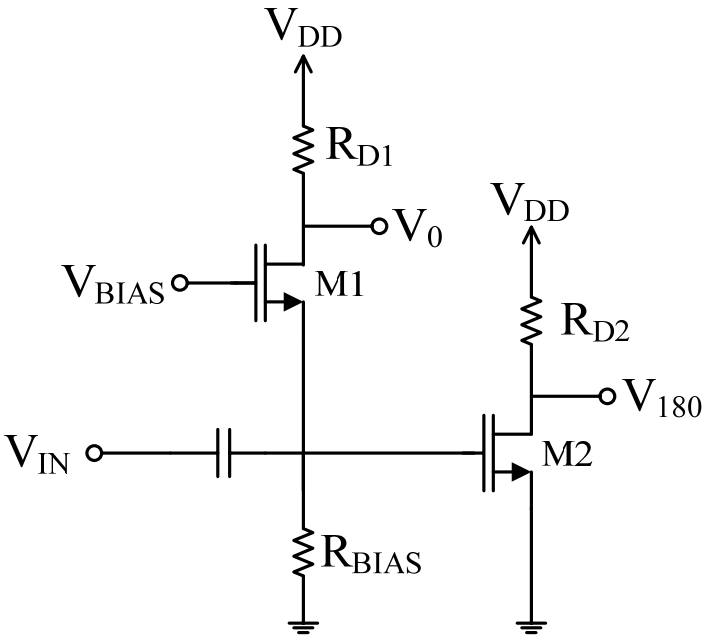

Figure 3.10: Common-gate, common-source (CG-CS) active balun.

The input impedance looking into the source of the common-gate FET is approximately given by $1/g_m$. Therefore the common-gate device can be designed with the appropriate size and bias current to yield a low input resistance close to the 50Ω system impedance. The biasing source resistance R_{bias} is also chosen large enough not to greatly affect the input impedance or attenuate the signal. As the low impedance of this common-gate circuit is in parallel with the very high impedance of the common-source device, it

dominates the overall input impedance of the balun. Thus it provides a low reflection coefficient so that most of the signal power is absorbed and not reflected [57]. In contrast, the input impedance looking into a single-transistor or differential-pair balun is very high making the reflection coefficient rather poor. A matching network must therefore be implemented in this case using passive structures such as inductors, capacitors or transmission lines, occupying a large area on the IC and defeating the main advantage of active baluns. Furthermore, the input match provided by the common-gate circuit is typically broadband as opposed to narrowband in passive networks, albeit the reflection coefficient could be higher at the centre frequency [35], [57].

The active balun circuit was designed and simulated in Agilent Advanced Design System (ADS) software using Taiwan Semiconductor Manufacturing Company (TSMC) 0.18μm RF CMOS BSIM3 device models for the transistors. The full circuit schematic of the balun is shown in Figure 3.11 below. It includes a source follower circuit at each output acting as a buffer. An S-parameter simulation was run from 1GHz to 10GHz with 50Ω ports at the input and outputs as shown in Figure 3.11. The resulting difference in phase and magnitude of the transmission coefficients S_{21} and S_{31} from the input to the outputs, i.e. the phase and amplitude balance of the balun, are plotted in Figures 3.12 and 3.13 respectively. As depicted from Figure 3.12, the phase difference is quite flat and reaches a maximum of about 181.8° for a low discrepancy of 1.8° from the desired 180°. Figure 3.13 shows that the amplitude ratio between the two output signals is within 0.2dB over the same frequency band. These results indicate that this balun is relatively wideband for this technology. The magnitude of the input reflection coefficient S_{11} is also shown in Figure 3.14, with a value less than about -8dB over the entire frequency

range from 1GHz to 10GHz. This is a significantly lower than that achieved by a single-transistor or differential-pair balun, which is close to 0dB indicating that most of the input power is reflected away.

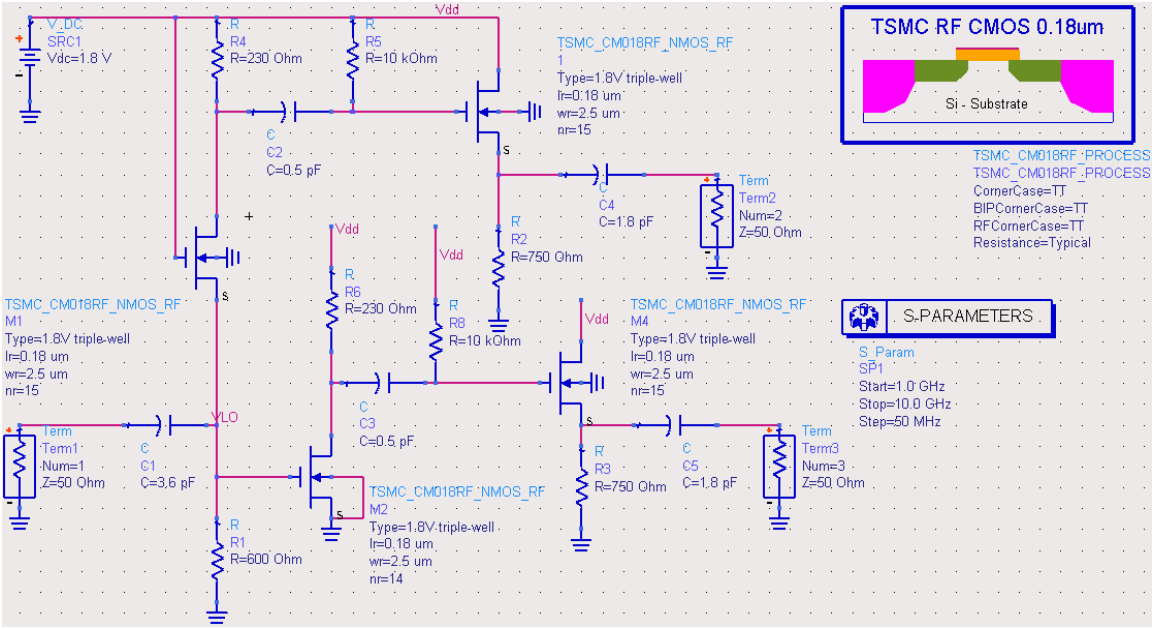

Figure 3.11: Balun circuit schematic in ADS.

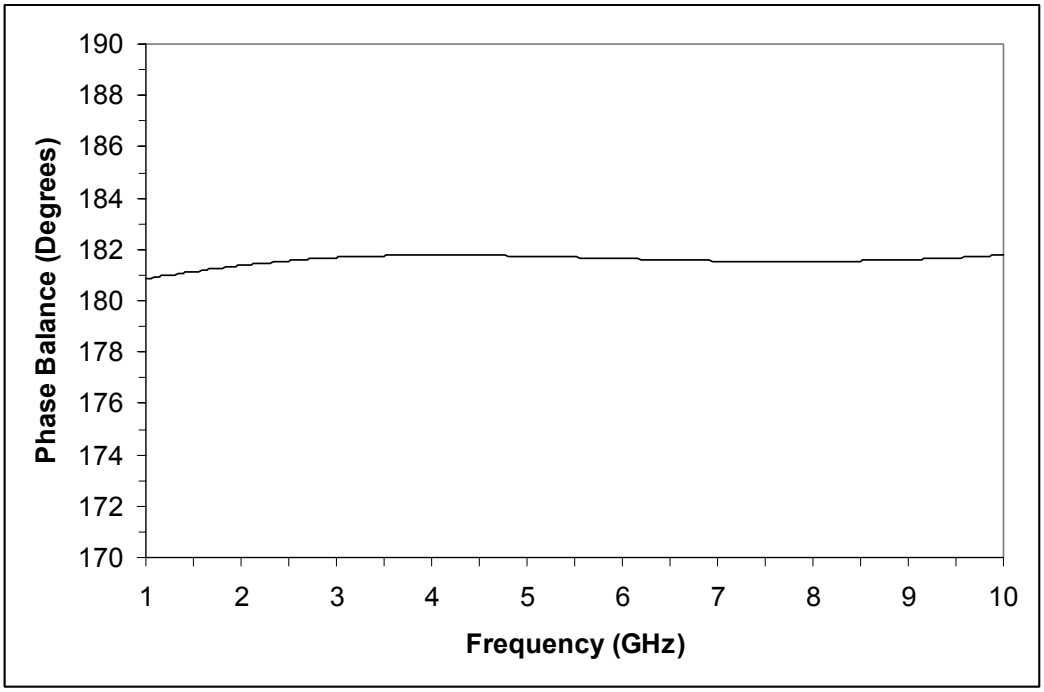

Figure 3.12: Simulated CG-CS balun phase balance from 1GHz to 10GHz.

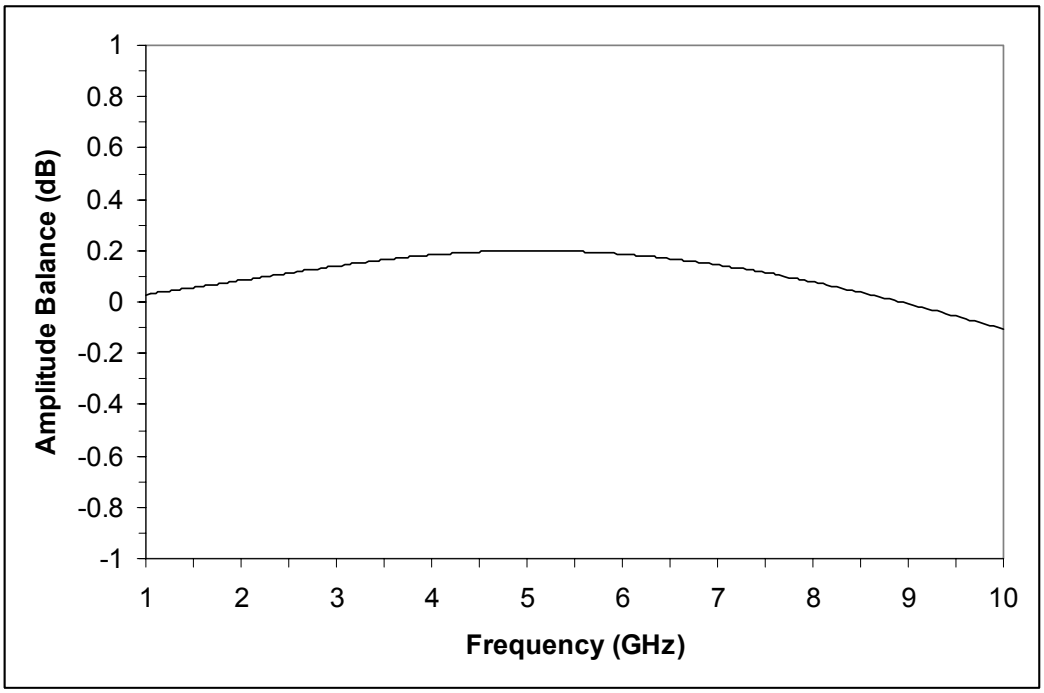

Figure 3.13: Simulated CG-CS balun amplitude balance from 1GHz to 10GHz.

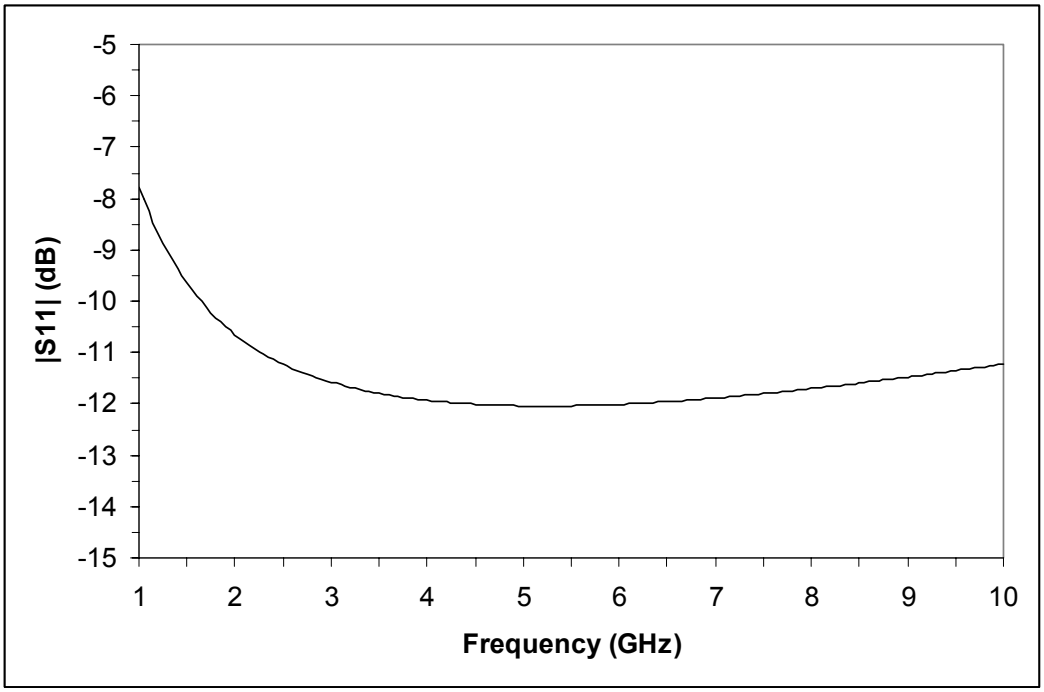

Figure 3.14: Simulated balun input reflection coefficient from 1GHz to 10GHz.

3.3.3 Complimentary Switch Networks

The purpose of the *I*, *Q* complimentary switch networks is to pass one signal from each quadrature balanced pair ($\pm\cos(\omega t)$ and $\pm\sin(\omega t)$), while blocking the other one. In particular, the in-phase signal $\cos(\omega t)$ or $\sin(\omega t)$ is passed for a binary digit of $I = 1$ or $Q = 1$, while the out-of-phase signal $-\cos(\omega t)$ or $-\sin(\omega t)$ is passed for $I = 0$ or $Q = 0$ thus creating the $I(t)\cos(\omega t)$ or $Q(t)\sin(\omega t)$ product term in (3.1). The two selected quadrature carriers can then be subtracted to generate the QPSK vector signal as shown in the next section.

Each complimentary switch network is essentially a Pass-Transistor Logic (PTL) circuit consisting of a pair of NMOS switches as shown in Figure 3.15, which have the advantages of small footprint, zero DC power consumption and high-speed operation. An NMOS FET can be naturally used as a switch, with the path of interest being between the source and drain of the device and the state controlled by the voltage applied to the gate (Figure 3.16). If the gate-to-source voltage (V_{GS}) is less than the threshold voltage V_T, no channel is created between the drain and source, and the device is said to be operating in the cut-off region. The switch is therefore in the OFF state, and can be simply modeled as an open circuit. On the other hand, if the gate voltage is well above the threshold V_T, e.g. at the supply voltage V_{dd}, a uniform channel is created between the drain and source, and the device is operating in the triode or linear region. The switch in this case is ON as the signal readily passes through the small channel resistance. The drain-to-source current-voltage (I_{DS}-V_{DS}) characteristic of the NMOS FET in this state (triode region) can be written as [1]:

$$I_{DS} = \frac{\mu_n C_{ox}}{1 + V_{DS}/(LE_{sat})} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} {V_{DS}}^2 \right] \tag{3.9}$$

where μ_n is the electron mobility, C_{ox} is the gate oxide capacitance per unit area, W and L are the width and length of the NMOS transistor, E_{sat} is the velocity saturation electric field, V_{GS} is the gate-to-source voltage, and V_T is the threshold voltage. Since the drain-to-source voltage (V_{DS}) is significantly smaller than the gate overdrive voltage ($V_{GS}-V_T$) and the velocity saturation voltage (LE_{sat}), this equation can be approximated as:

$$I_{DS} \approx \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T) V_{DS} . \tag{3.10}$$

From equation (3.10) above the NMOS switch can be simply modeled as a resistance R_{DS} in the ON state (Figure 3.16) given by:

$$R_{DS} = \left(\left. \frac{\partial I_{DS}}{\partial V_{DS}} \right|_{v_{gs}=0} \right)^{-1} \approx \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)} , \tag{3.11}$$

where the applied gate-to-source voltage V_{GS} is equal to the supply voltage V_{DD} in this case:

$$R_{DS} \approx \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{DD} - V_T)} . \tag{3.12}$$

It is clear from (3.12) that increasing the device width W as much as possible would minimize the switch's on-resistance R_{DS} and thus reduce the signal loss across it. However at high frequencies a more careful analysis is necessary that includes the most important intrinsic parasitic capacitances of the FET (Figure 3.8) in the switch model as shown in Figure 3.17 [58]. The gate-to-source (C_{gs}) and gate-to-drain (C_{gd}) capacitances in the model are given by [54]:

$$C_{gs} = C_{gd} = \frac{1}{2}C_{gc} + C_{ov} \approx \frac{1}{2}C_{ox}WL_{eff} + C_{ox}WL_D, \tag{3.13}$$

where C_{gc} is the gate-to-channel capacitance, C_{ov} is the overlap capacitance of the gate oxide with the drain or source diffusion, L_{eff} is the effective channel length and L_D is the diffusion overlap length. The factor of ½ is present as the channel is uniform in the triode region as opposed to pinched off at the drain in the saturation region (Figure 3.8); so the total gate-to-channel capacitance $C_{gc} = C_{ox}WL_{eff}$ can be split evenly between the source and drain. While the overlap capacitance $C_{ov} = C_{ox}WL_D$ has been traditionally neglected due to its small value compared to the gate-to-channel capacitance C_{gc}, it is becoming more significant as the device length L scales down from one technology generation to the next. Regardless, it is still clear from (3.13) that as the width W of the device is made larger, the gate-to-source (C_{gs}) and gate-to-drain (C_{gd}) capacitances increase, reducing their impedance and allowing more of the RF signal to be shorted to AC ground. This leads to a higher signal loss adversely affecting the performance of the QPSK modulator. Therefore a trade-off between these two effects is necessary and a medium device size of ten 2.5µm-wide fingers is used.

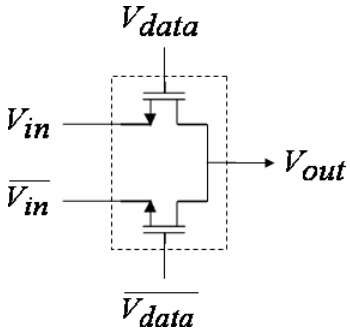

Figure 3.15: Pass-Transistor Logic (PTL) circuit with NMOS switches.

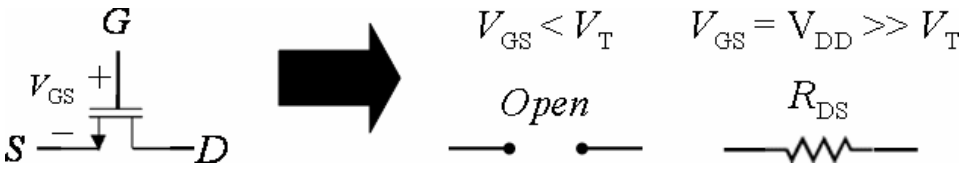

Figure 3.16: NMOS FET switch operation and model.

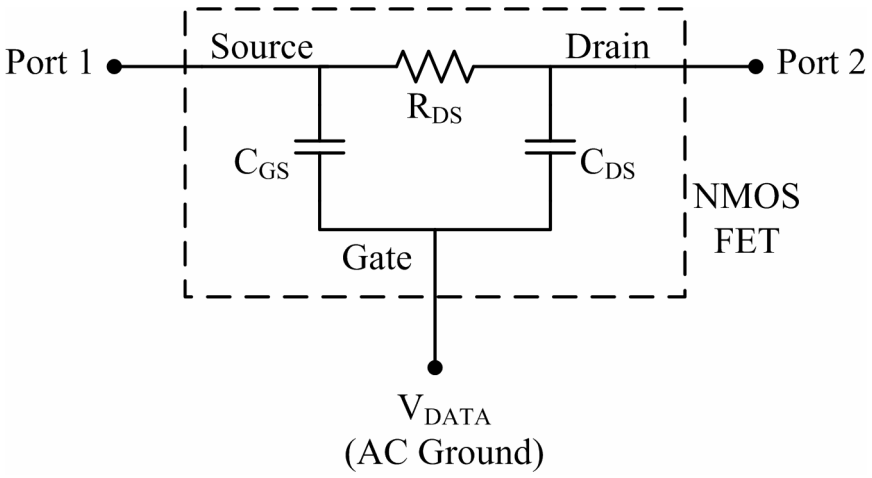

Figure 3.17: High-frequency model of NMOS switch.

3.3.4 Summing Junction

A summing junction is required by the QPSK modulator to combine (subtract) the two quadrature signals selected by the input data. This should be performed with sufficient accuracy so as not to degrade the performance of the QPSK modulator significantly. Many passive summing junctions have been reported in the literature to add or subtract signals for various RF/Microwave circuits including mixers. Among them are transmission-line networks, such as the ring hybrid, T-junction and the Wilkinson power combiner. The 180° ring hybrid shown in Figure 3.5 for example can be operated as a combiner with the input signals applied to ports 2 and 3, so that the sum of the signals is formed at port 1, while the difference is formed at port 4. The T-junction shown in Figure 3.18 is a simpler three-port network that is also implemented using

planar transmission lines, but it suffers from poor input match and very low isolation between the two input ports, allowing the signals to interfere with each other. The Wilkinson power combiner (Figure 3.19) offers good isolation between the two inputs as well as an impedance match for all three ports at the design center frequency. Other networks such as transformers and lumped-element circuits (resistor and/or capacitors) have also been used. The centre-tapped transformer in Figure 3.4 for example can be operated as a combiner with the two inputs applied to V_2 and V_3, so that their difference is generated at V_1. Resistors or capacitors connected in a T-network configuration (Figure 3.20) provide a simple solution as well. However the insertion loss of these combiners can be excessively high.

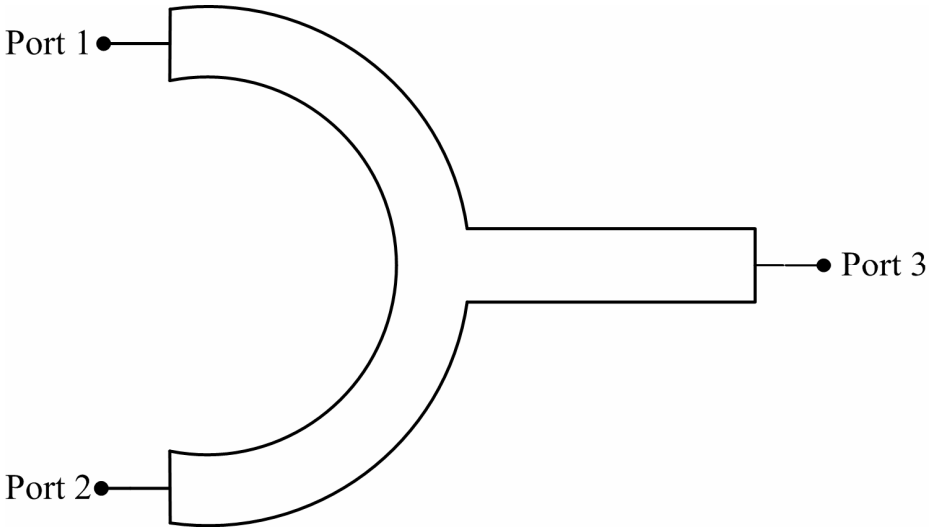

Figure 3.18: T-Junction using transmission lines.

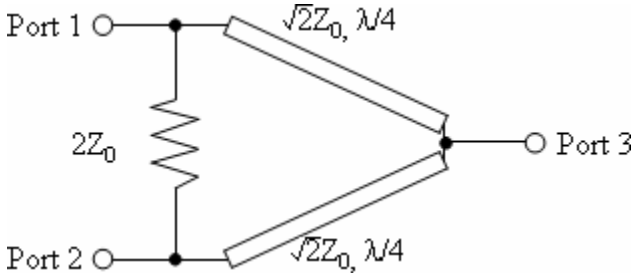

Figure 3.19: Wilkinson power combiner.

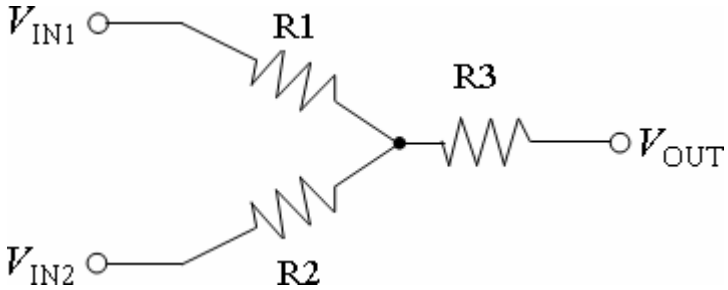

Figure 3.20: Resistor T-junction.

An active difference circuit using FETs is employed in this work as opposed to a passive combiner, since the latter can be quite large at this frequency band to integrate on-chip. It can also provide insertion gain albeit at the cost of DC power consumption, noise and large-signal distortion. Figure 3.21 below shows the circuit schematic of the summing junction with the DC bias networks omitted for clarity. It consists of a differential pair amplifier and an output buffer using only five transistors and resistors making its size comparatively small for IC integration.

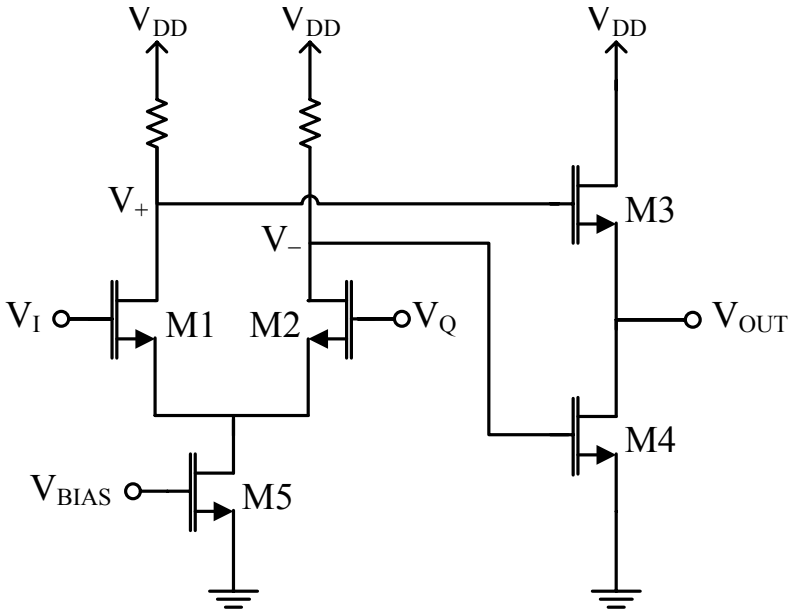

Figure 3.21: Differential amplifier and output buffer as a summing junction.

The differential pair amplifier subtracts the quadrature outputs of the complimentary switch networks ($I(t)\cos(\omega t)$ and $Q(t)\sin(\omega t)$) and generates the resultant QPSK signal vector ($QPSK(t)$) as in (3.1). Figure 3.22 below illustrates this vector subtraction process. The intrinsic parasitics of the FETs, particularly the gate-to-source capacitance C_{gs}, provides a capacitive path between the quadrature inputs V_I and V_Q of the differential pair as shown in Figure 3.23. This essentially pulls the quadrature phases closer together creating a phase and amplitude imbalance at the inputs, which in turn translates to discrepancies upon subtraction at the output. Such capacitive coupling can cause significant phase and amplitude errors if the output impedance of the preceding stage is not sufficiently small. Therefore buffering the baluns using source followers (Figure 3.3) lowers their output impedance and minimizes this effect. In addition, choosing a small width W for the FETs helps to reduce capacitive parasitics and coupling between the inputs. However, a smaller FET exhibits a lower transconductance, reducing the conversion gain of the differential pair.

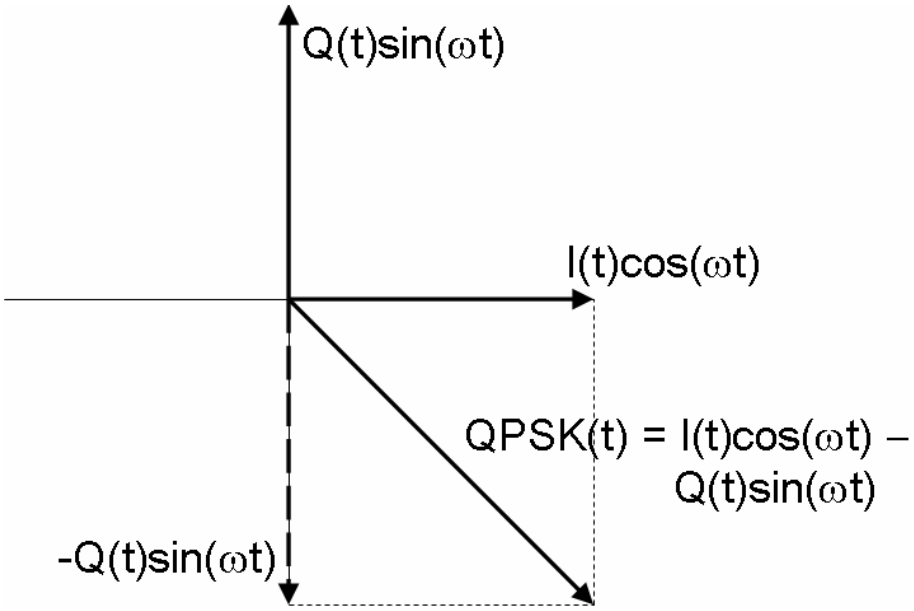

Figure 3.22: Vector subtraction performed by summing junction.

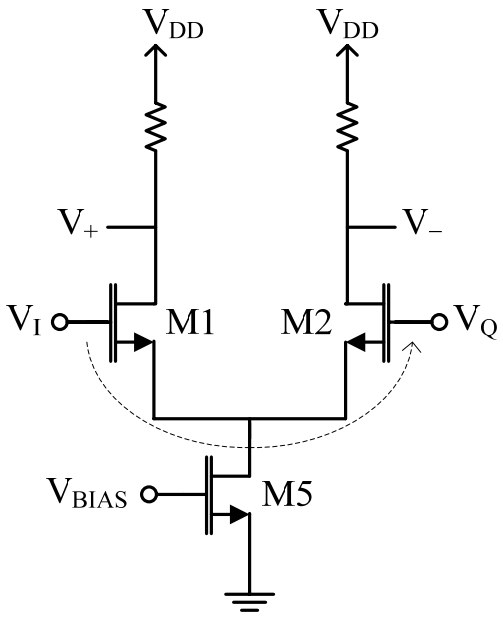

Figure 3.23: Capacitive path between differential amplifier inputs.

The differential amplifier also eliminates traces of spurious signals and noise that are in common-mode. However, the outputs of the differential pair (V_+, V_-) should be taken differentially (i.e. $V_+ - V_-$) and not single-ended for this to happen. Doing so also provides a larger signal swing for a higher transmission gain. Therefore an output buffer of common-drain and common-source devices converts the differential outputs to a single-ended one and drives the external 50Ω load. The common-drain device transfers the positive voltage (V_+) while the common-source device inverts the negative one (V_-) so that the two signals combine in-phase at the load. The output impedance looking into the source of the common-drain FET is approximately given by $1/g_m$. Thus the common-drain device can also be designed with the appropriate size and bias current to yield a low output resistance close to 50Ω. As the low impedance of the common-drain FET (M3) is in parallel with the relatively large impedance of the common-source device (M4), it dominates the overall output impedance of this buffer stage. This presents a low

reflection coefficient over a wide bandwidth as opposed to using a conventional matching network.

3.4 QPSK Modulator Simulation and Measurement Results

In this section, the simulation and testing procedure of the L-band QPSK modulator circuit in 0.18μm CMOS technology will be discussed in detail. The acquired results from these simulations and measurements will be presented along with important practical considerations.

3.4.1 QPSK Modulator Simulation

The QPSK modulator design was simulated in Agilent Advanced Design System (ADS) software using Taiwan Semiconductor Manufacturing Company (TSMC) 0.18μm RF CMOS BSIM3 device models for the transistors. The full circuit schematic of the QPSK modulator is shown in Figure 3.24. To verify the circuit's operation, a time-domain simulation was run with a 1.7GHz, -20dBm sinusoidal signal source for the carrier, and 100Mbps pseudo-random binary sequences (PRBS) to mimic random digital data at the I and Q inputs. These sequences were encoded in the non-return-to-zero (NRZ) format with rectangular pulses having a low level of 0V (ground) for logic 0 and a high level of 1.8V (V_{dd}) for logic 1. It is important to note that a high data rate of 100Mbps was necessary for this simulation because of the speed and memory constraints of the computer system. The difficulty arises from the widely different frequencies involved: tracing the fast-varying carrier signal long enough to obtain adequate information about the relatively slow modulating signal can be computationally expensive.

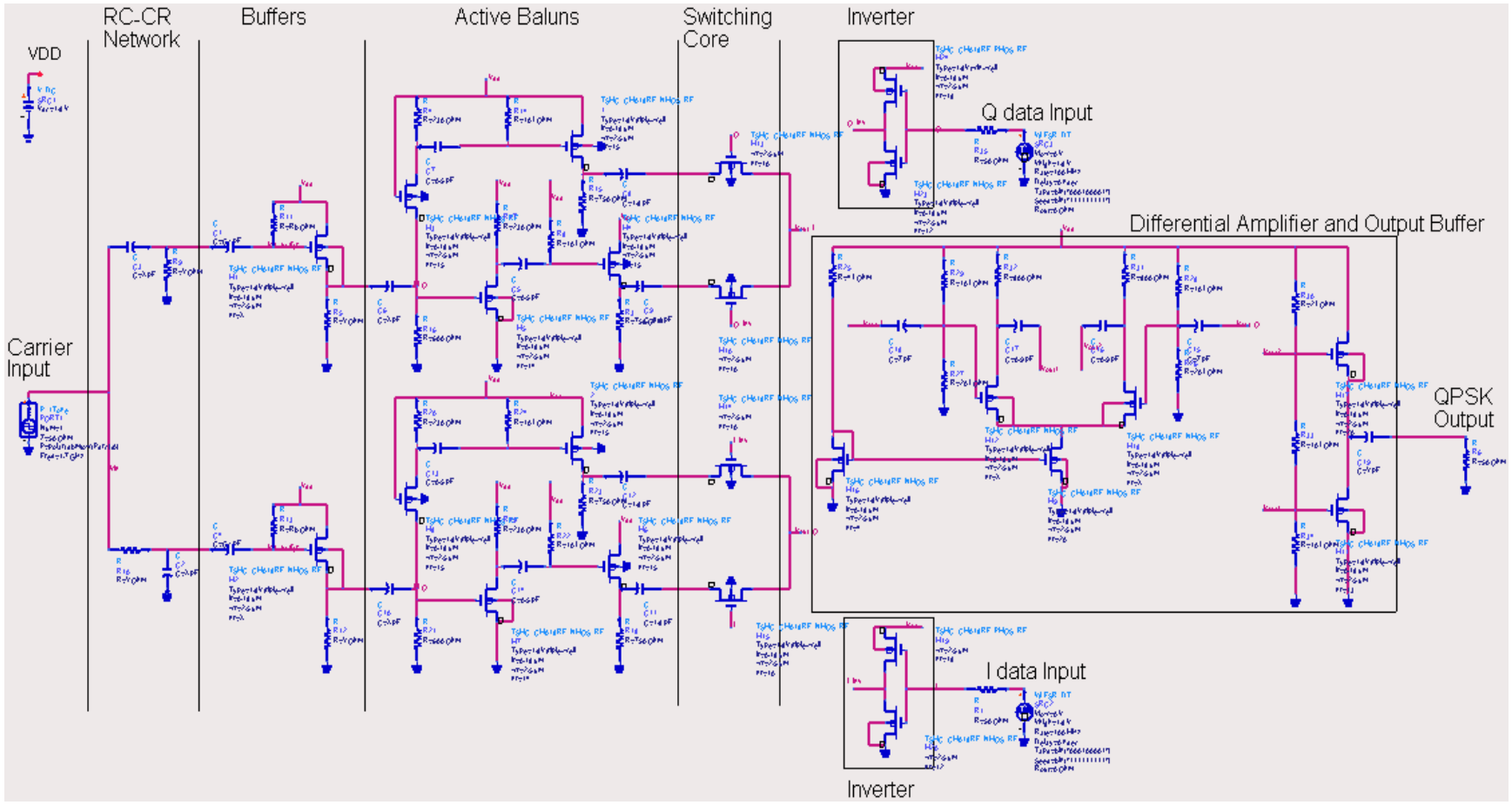

Figure 3.24: Full QPSK modulator schematic in ADS.

For instance, with the carrier frequency at 1.7GHz, the maximum simulation time step can only be around 0.05ns if 10 data points are required per cycle. To cover 200 symbols (dibits) of data at a much lower modulation rate, say 1Mbps, a total simulation time of 200μs or 4×10^6 points is required. Such a large amount of processing can exhaust the computer's resources or take a very long time, becoming more of a problem if the carrier frequency is increased. However at 100Mbps, the number of data points needed is only 40000, which significantly reduces computational time and memory requirements.

The generated time-domain plot for the modulator's output voltage at the 50Ω load (Figure 3.24) is shown in Figure 3.25, with a focus on the phase traversals of the carrier signal. The frequency spectrum of this modulated signal over 200 pseudo-random symbols (dibits) is illustrated in Figure 3.26. This reveals a typical QPSK spectrum that matches the theoretical power spectrum discussed in Chapter 2 (Figure 2.13), verifying the design of our proposed modulator.

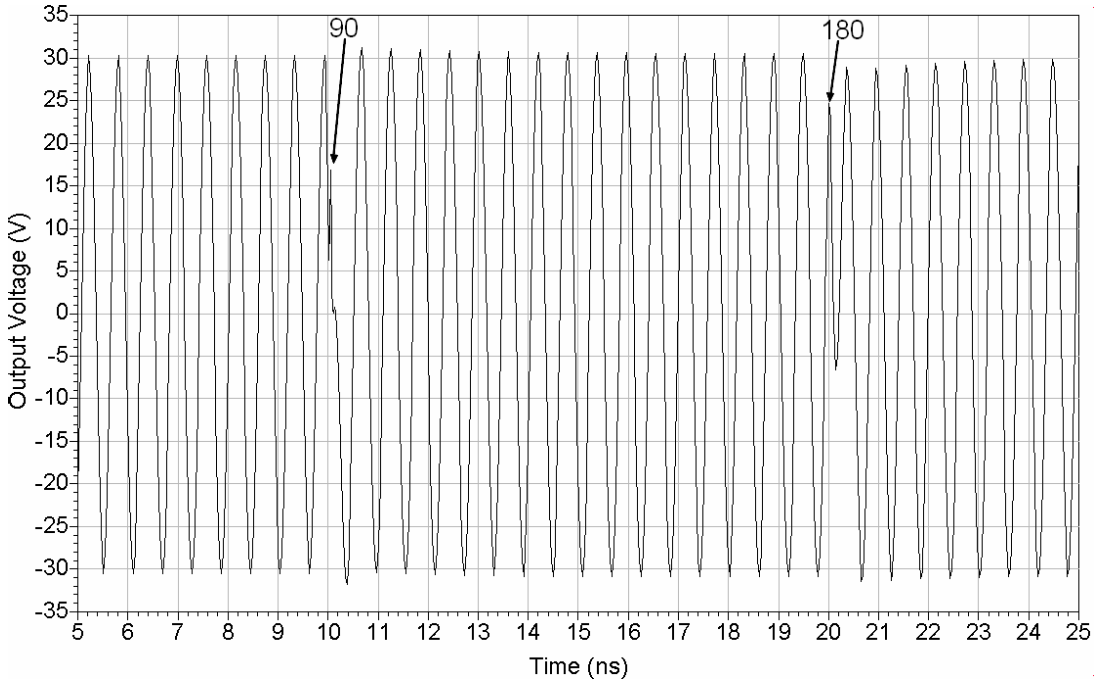

Figure 3.25: Simulated QPSK time-domain signal.

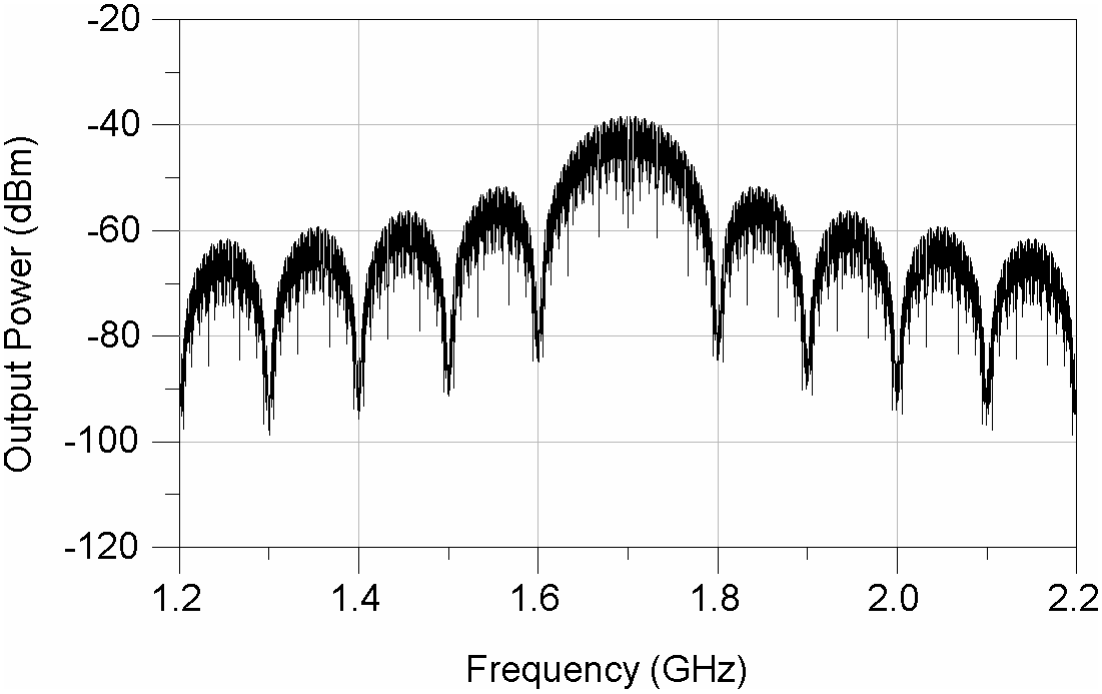

Figure 3.26: Simulated QPSK spectrum at 100Mbps.

To view the signal constellation of the QPSK modulator's output, an envelope simulation was set up in ADS using the same signal sources for the carrier and digital data. The simulation was run for 8 symbol periods at 100Mbps, or 80ns in total. The resulting constellation of the modulator's output voltage is shown in Figure 3.27, with the generated points very close to the ideal QPSK constellation discussed in Chapter 2 (Figure 2.11), further verifying the design of our QPSK modulator. From the phase values marked on each point in the plot, the maximum phase error is approximately 5° between adjacent (quadrature) points and about 1.8° between opposite (complimentary) points. Similarly, the maximum amplitude imbalance between all four points is about 1.04 or 0.3dB. As the lowest voltage amplitude is about 14.8mV, the power available at the 50Ω load is -26.6dBm, which implies that the signal exhibits a loss of 6.6dB from a -20dBm input. Nevertheless the phase and amplitude imbalance are comparatively small, ensuring adequate modulation accuracy and bandwidth.

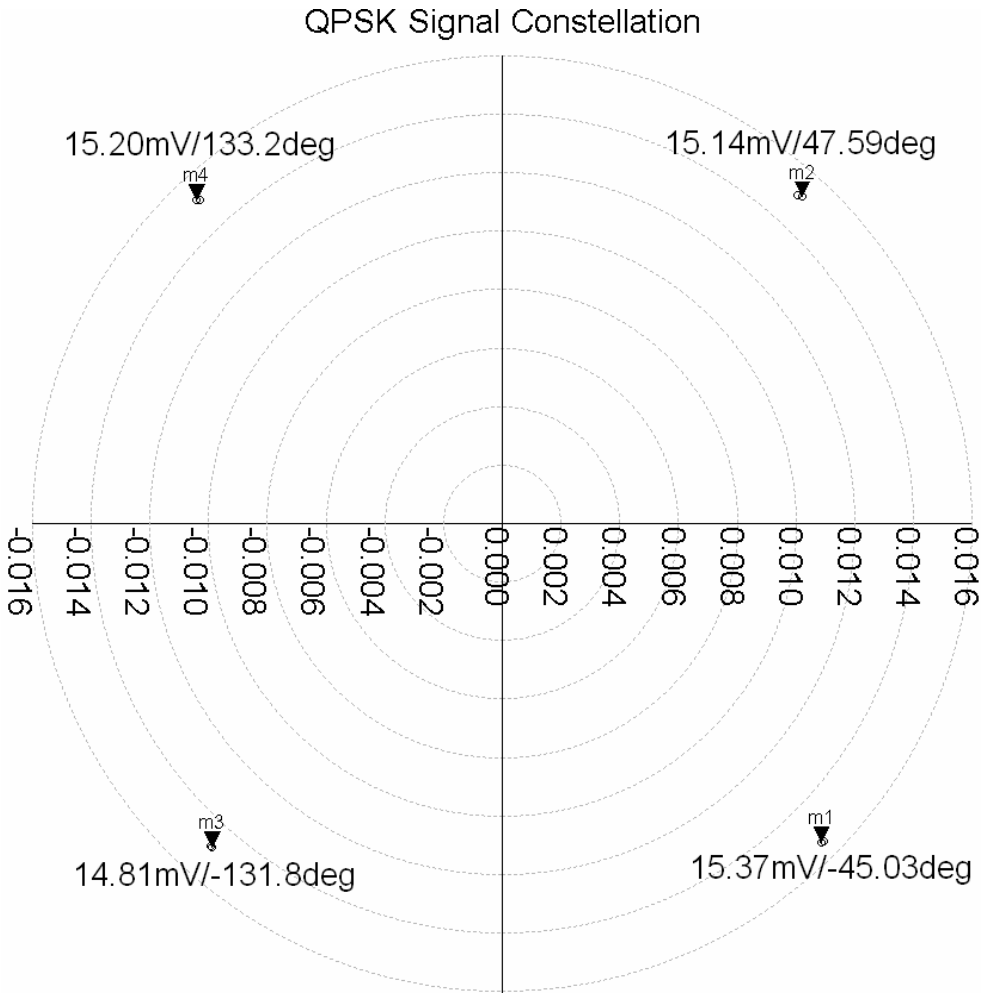

Figure 3.27: Simulated QPSK Signal Constellation at 100Mbps.

3.4.2 QPSK Modulator Test and Measurement

The QPSK modulator was fabricated in a standard (six-metal, single-poly) 0.18μm CMOS process. A photograph of the IC is shown in Figure 3.28. It occupies a die area of about 0.425 × 0.675mm without bonding pads and 0.425 × 0.825mm with bonding pads included. The circuit consumes less than 24mA of current from a 1.8V voltage supply, i.e. 43mW of power.

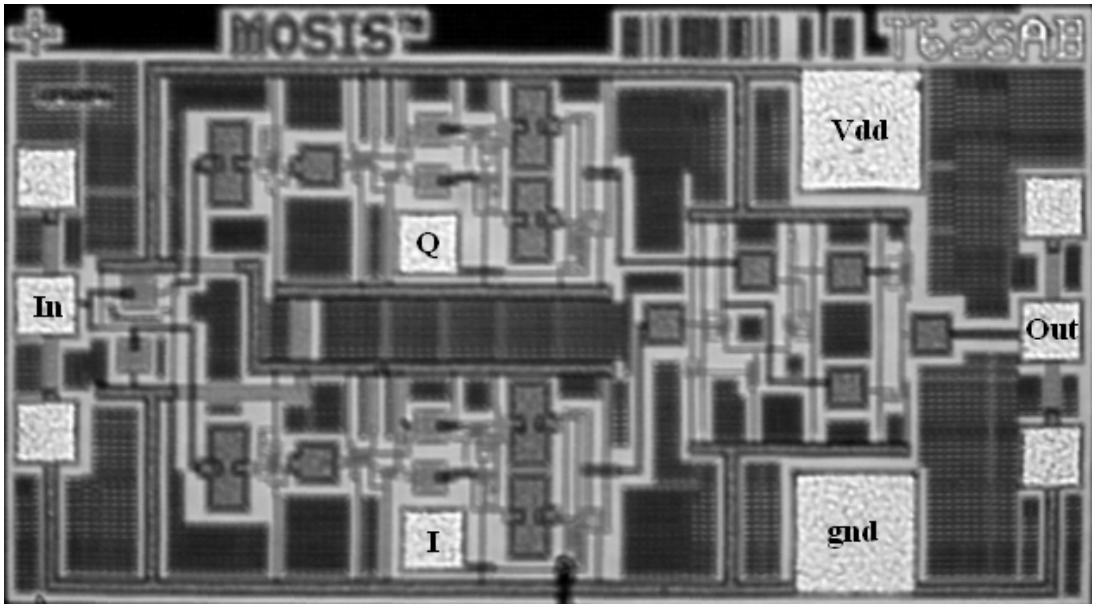

Figure 3.28: Photograph of L-Band QPSK modulator IC.

To test the QPSK modulator IC, a direct on-wafer measurement was carried out using Cascade Microtech coplanar waveguide (CPW) probes and DC probes on a Wentworth probe station. An Anritsu signal generator (model MG3694A) and Tektronix arbitrary function generator (model AFG310) were used to apply the input carrier signal and digital data signals respectively. To examine the output signal spectrum, the Agilent E4446A spectrum analyzer was used. Finally, a vector network analyzer (Agilent 8510C) was employed for all S-parameter measurements including QPSK signal constellations and reflection coefficients. Prior to the VNA measurements, a full two-port SOLT calibration was performed using a SUSS MicroTec calibration substrate.

The first measurement performed was the loss through the modulator while the I and Q data switches are held at constant values to generate the base QPSK constellation signal, corresponding to the symbol (dibit) value of $I = 1$ and $Q = 1$. A high voltage level (1.8V) representing logic 1 is applied to both I and Q data channels, connecting the 0° and 90° paths to the summing junction for combination at the output, as depicted in

Figure 3.1. The magnitude of the transmission coefficient from the input to the output (S_{21}) in this state is shown in Figure 3.29 from 1.5GHz to 1.9GHz. It is clear that the loss exhibited at the centre frequency of 1.7GHz is about 8.2dB, which is relatively close to simulation and not overly excessive, at least when compared to other QPSK modulators. If we consider the equal four-way power split of a signal by a passive solution for example, the minimum theoretical loss is already 6dB, and in addition there are parasitic losses through the silicon substrate, metal conductors and switches that could increase the total loss beyond the 6-8dB range. The input reflection coefficient (S_{11}) was also measured in this state and a similar plot of its magnitude is shown in Figure 3.30. At the centre frequency of 1.7GHz, the reflection coefficient is quite high at about -4.5dB. This is due to the relatively high input impedance presented by the RC-CR network. While a high reflection coefficient is generally not desirable, it should be noted that in the context of a typical direct-digital transmitter, the on-chip local oscillator (LO) will be preceding this QPSK modulator instead of a 50Ω signal generator. So a relatively high loading impedance from the perspective of the LO could be advantageous for increased voltage swing. Nevertheless, this reflection coefficient will be significantly improved upon in the enhanced S-band modulator by ensuring an adequate impedance match to 50Ω, as discussed in more detail in Chapter 4.

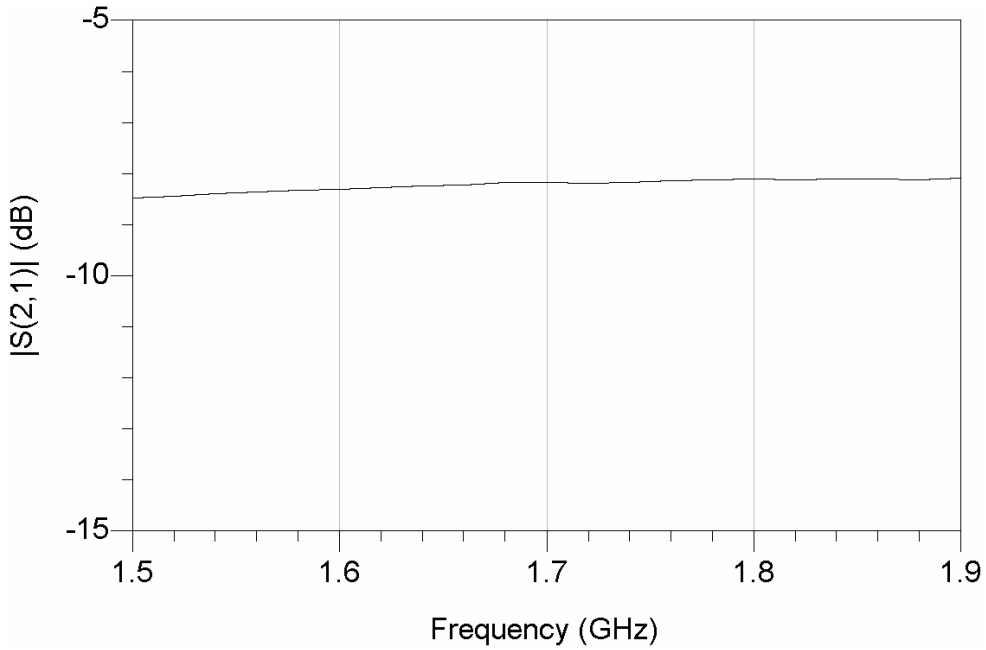

Figure 3.29: Measured S21 for the base QPSK symbol (I = 1, Q = 1).

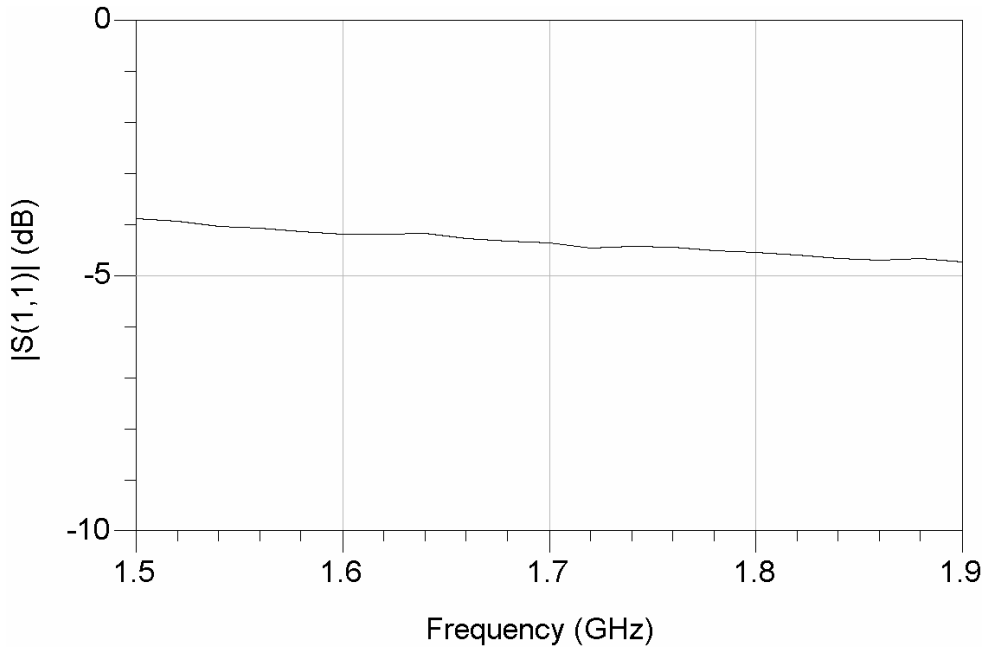

Figure 3.30: Measured S11 for base QPSK symbol (I=1, Q=1).

To assess the 90° phase difference and amplitude match of two quadrature signals in the QPSK constellation, the switches were held fixed at the same base state with the transmission coefficient S_{21} measured, then the switches were toggled for the adjacent

constellation point of I = 1, Q = 0, and S_{21} was again measured. For the first state, a high voltage level of 1.8V was applied for both I and Q data inputs as before, but in the second state, the voltage for the Q input is switched to 0V for logic 0. The difference in the phase of the measured transmission coefficient S_{21} in each state is plotted in Figure 3.31 over a span of 400MHz around the centre frequency. As depicted from the plot, the phase difference reaches about 84.7° for a relatively low phase error of 5.3°, in close agreement with our simulation results presented earlier. The magnitude ratio between these transmission coefficients is also plotted on a similar graph in Figure 3.32, indicating a low amplitude imbalance of 0.4dB at around the same frequency.

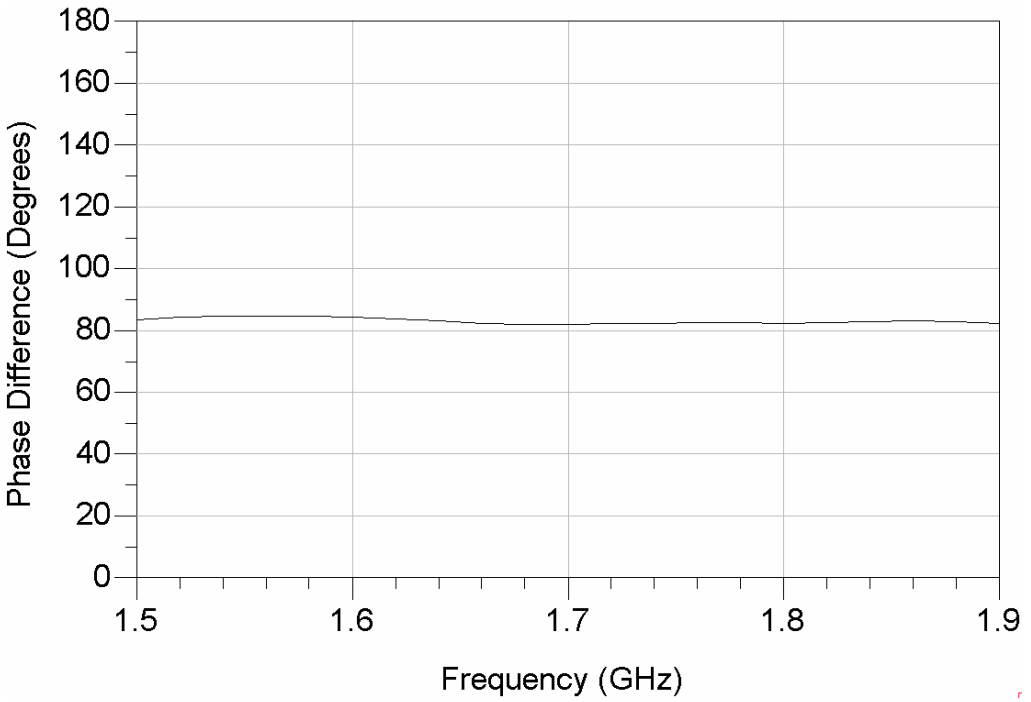

Figure 3.31: Measured phase difference between quadrature QPSK signals.

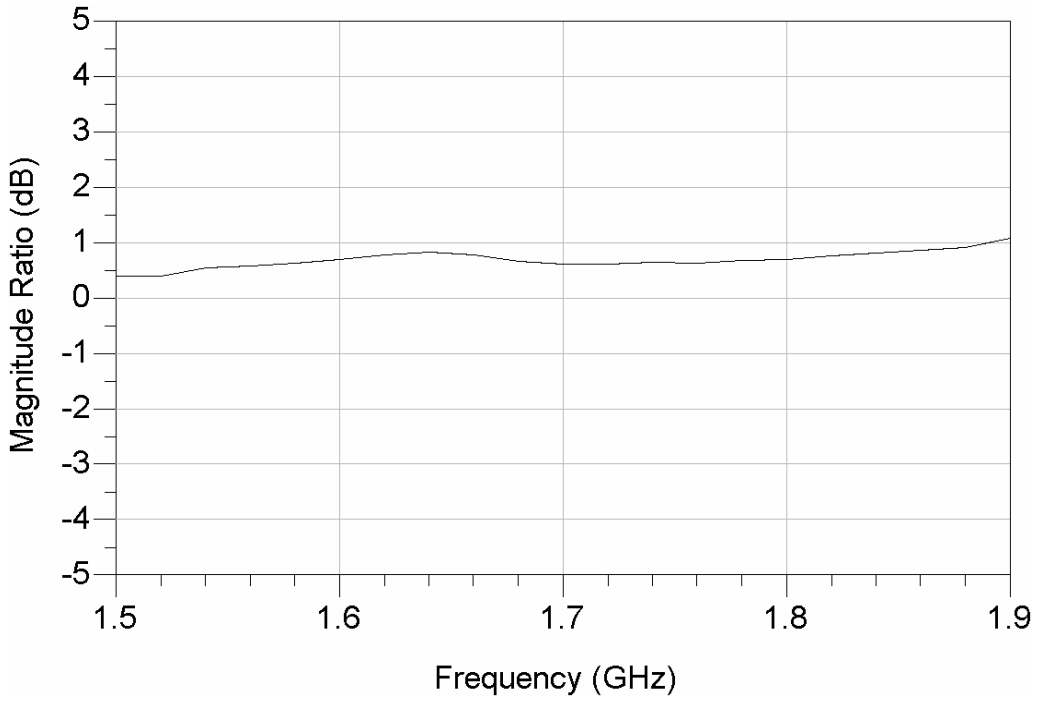

Figure 3.32: Measured amplitude imbalance between quadrature QPSK signals.

While the quadrature phase match is probably the most important feature of the QPSK constellation, it is still necessary to examine the 180° phase difference between opposite points in the constellation. In this test, the switches were again held fixed at the same base state while the transmission coefficient S_{21} was measured, then the switches were toggled for the opposite constellation point of I = 0, Q = 0 and S_{21} was again measured. For the first state, a high voltage level of 1.8V was applied for both I and Q data inputs as before, but in the second state their voltage is switched to 0V for logic 0. The difference in the phase of the measured transmission coefficient S_{21} in each of these states is plotted in Figure 3.33 over a span of 400MHz around the centre frequency. As depicted from this plot, the best phase difference reaches about 179° for a very low phase error of 1°. The magnitude ratio between these transmission coefficients is also plotted similarly in Figure 3.34, indicating an amplitude imbalance of 1.7dB at around the same frequency. This is equivalent to an absolute ratio of 1.2 which is actually quite

significant. Such discrepancies are largely the result of component tolerances, device mismatches and asymmetries in the circuit, which are usually accounted for in a second design cycle. However in our modified S-band modulator, a tunable solution is adopted to trim these errors as much as possible, as described in Chapter 4.

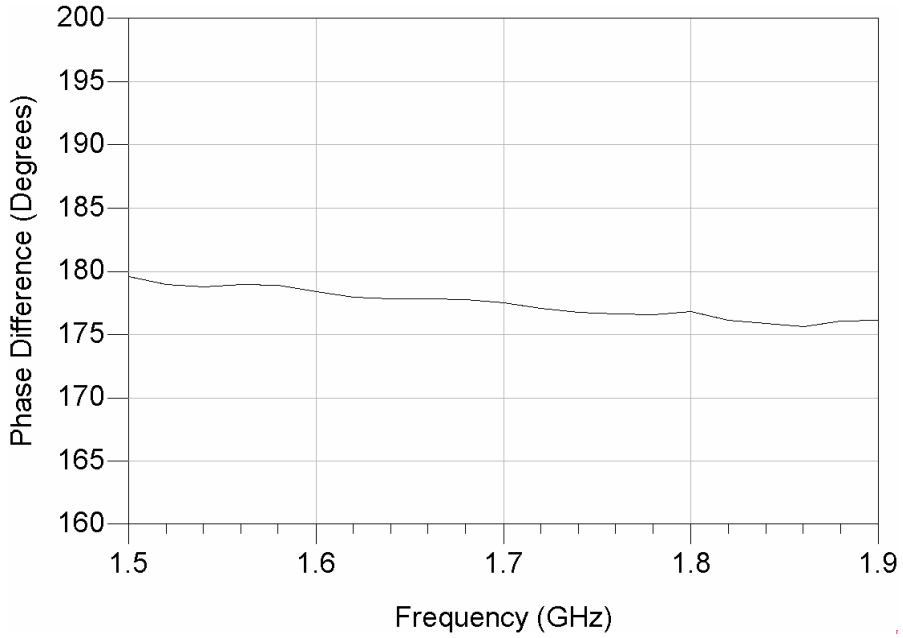

Figure 3.33: Measured phase difference between complimentary QPSK signals.

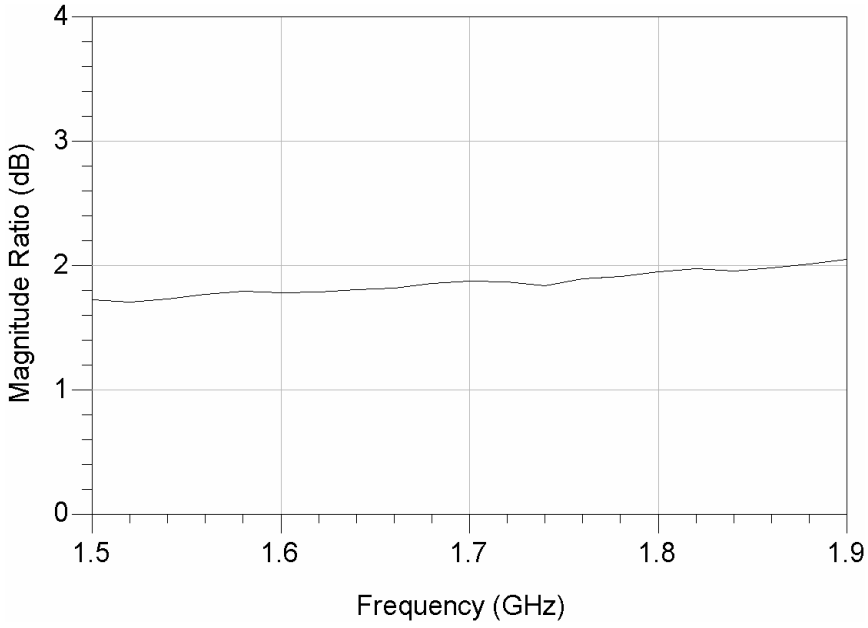

Figure 3.34: Measured amplitude imbalance between complimentary signals.

To measure the QPSK modulator's carrier rejection, the same square wave is applied to both I and Q data channels, with an amplitude level of 1.8V (V_{dd}) in the high state and 0V (ground) in the low state. At 1.8V the NMOS switches are fully turned on, while at 0V they are practically off. The output of the IC is then connected directly to the spectrum analyzer. The frequency of the square wave f_{MOD} is chosen to be 0.5MHz (time period $T = 1/f_{MOD} = 2\mu s$) for a 1Mbps data rate per channel or a total data throughput of 1Mbps × 2 channels = 2Mbps. From Fourier signal analysis, the frequency spectrum of an ideal periodic square wave has non-zero components only at the odd-order harmonics of the fundamental frequency (0.5MHz, 1.5MHz, 2.5MHz and so on), featuring a sinc-shaped amplitude envelope. This spectrum is shifted in frequency by the carrier upon modulation. Figure 3.35 shows the resulting output signal spectrum with a centre (carrier) frequency of 1.76GHz, a frequency span of 25 MHz and resolution bandwidth of 240kHz. The spectrum shape is quite good with a high degree of symmetry around the centre frequency. As depicted from the plot, the carrier at 1.76GHz is also well suppressed by more than 40dB relative to the main lobes at 1.76GHz ± 0.5MHz.

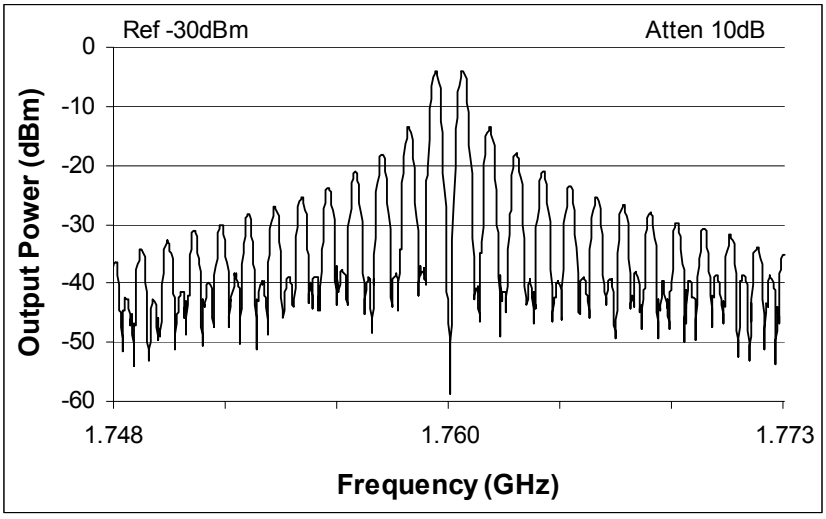

Figure 3.35: Plot of the measured carrier rejection.

However, although relatively small, a few imperfections are apparent in the output spectrum shown in Figure 3.35, including non-zero even-order components. This is most likely due to the limited bandwidth of DC probes and its associated dispersive effects on the digital signals. Other non-idealities include the finite rise and fall times of the generated square wave, along with the finite switching time of the NMOS switches, which allow both paths in a complimentary pair to be simultaneously on. Such intervals can be significant compared to the symbol period involved (1μs), possibly contributing to the discrepancies observed in the output spectrum.

As the transmitted information in real-world communication systems is most often random as opposed to periodic, further tests were carried out. Pseudo-Random Binary Sequences (PRBS) with a 9-bit shift register were employed to mimic random digital data for the input I and Q channels. The sequences were encoded in the non-return-to-zero (NRZ) format with rectangular pulses having an amplitude level of 0V (ground) in the low state and 1.8V (V_{dd}) in the high state. Their data rate was set to be 10Mbps (pulse width $T = 1/f_{MOD} = 0.1\mu s$) for a total data throughput of 10Mbps × 2 channels = 20Mbps. Finally, the output of the IC was directly connected to the spectrum analyzer. Figure 3.36 shows the resulting output signal spectrum with a centre frequency of 1.76GHz and a frequency span of 100MHz. The resolution bandwidth and averaging of the spectrum analyzer were set to 910kHz and 100 points respectively. It is evident that the circuit operates as a QPSK modulator with its generated spectrum closely matching the theoretical QPSK power spectrum discussed in Chapter 2 (Figure 2.13). The output spectrum is also quite smooth with little or no imperfections in its sinc-squared shape.

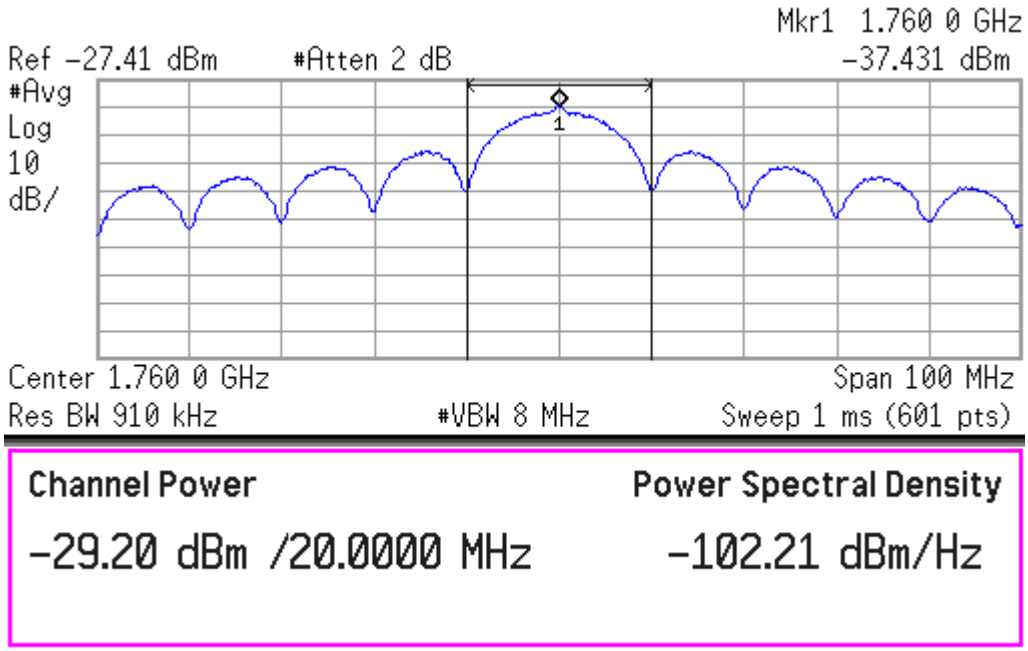

Figure 3.36: Measured output QPSK spectrum for 20Mbps.

The QPSK modulator was also tested at higher speeds. For a data rate of 16Mbps per channel or 32Mbps total, which is the highest frequency setting on the arbitrary function generator, the measured output spectrum of the modulator is as shown in Figure 3.37. While the main (center) lobe of the spectrum remains mostly intact, there are visible discrepancies in the side lobes due to practical non-idealities. The low bandwidth of DC probes has definitely limited the maximum data rate that can be tested for this QPSK modulator. To alleviate this problem and enable higher data rates, high-performance CPW probes are used to apply the digital data signals on the IC for the enhanced S-band modulator, as discussed in Chapter 4.

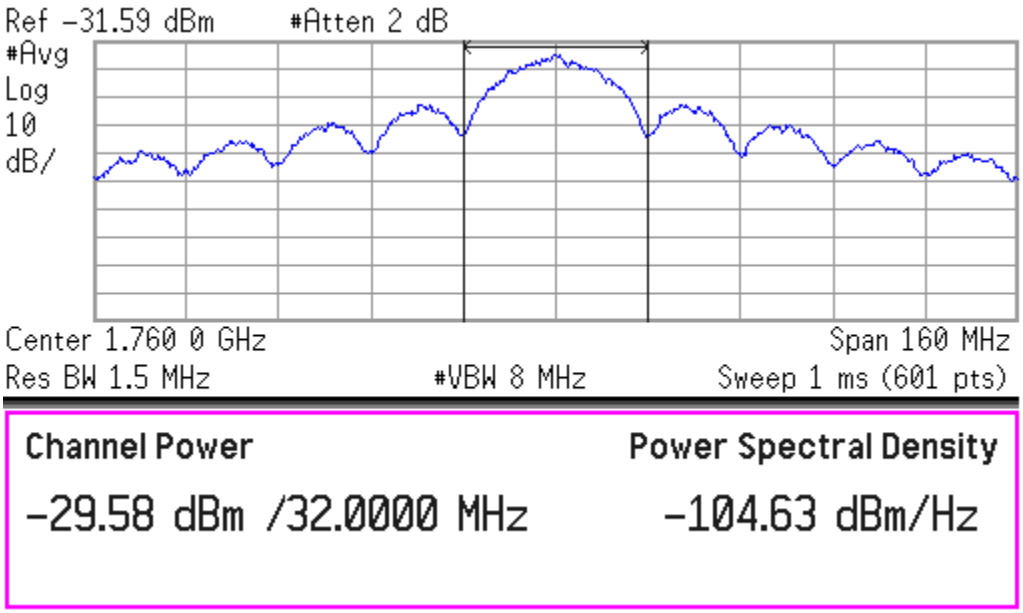

Figure 3.37: Measured output QPSK spectrum for 32Mbps.

Table 3.1 below summarizes the measured characteristics of the L-band QPSK modulator.

Table 3.1: Summary of measured characteristics of L-band QPSK modulator.

Characteristic	Results
Active Area	0.425 × 0.675mm
DC Power Consumption	43mW from 1.8V
Insertion Loss	8dB
Carrier Rejection	> 40dB
Data Throughput	Nominal: 20Mbps Maximum: 32Mbps

Chapter 4

S-Band Direct-Digital QPSK Modulator

4.1 Introduction

This chapter introduces a novel direct-digital QPSK modulator concept which offers several benefits over our previous work discussed in Chapter 3. It then describes the design of an S-band modulator in 0.18μm CMOS technology that demonstrates this new concept. Finally, the chapter concludes with simulations and measurement results of the fabricated IC, presenting the improved performance achieved over our original modulator.

4.2 New Direct-Digital QPSK Modulator Concept

The proposed concept for the new QPSK modulator builds on our previous work described in Chapter 3. A block diagram illustrating it is shown in Figure 4.1. It consists of: 1) a 180° balun, 2) a 90° phase shifter and 3) a switch network. The main advantage of this topology is its relative simplicity compared to our previous QPSK modulator, as it requires only one balun and no summing junction. This potentially yields a more compact modulator IC with additional savings in size and cost of the transmitter. In addition, a lower DC power consumption can be attained if a passive 90° phase shifter is

used, making it more attractive for portable communication devices that are battery-powered. Furthermore, since the need for a summing junction is completely eliminated, its associated non-idealities are no longer present, enabling higher modulation accuracy and data rates for more ambitious wireless applications.

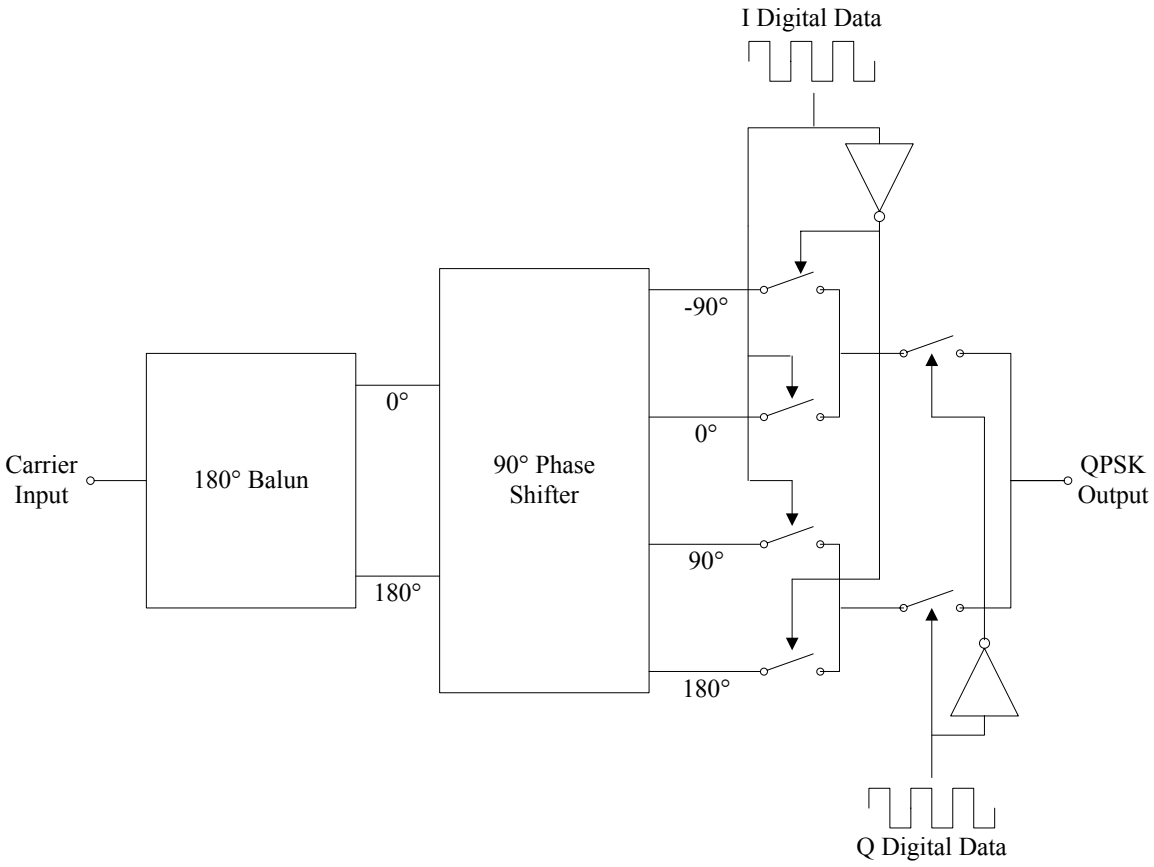

Figure 4.1: QPSK modulator concept.

As shown in Figure 4.1, the 180° balun first splits the input RF carrier into a pair of differential, balanced signals. These signals are then fed to the 90° phase shifter which generates differential quadrature signals, yielding all four quadrature phases of the carrier: 0°, -90°, 90° and 180°. Only one from the four differential quadrature signals is later selected in the switch network according to both in-phase (*I*) and quadrature-phase (*Q*) digital data values, which constitute the QPSK symbol (dibit) value. This eliminates

the need for a summing junction at the output to generate the QPSK signal. In effect, the circuit behaves as a QPSK modulator with the following signal constellation shown in Figure 4.2.

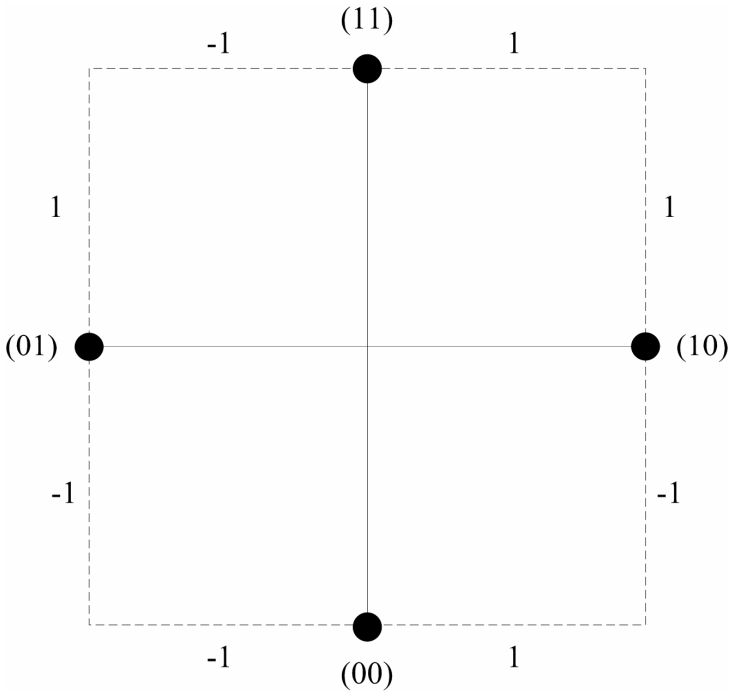

Figure 4.2: QPSK modulator constellation.

4.3 QPSK Modulator Design

In this section, the design of the S-band QPSK modulator in 0.18µm CMOS will be described with detailed analysis of its various components including the balun, the 90° phase shifter and the switch network. In addition, important design considerations will be stressed wherever appropriate.

4.3.1 Balun

The proposed QPSK modulator requires a balun to generate 180° out-of-phase signals from the input carrier as shown in Figure 4.1. The accuracy of this 180° phase split will affect the modulator's performance including its modulation bandwidth. The

same active balun discussed in Chapter 3 [57] which consists of common-gate and common-source FETs (CG-CS) is also used here for the advantages of conversion gain, reduced area and ease of IC integration. Its performance was optimized over the S-band frequency range from 2GHz to 4GHz as appropriate for this modulator design. The circuit schematic of the CG-CS pair is repeated below in Figure 4.3 for convenience.

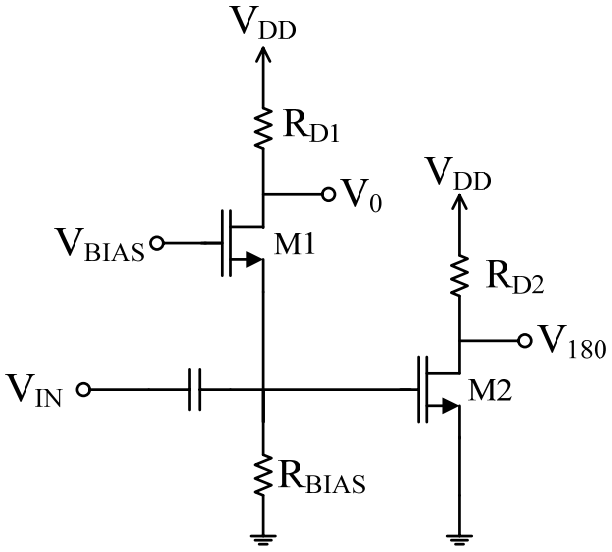

Figure 4.3: Common-gate, common-source (CG-CS) active balun [57].

The common-gate device of the CG-CS active balun is designed with the appropriate width and bias current to yield a low input resistance ($\approx 1/g_m$) close to the 50Ω system impedance. This is achieved over a wide bandwidth without using any bulky matching networks as described in Chapter 3. The biasing source resistance R_{bias} is also chosen large enough not to greatly affect the input impedance or attenuate the signal. Finally, the gains of the common-source and common-gate amplifiers ($\approx g_m R_d$) are matched for the two outputs to have equal amplitudes.

The outputs V_0 and V_{180} of the balun (Figure 4.3) are buffered using FETs in a common-drain (source follower) configuration similar to those described in Chapter 3 (Figure 3.3). This is needed to isolate the outputs from the following 90 º phase shifter,

presenting a larger loading impedance for improved performance including conversion gain. The buffers are also necessary to sufficiently drive the relatively low input impedance of the 90º phase shifter, which is discussed in more detail in the next section.

The balun design was simulated in Cadence software using Taiwan Semiconductor Manufacturing Company (TSMC) 0.18µm RF CMOS BSIM3 device models for the transistors. The full circuit schematic of the balun is shown in Figure 4.4.

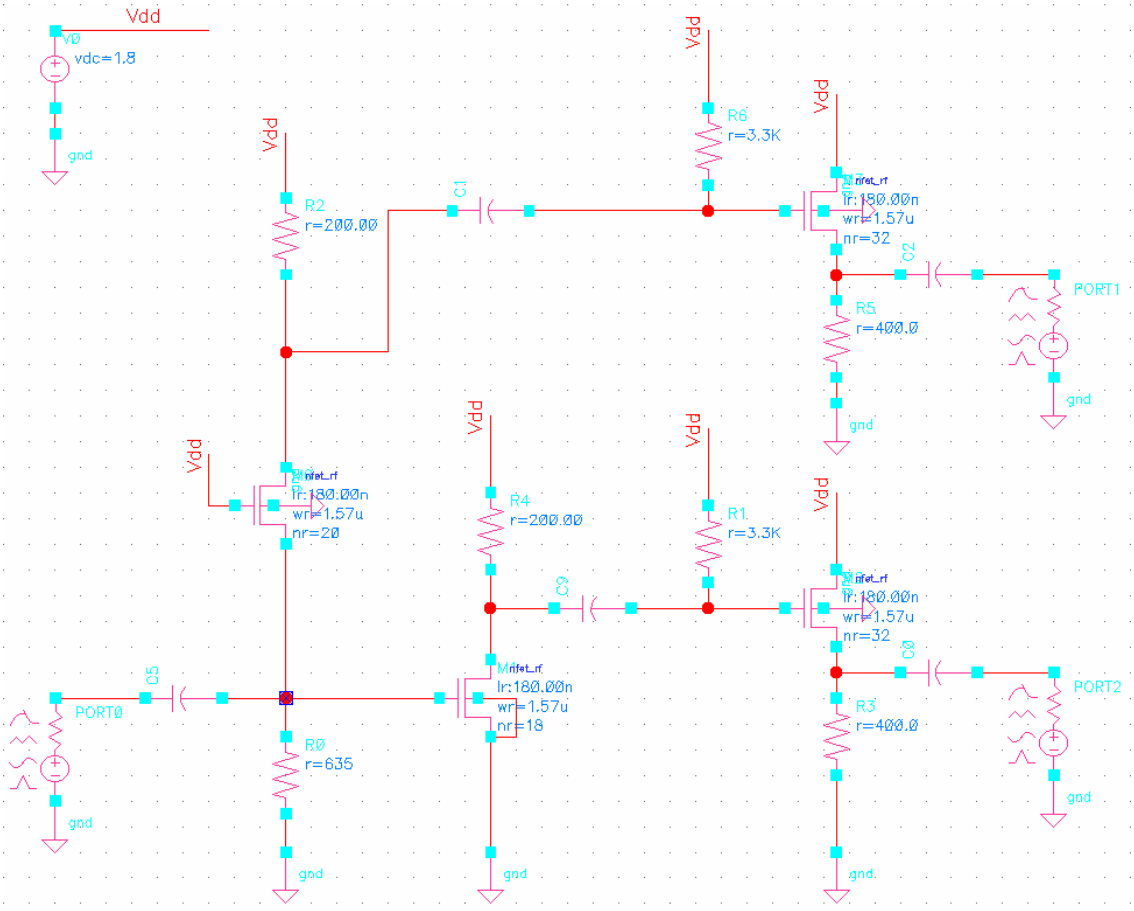

Figure 4.4: Full balun schematic in Cadence.

To verify the circuit's operation, an S-parameter simulation was run over the S-band frequency range from 2GHz to 4GHz with 50Ω ports at the input and outputs as shown in Figure 4.4. The magnitude of the resulting input reflection coefficient S_{11} is plotted in Figure 4.5. It is clear that the coefficient's magnitude is quite low and less than

-11dB over the entire bandwidth. This means that most of the carrier signal power is absorbed by the circuit and not reflected at the input as desired. The transmission coefficient S_{21} from the input to the in-phase output was also computed and its magnitude plotted in Figure 4.6. It is apparent that the transmission coefficient is quite flat with less than ±0.25dB variation across the frequency band and a maximum value of -0.9dB. A signal loss of 0.9dB is actually quite good, at least when compared to a passive balun since an equal two-way power split has a minimum theoretical loss of 3dB. Furthermore, the reflection coefficient S_{22} looking into the circuit from this output is shown in Figure 4.7. Its magnitude is less than -8dB and can be as low as -16dB in this frequency band, indicating that the output resistance of the circuit is sufficiently low (≈50Ω) for the following 90° phase shifter.

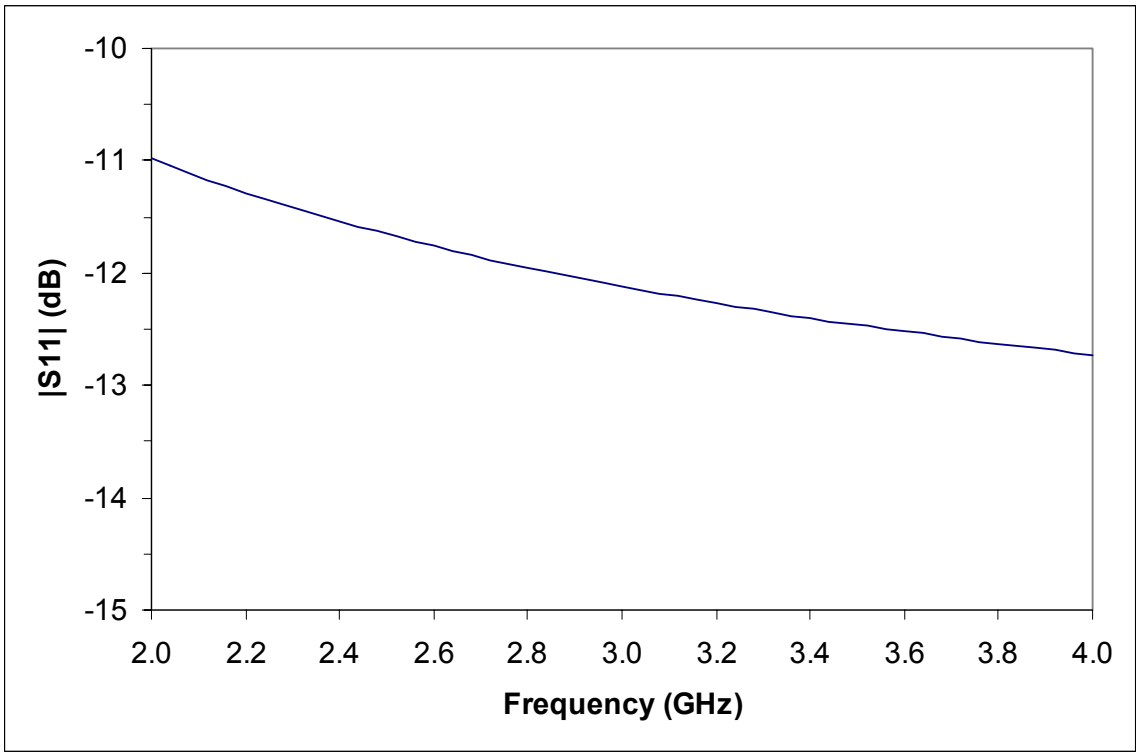

Figure 4.5: Plot of input reflection coefficient (S11) magnitude from 2 to 4GHz.

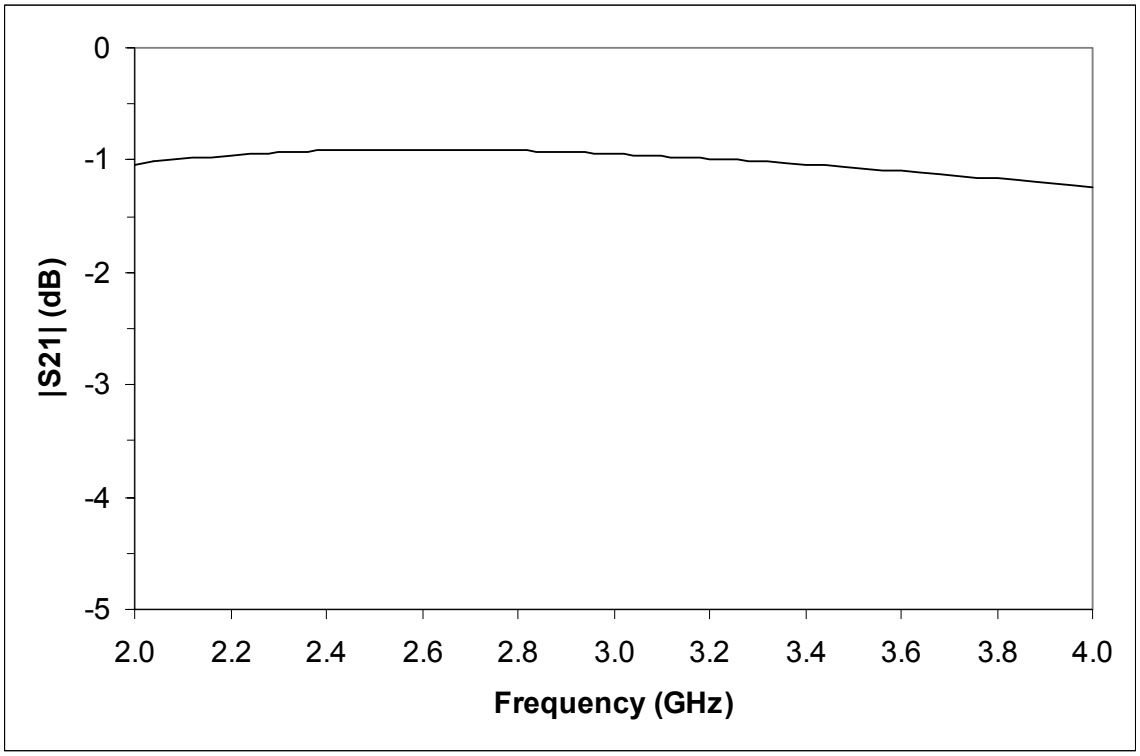

Figure 4.6: Plot of transmission coefficient (S21) magnitude from 2 to 4GHz.

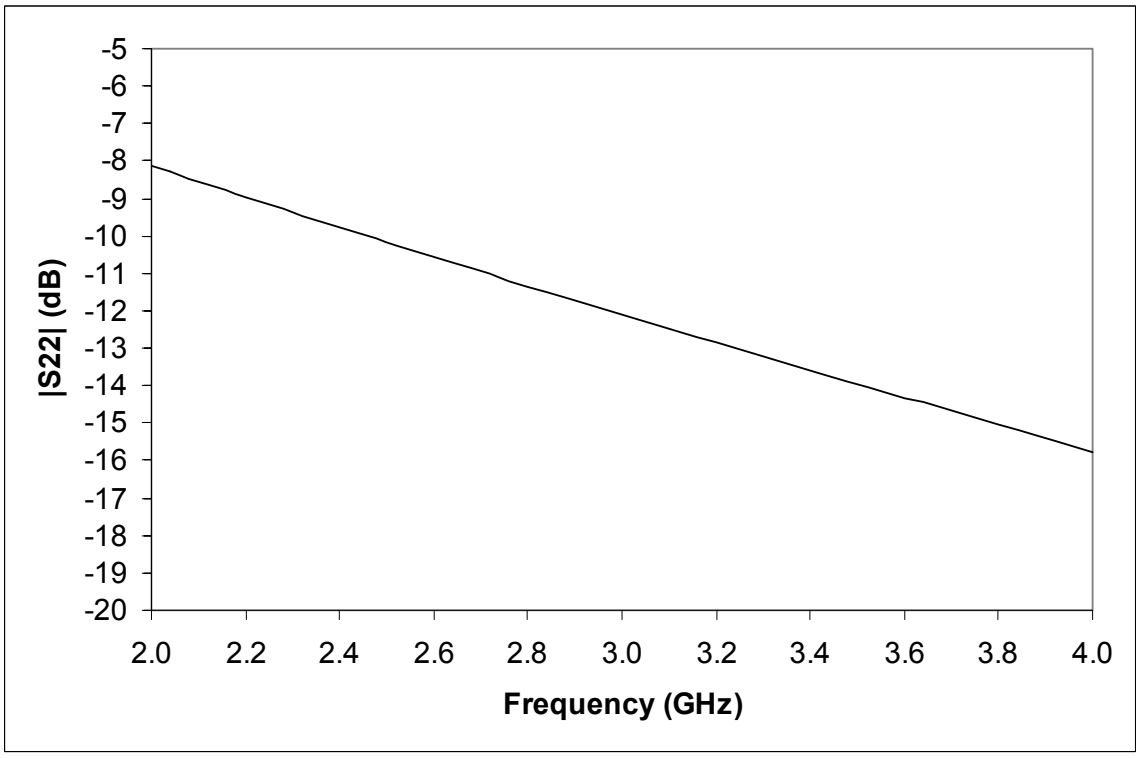

Figure 4.7: Plot of output reflection coefficient (S22) magnitude from 2 to 4GHz.

As the transmission coefficient S_{31} from the input to the antiphase output is also computed in this S-parameter simulation, the phase and amplitude difference between the two balun outputs can be examined. The difference in the phase of the transmission coefficients S_{21} and S_{31} is plotted in Figure 4.8 from 2GHz to 4GHz. As depicted from the plot, the phase difference is quite flat and reaches a maximum of about 180.7° for a very low discrepancy of 0.7° from the desired 180°. The magnitude ratio between these transmission coefficients is also plotted on a similar graph in Figure 4.9, indicating a particularly low amplitude imbalance of 0.075dB over the same frequency band. This verifies and completes the design of the active CG-CS balun for the proposed QPSK modulator.

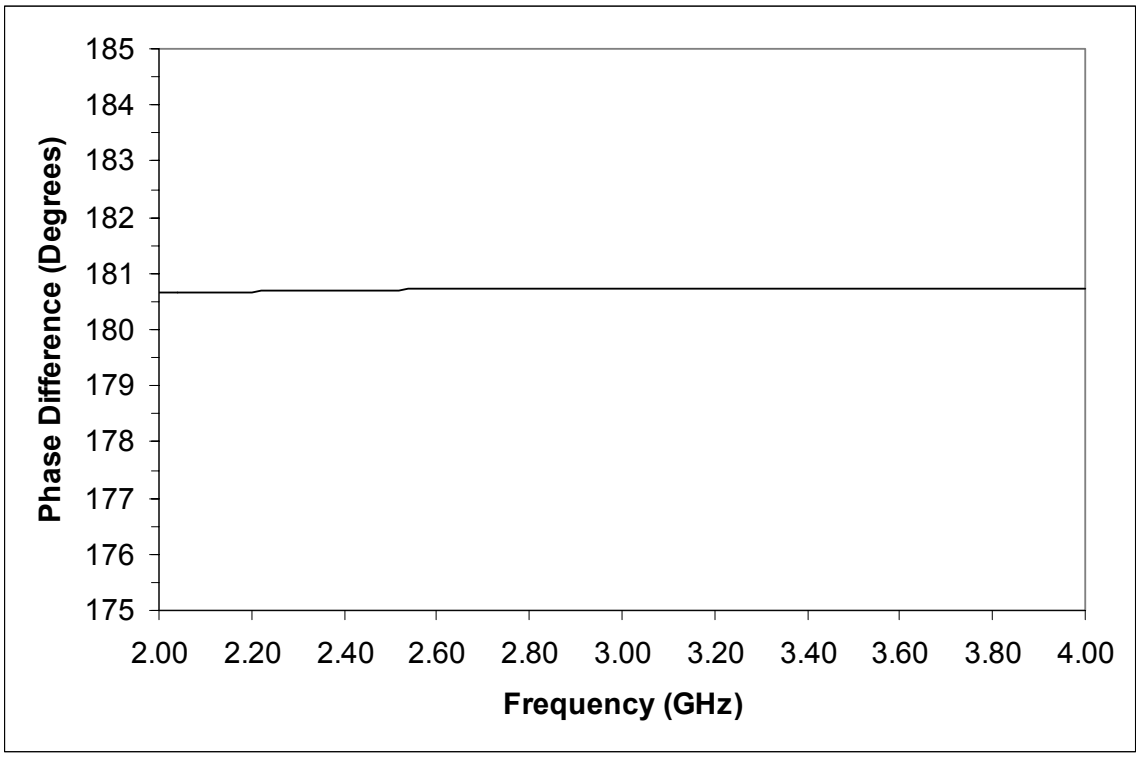

Figure 4.8: Phase difference between balun outputs.

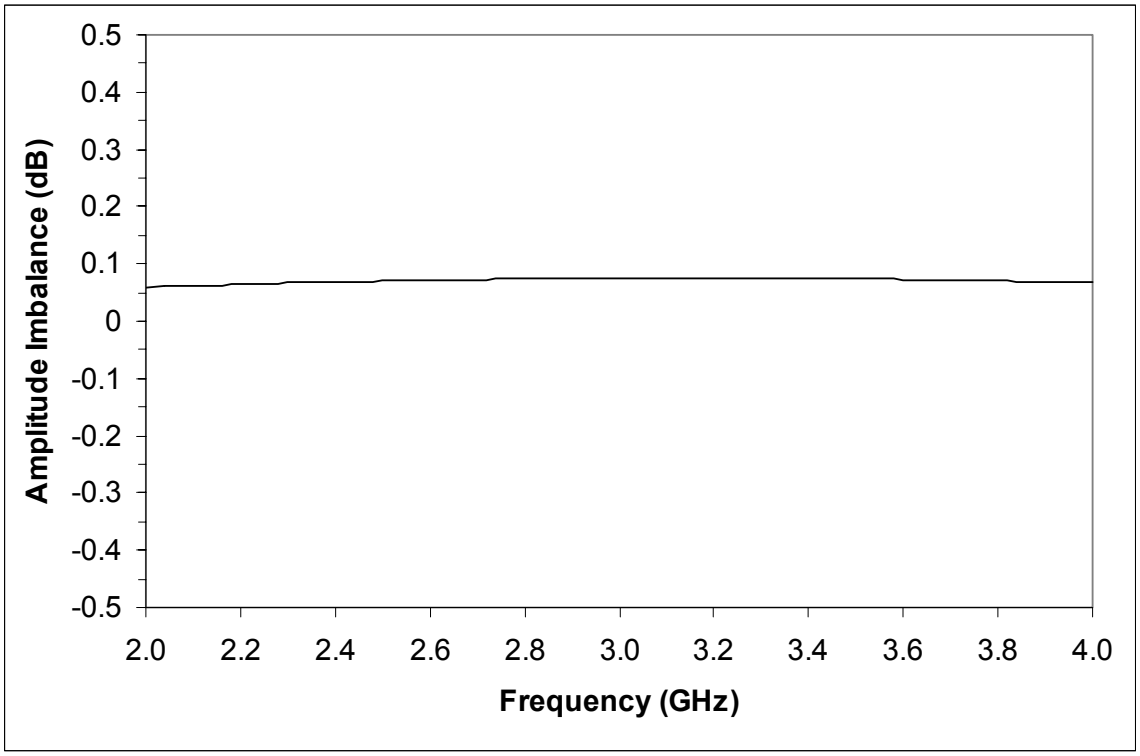

Figure 4.9: Amplitude imbalance between balun outputs.

4.3.2 Quadrature Phase Shifter

The resistor-capacitor (RC) polyphase network is chosen for generating quadrature carriers due to its simple design, small IC footprint and zero DC power consumption. It also offers a lower signal loss compared to using two RC-CR circuits, one for each differential signal. This is because it combines the two balanced signals in a quadrature fashion as opposed to splitting each signal separately. Figure 4.10 below shows the polyphase network and how it generates the differential quadrature phases from the differential input. Each integrating RC branch leads to a -45° phase shift at the cutoff frequency of $1/(RC)$, while each differentiating CR branch leads to a +45° phase shift at the same frequency. A result of this is that the differential inputs are now shifted

±45° towards each other before they are combined at the outputs (with 0dB gain), thus forming differential quadrature signals as illustrated in Figure 4.10.

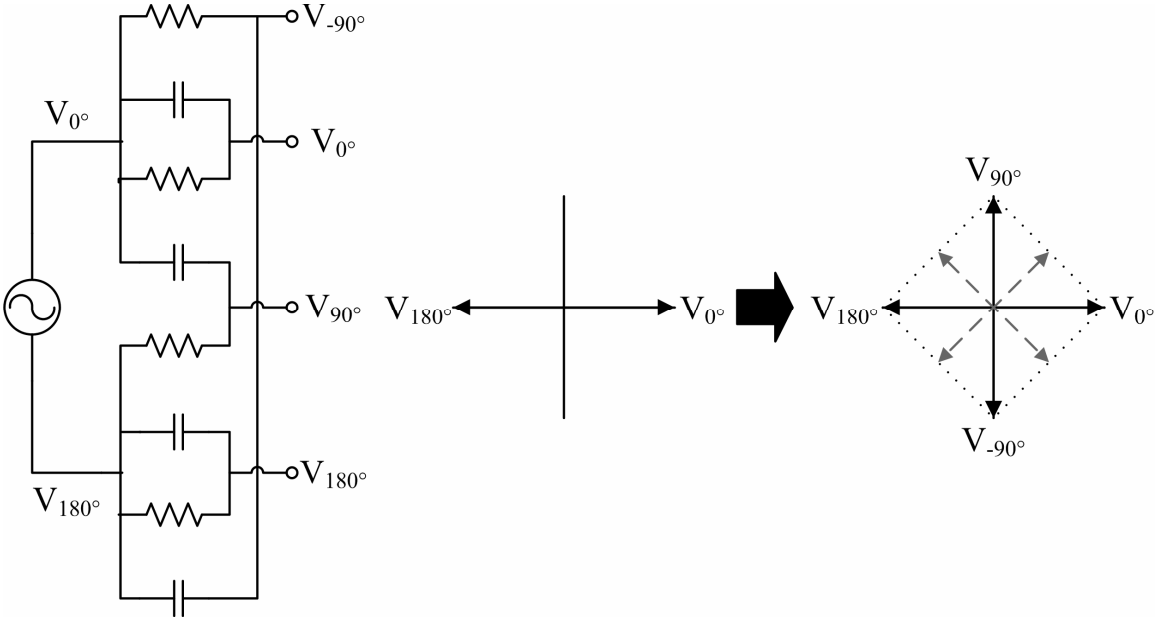

Figure 4.10: RC polyphase network generating differential quadrature phases.

As previously discussed in Chapter 2, the RC polyphase network generally has an all-pass frequency response with the amplitudes matched irrespective of frequency, while the desired 90° phase difference only appears at the cut-off frequency of 1/(*RC*). Therefore at the relatively high carrier frequencies involved, a small RC product is required. This is beneficial as it allows small resistors and capacitors to be used. However integrated polysilicon resistors generally exhibit large tolerances (more than 20%) for small footprints and low resistance values (less than 1kΩ). Such high tolerances are critical since descrepancies will change the network's cutoff frequency, introducing phase errors at the frequency of interest. For this reason, an alternative resistor implementation is preferred in the form of an NMOS transistor biased in the triode region, with the path of interest being between the drain and source of the device and its resistance controlled by a tuning voltage (V_{TUNE}) applied to the gate (Figure 4.11).

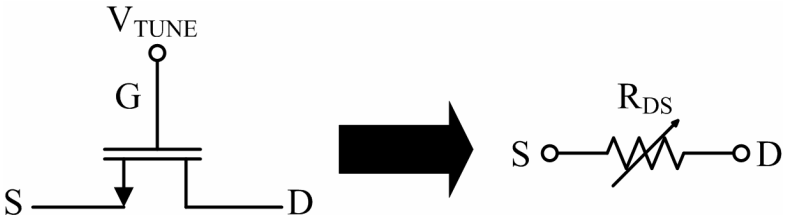

Figure 4.11: NMOS FET resistor operation and model.

A definite advantage of using voltage-controlled resistors is that the RC polyphase network can now be fine-tuned for the lowest possible phase error after process variations. As described in Chapter 3, an NMOS transistor operating in the triode region has a channel induced between its drain and source, with a drain current-voltage (I_{DS}-V_{DS}) characteristic given by:

$$I_{DS} = \frac{\mu_n C_{ox}}{1 + V_{DS}/(LE_{sat})} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}{V_{DS}}^2\right] \tag{4.1}$$

Since the drain-to-source voltage (V_{DS}) is significantly smaller than the gate overdrive voltage ($V_{GS}-V_T$) and the velocity saturation voltage (LE_{sat}), this equation can be approximated as:

$$I_{DS} \approx \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)V_{DS}, \tag{4.2}$$

yielding an equivalent resistance R_{DS}:

$$R_{DS} = \left(\left.\frac{\partial I_{DS}}{\partial V_{DS}}\right|_{v_{gs}=0}\right)^{-1} \approx \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)}, \tag{4.3}$$

where V_{GS} is the applied gate-to-source voltage which is equal to the tuning voltage V_{TUNE} in this case:

$$R_{DS} \approx \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{TUNE} - V_T)}. \tag{4.4}$$

It is now clear that the device behaves as a variable resistor with its resistance (R_{DS}) inversely proportional to the applied tuning voltage (V_{TUNE}) and gate width (W). Therefore a large voltage and/or gate width can be chosen to yield a relatively low resistance value. However at RF frequencies, it is necessary to consider the intrinsic parasitics of the FET (Figure 3.8). Figure 4.12 below shows a high-frequency model of the resistor including the gate-to-source (C_{gs}) and gate-to-drain (C_{gd}) parasitic capacitances, which is very similar to Figure 3.17. From equation (3.13), a larger device width W will increase the parasitic capacitances, reducing their impedance and allowing more of the RF signal to be shorted to AC ground. This leads to a higher signal loss hindering the performance of the RC polyphase network. Therefore the gate width is made narrower while the tuning voltage is increased to keep the same effective resistance. The larger gate overdrive voltage also helps to extend the linearity of the FET and reduce signal distortion as can be seen from (4.1).

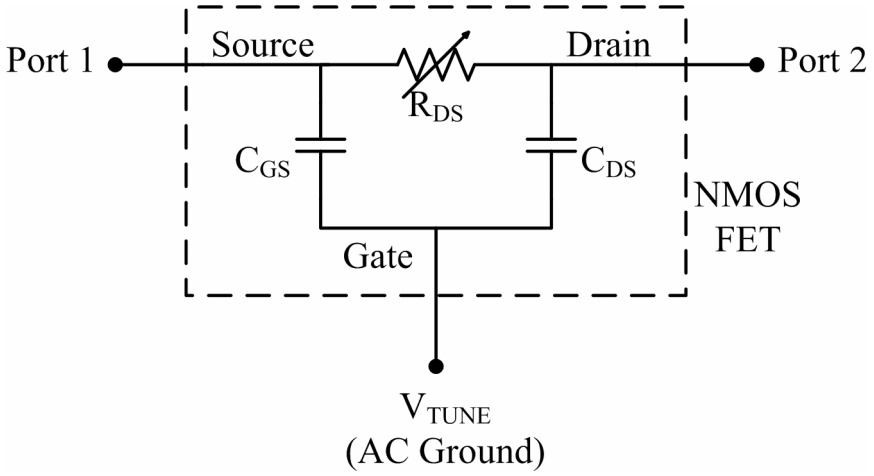

Figure 4.12: Equivalent high-frequency model of FET resistor.

The differential quadrature outputs V_{-90}, V_0, V_{90} and V_{180} of the polyphase filter (Figure 4.10) are amplified using common-source amplifiers illustrated in Figure 4.13.

This is needed to isolate the outputs from the following switch network, presenting a constant loading impedance regardless of the switching state to ensure good quadrature phase and amplitude matching. They are also necessary to reduce the insertion loss through the 90° phase shifter, by providing a relatively large loading impedance and amplifying the signals as well. Large AC coupling capacitors are used to block the DC bias from the input and output, and the biasing resistor R_G is also large enough not to attenuate the input signal significantly.

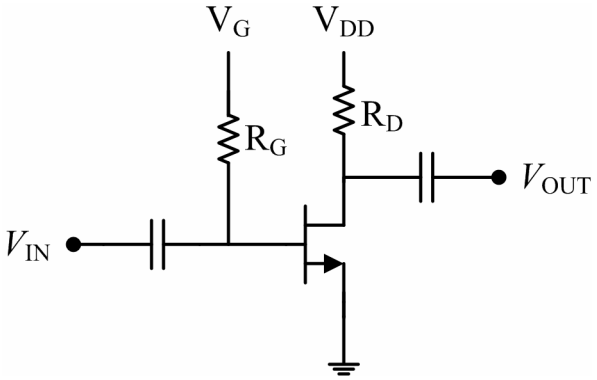

Figure 4.13: Common-source FET as an amplifier.

The 90° phase shifter design was simulated in Cadence software using Taiwan Semiconductor Manufacturing Company (TSMC) 0.18μm RF CMOS BSIM3 device models for the transistors. The full circuit schematic of the phase shifter is shown in Figure 4.14. To verify the circuit's operation, an S-parameter simulation was set up with 50Ω ports at the input and outputs as shown in the figure. An ideal balun was also used to generate the needed balanced signals at the inputs of the polyphase network, as opposed to the active balun designed in the previous section. This allows us to examine the phase and amplitude accuracy of the 90° phase shifter separately to validate its design procedure.

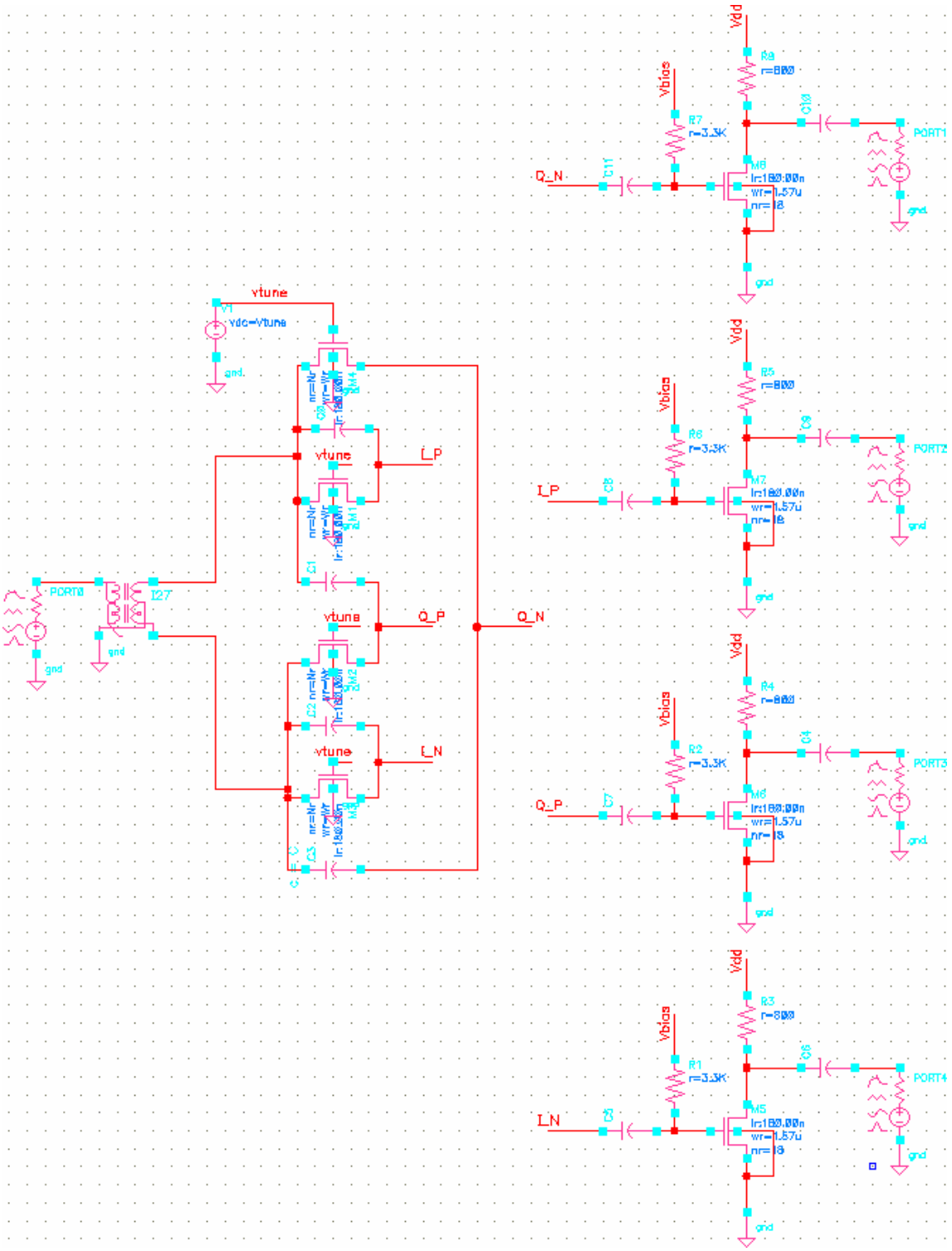

Figure 4.14: Full schematic of quadrature phase shifter in cadence.

The cutoff frequency of the polyphase network ($1/RC$) was chosen to be 2.4GHz for this QPSK modulator. This is an unlicensed frequency band that is widely used for

wireless communication devices including IEEE 802.11a/g WLANs. The capacitance C in the polyphase network was set to a relatively small value of 0.1pF to minimize its IC footprint. With C = 0.1pF, a resistance of R = 660Ω is needed to yield a cutoff frequency of $1/RC = 2\pi\times 2.4\text{GHz}$. An NMOS FET with a narrow gate width of W = 1.5μm is used to implement this resistance with a low parasitic capacitance. For 0.18μm CMOS technology, the device parameters are: $\mu_n = 4.38\times10^{-2}$ m^2/Vs, $C_{ox} = 8.03\times10^{-3}$ F/m, V_T = 0.475V and L = 0.18μm. Therefore the required tuning voltage can be calculated from (4.4) as:

$$V_{TUNE} \approx \frac{1}{\mu_n C_{ox}\frac{W}{L}R} + V_T \tag{4.5}$$
$$= \frac{1}{\left(4.38\times10^{-2}\right)\left(8.03\times10^{-3}\right)\left(\frac{1.5}{0.18}\right)(660)} + 0.475 = 0.99V \approx 1.0V$$

To verify that this combination of gate width W = 1.5μm and tuning voltage V_{TUNE} = 1V will yield the desired effective resistance R = 660Ω, an S-parameter simulation was set up in Cadence as shown below in Figure 4.15. A 50Ω port was placed at the drain and source of the NMOS FET and the simulation was run from 2.3GHz to 2.5GHz. The impedance Z_{in} looking in from port 1 (or port 2) was calculated from the reflection coefficient S_{11} as follows:

$$S_{11} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \Rightarrow Z_{in} = \frac{1+S_{11}}{1-S_{11}}Z_0 . \tag{4.6}$$

The real part of this result $Re\{Z_{in}\}$ is plotted against frequency in Figure 4.16, showing a constant value of about 700Ω. However the impedance Z_{in} looking in from port 1 also includes the 50Ω impedance of port 2 in series. Therefore if 50Ω is subtracted from this

result we arrive at the effective resistance of the FET which is around 650Ω. This is close to the desired resistance value of 660Ω, thus validating our design procedure.

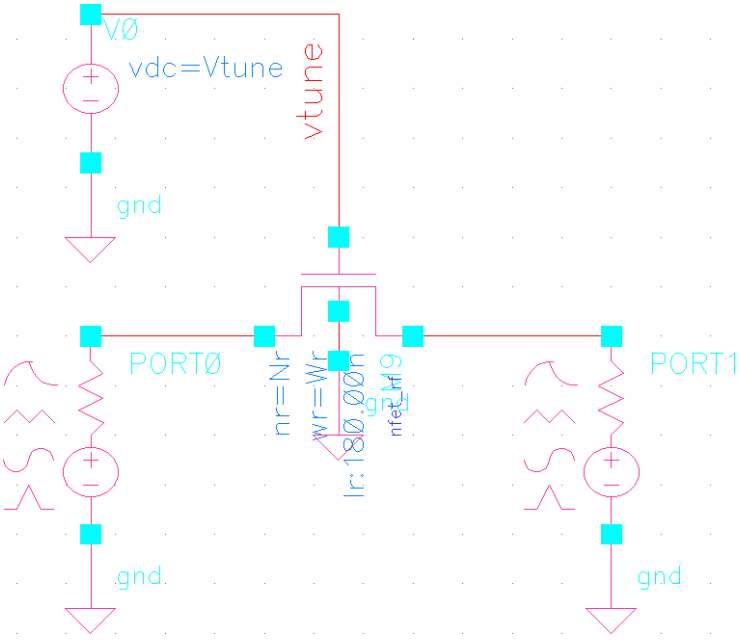

Figure 4.15: S-parameter simulation of NMOS FET resistor in Cadence.

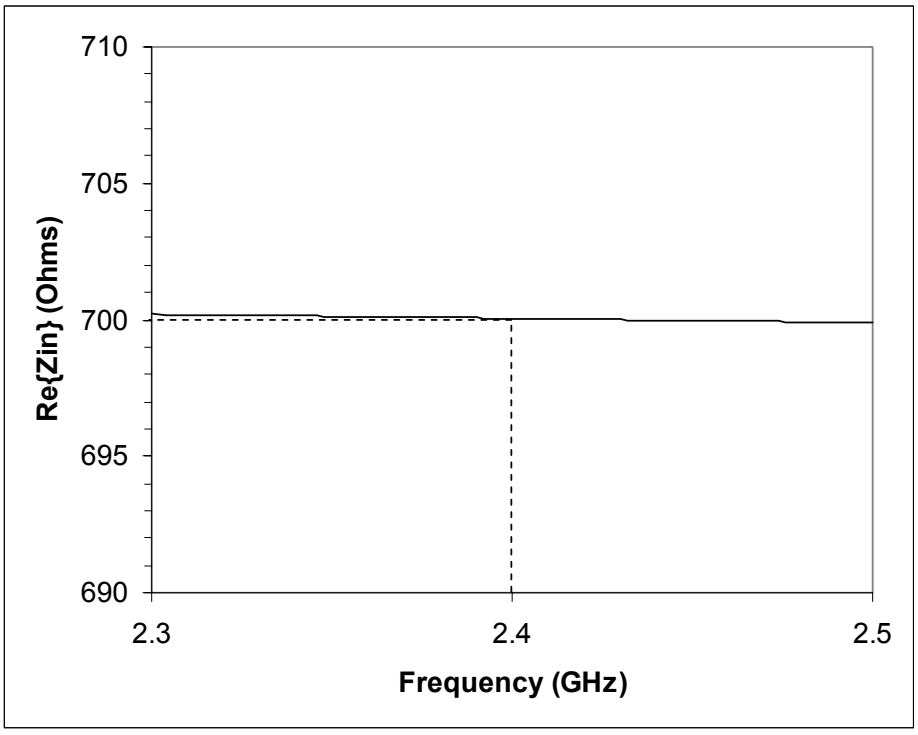

Figure 4.16: Real part of the simulated impedance looking in from port 1.

The above design values for C, W and V_{TUNE} were entered in the schematic and the S-parameter simulation was run over the S-band frequency range from 2GHz to 4GHz. The phase of the resulting transmission coefficients of the polyphase network (S_{21}, S_{31}, S_{41}, and S_{51}) from the input to the outputs is plotted in Figure 4.17 from 2GHz to 4GHz. As indicated on the plot at 2.4GHz, the phase differences between the outputs are very close to the desired 90°, 180° and 270° (-90°), with a maximum phase error of only 0.08°. The magnitudes of these transmission coefficients are also plotted on a similar graph in Figure 4.18, indicating a particularly low amplitude imbalance of 0.071dB at the same frequency. This verifies the design procedure of the 90° phase shifter for the proposed QPSK modulator.

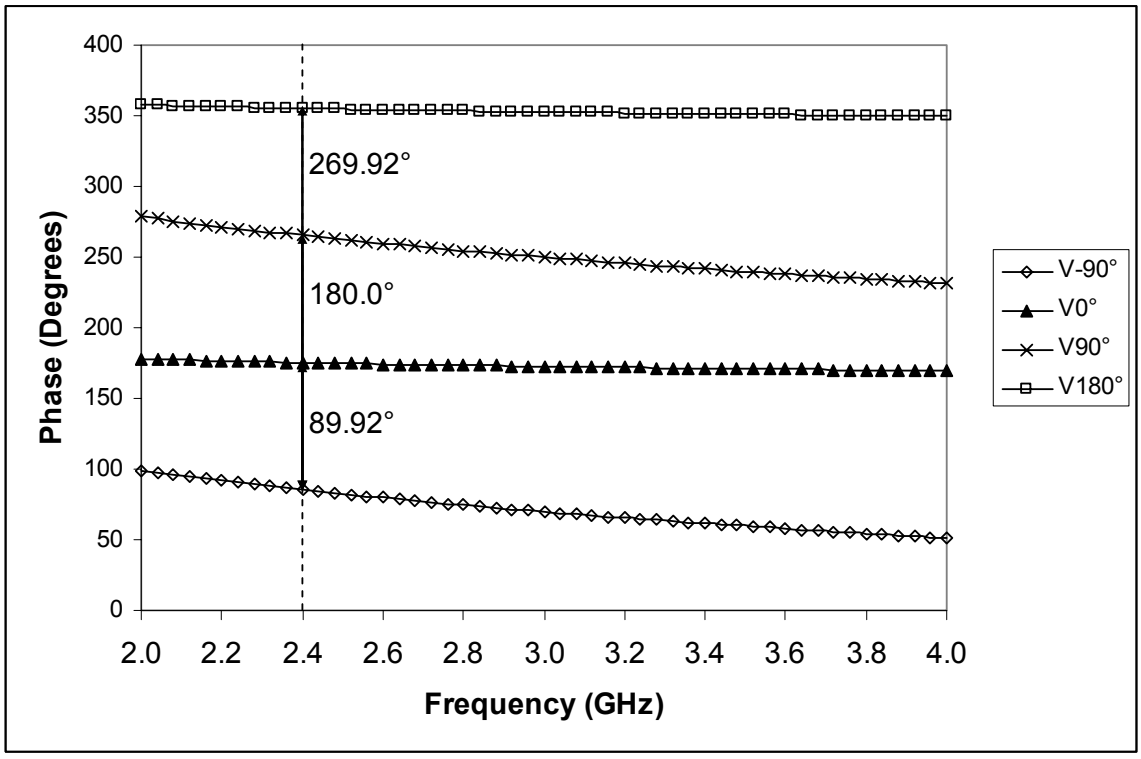

Figure 4.17: Plot of transmission coefficient phase for phase imbalance at 2.4GHz.

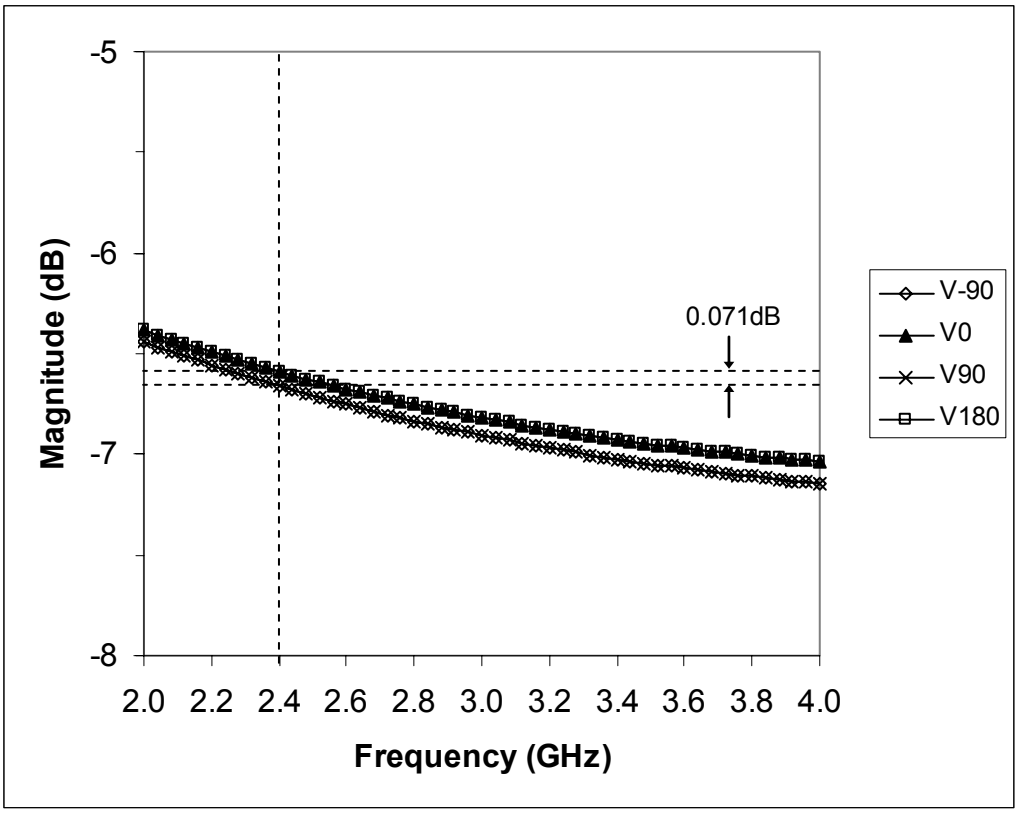

Figure 4.18: Plot of transmission coefficient magnitude for amplitude imbalance

The magnitude plot in Figure 4.18 seems to indicate that the signal loss through the 90° phase shifter is around 6.6dB. However this loss is only valid when the outputs are loaded with 50Ω ports. In the context of the overall QPSK modulator, this circuit will actually be followed by a switch network and then by an output buffer, which provides a much higher loading impedance and enables the common-source FETs to amplify the signals. Therefore the overall signal loss will be lower than Figure 4.16 suggests, as discussed in section 4.3.4.

4.3.3 Switch Network

The purpose of the switch network is to pass one signal from the four differential quadrature signals (V_{-90}, V_0, V_{90} and V_{180}) while blocking the other three, according to both *I* and *Q* data values which constitute the QPSK symbol. In particular, the following

digital logic should be realized by the switch network in order to yield the desired QPSK signal constellation (Figure 4.2) at the output:

$$V_{QPSK} = \bar{I}\bar{Q}(V_{-90^\circ}) + I\bar{Q}(V_{0^\circ}) + IQ(V_{90^\circ}) + \bar{I}Q(V_{180^\circ}), \tag{4.7}$$

which can be simplified to:

$$V_{QPSK} = \bar{Q}\left(\bar{I}(V_{-90^\circ}) + I(V_{0^\circ})\right) + Q\left(I(V_{90^\circ}) + \bar{I}(V_{180^\circ})\right). \tag{4.8}$$

This is realized in Figure 4.1 as a set of six complimentary switches in two stages, the first four being for the I data stream and the remaining two for the Q data stream.

A Pass-Transistor Logic (PTL) circuit consisting of six NMOS switches as shown in Figure 4.19 is used to implement the needed switch network in Figure 4.1, which has the advantages of small footprint, zero DC power consumption and high-speed operation. An NMOS FET can be naturally used as a switch, with the characteristic models in Figures 3.16, 3.17 and the design equations (3.10)-(3.13) discussed in Chapter 3. While increasing the FET width W will reduce its on-resistance R_{DS} given by (3.12) and thus the signal loss across it, it will also increase its gate-to-source (C_{gs}) and gate-to-drain (C_{gd}) parasitic capacitances as in (3.13). This leads to more capacitive coupling between the *I* and *Q* digital data signals and the QPSK signal, adversely affecting the performance of the QPSK modulator. Therefore a narrow gate width of W = 1.5μm was chosen for this design to minimize this effect, especially at higher data rates where it is more pronounced. To maintain circuit symmetry between the *I* and *Q* data inputs and present the same loading impedance (i.e. gate parasitic capacitance) to both, transistors M5 and M6 are made twice as wide as transistors M1-M4 with W = 3μm.

The QPSK signal output V_{QPSK} of the switch network (Figure 4.19) is buffered using a FET in a common-drain (source follower) configuration similar to the one described in Chapter 3 (Figure 3.3). This is needed to present a large loading impedance for the switch network and the preceding common-source amplifiers to reduce the insertion loss. The buffer is also designed to drive the external 50Ω load with a low reflection coefficient by ensuring an adequate output impedance match in the buffer given by:

$$Z_{OUT} = \frac{1}{g_m} \Big\| R_s \approx 50\Omega, \tag{4.8}$$

where g_m is the transconductance of the FET and R_s is the source resistance. This can be achieved over a wide bandwidth as opposed to using a narrowband passive network which could also be prohibitively large in this frequency range (2.4GHz).

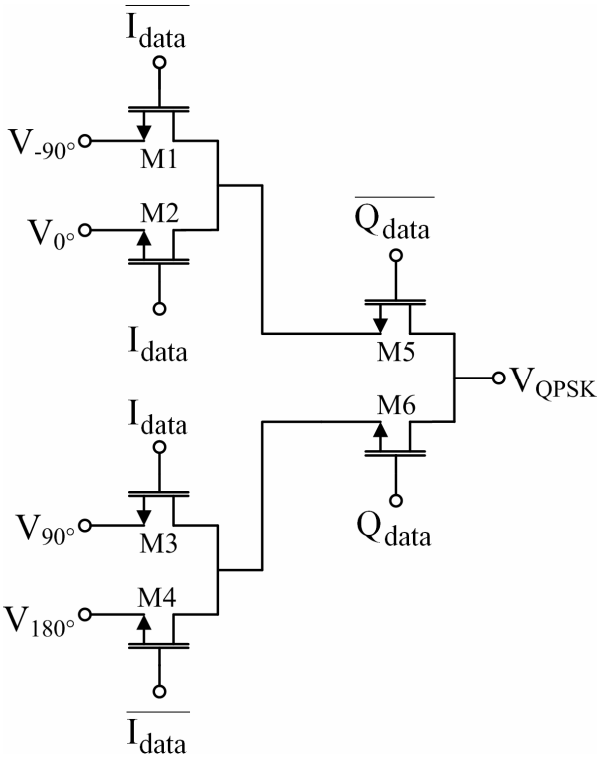

Figure 4.19: Circuit Schematic of Switch Network for QPSK Modulator

4.3.4 QPSK Modulator Simulation

The complete QPSK modulator design was simulated in Cadence software using Taiwan Semiconductor Manufacturing Company (TSMC) 0.18μm RF CMOS BSIM3 device models for the transistors. The full circuit schematic of the QPSK modulator is shown in Figure 4.20.

To assess the signal constellation of the QPSK modulator, an S-parameter simulation was set up in Cadence with 50Ω ports at the carrier input and the QPSK output, in addition to DC voltage sources for the I and Q data inputs. The simulation was then run over the S-band frequency range from 2GHz to 4GHz. The voltage values for the DC sources were also swept from 0V to 1.8V in a parametric analysis to include all four possible combinations of the I and Q data values (00, 01, 11, 10), with 0V denoting logic 0 and 1.8V denoting logic 1. This in effect simulates all four points in the desired signal constellation (Figure 4.2) one at a time. The phase of the resulting transmission coefficient (S_{21}) from the input to the output in each of these four cases is plotted in Figure 4.21. As indicated on the plot at 2.4GHz, the phase differences between the outputs are very close to the desired 90°, 180° and 270° (-90°), with a maximum phase error of only 0.26°. The magnitude of this transmission coefficient is plotted on a similar graph in Figure 4.22, indicating a particularly low amplitude imbalance of 0.079dB at the same frequency. Also it is clear that the signal exhibits a maximum loss of about 3.3dB, which is not excessive if we consider the fact that the minimum theoretical loss through an equal 4-way power split is 6dB as discussed in Chapter 3. In conclusion, the low phase and amplitude errors show that the generated signal constellation is close to the ideal QPSK one (Figure 4.2), thus verifying the design of our modulator.

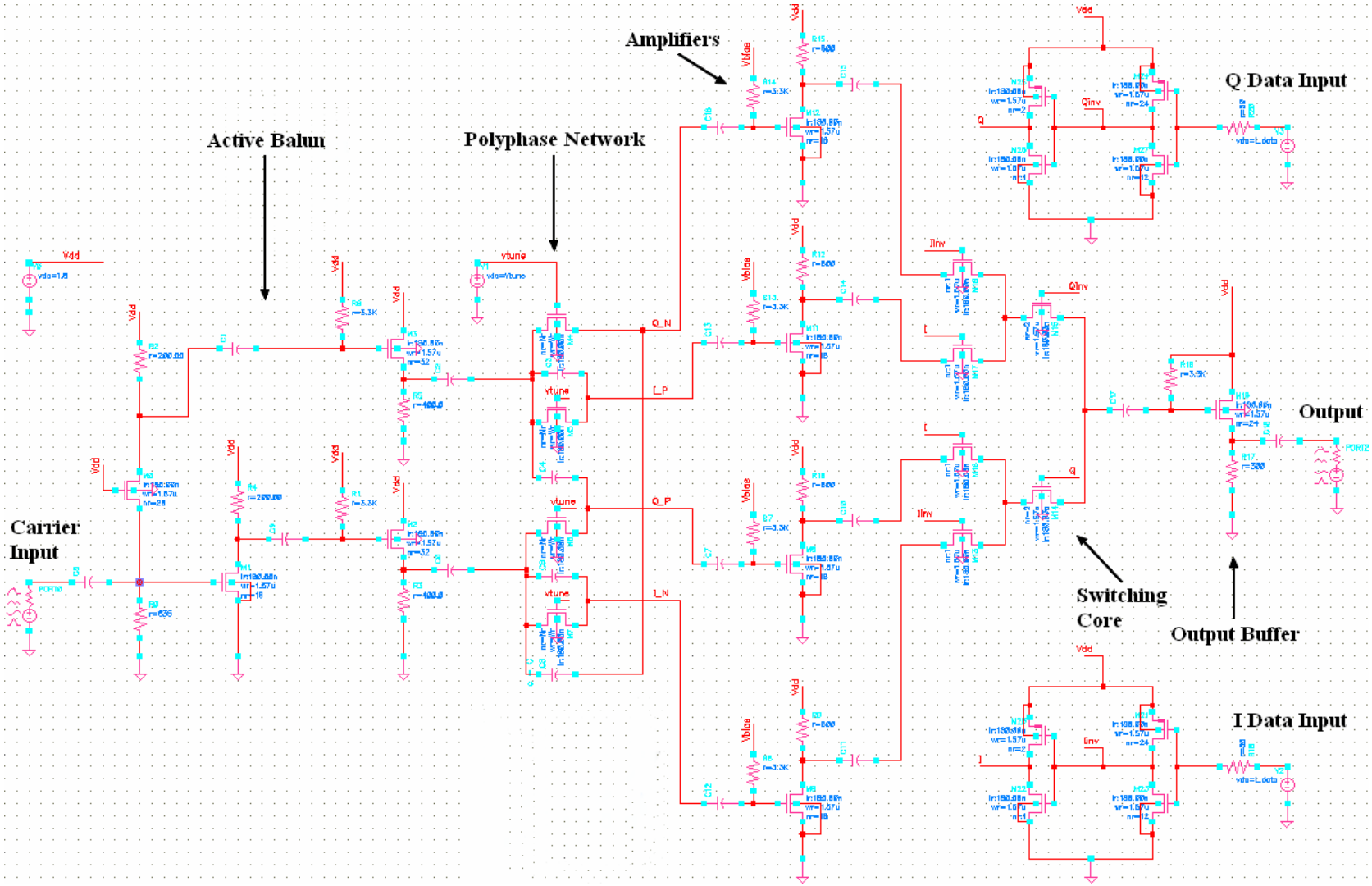

Figure 4.20: Full QPSK modulator circuit schematic in Cadence.

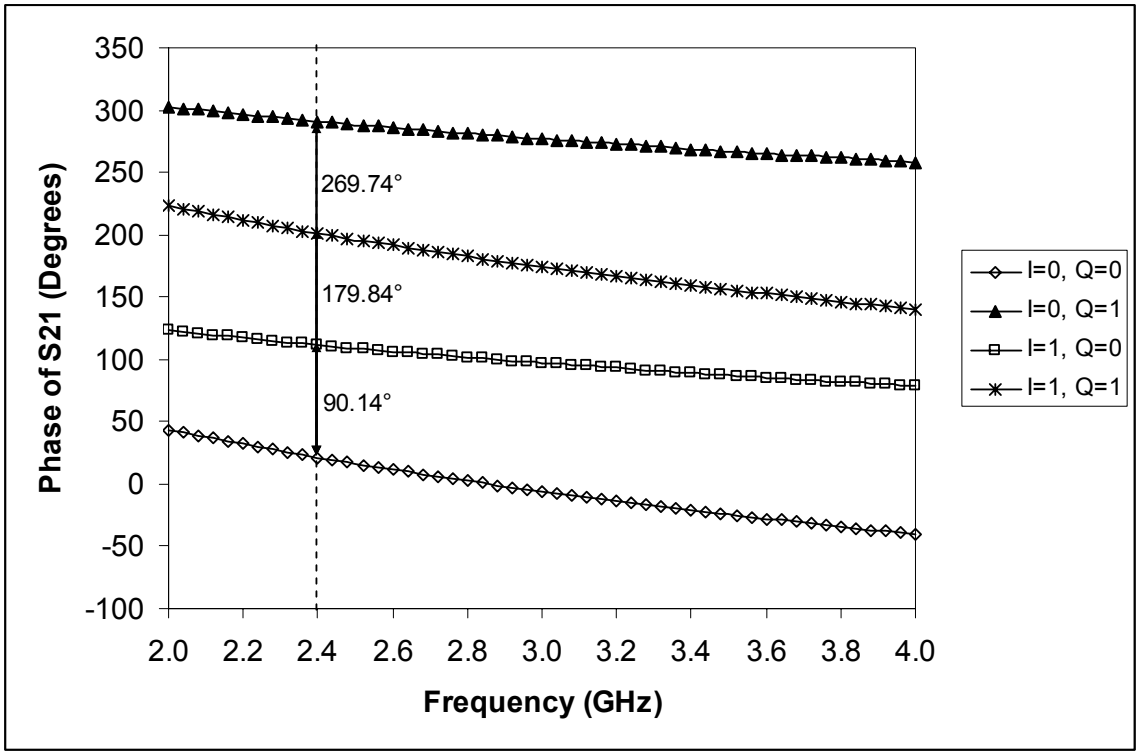

Figure 4.21: Transmission coefficient S21 phase for all four I and Q combinations.

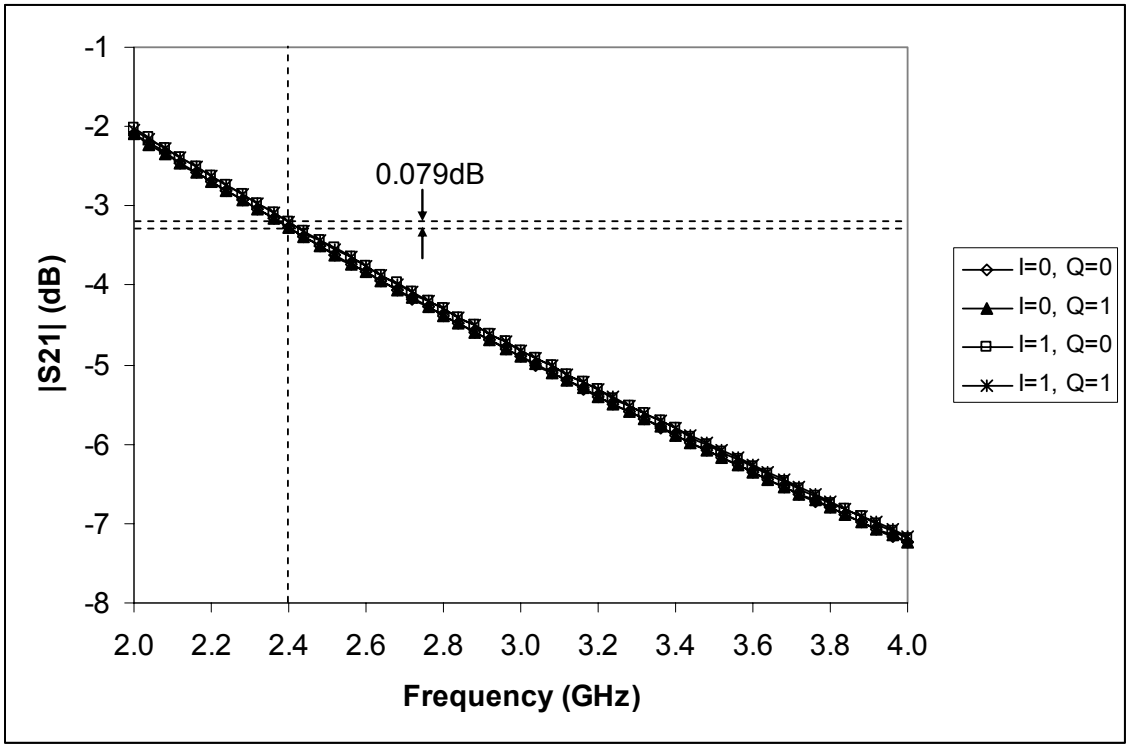

Figure 4.22: Transmission coefficient S21 magnitude for all I and Q combinations.

The input (S_{11}) and output (S_{22}) reflection coefficients were also computed as part of these simulations and their magnitudes plotted separately in Figures 4.23 and 4.24. It is clear that the reflection coefficients are quite low, with magnitudes lower than -11dB over the entire bandwidth. Furthermore, the same reflection coefficient is observed for all combinations of I and Q, indicating that the switches are sufficiently isolated from the input and output ports.

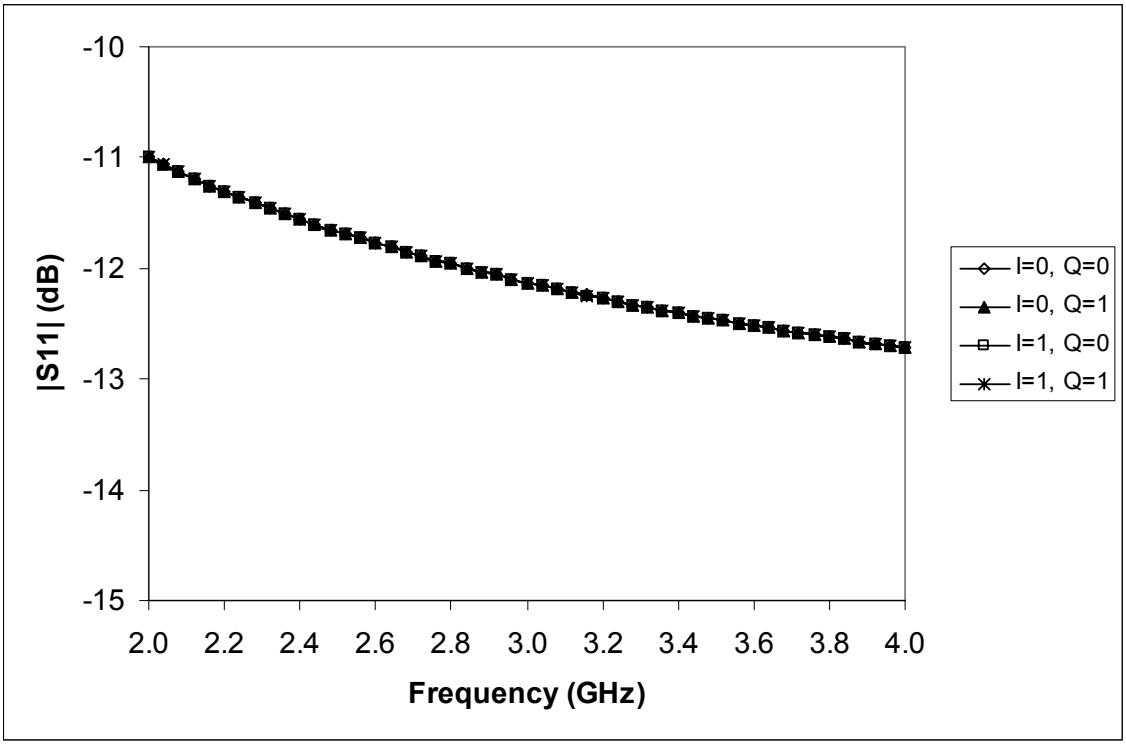

Figure 4.23: Input reflection coefficient S11 magnitude for all combinations.

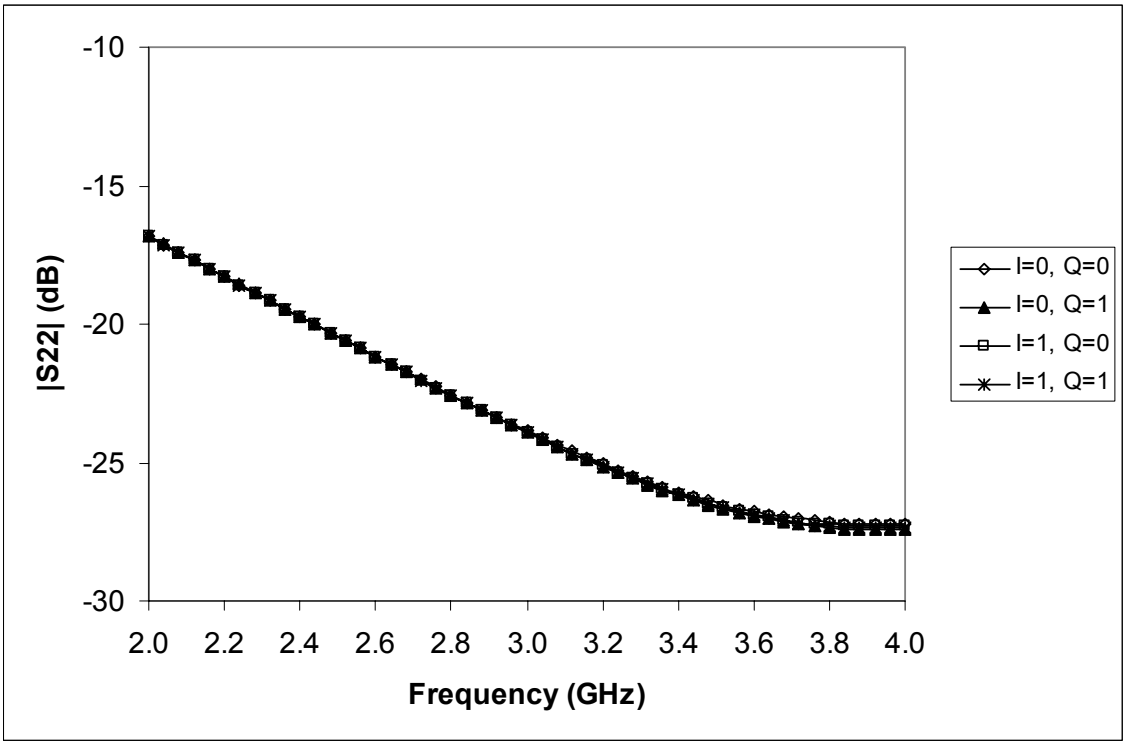

Figure 4.24: Output reflection coefficient S22 magnitude for all combinations.

In order to have more confidence in the circuit's performance after fabrication, simulations were performed on the layout of the modulator IC in Cadence Virtuoso, which is shown in Figure 4.25. The layout was first extracted with the parasitic capacitance between the various metal traces and other process layers included in it. Then a test bench (Figure 4.26) was set up to run the simulations on this extracted layout. The same S-parameter simulation was run to assess the signal constellation, loss and reflection coefficients. The phase of the resulting transmission coefficient (S_{21}) from the input to the output for each of the four QPSK symbol values is plotted in Figure 4.27. As indicated on the plot at 2.4GHz, the phase differences between the outputs remain very close to the desired 90°, 180° and 270° (-90°), with a maximum phase error of only 0.53°. The magnitude of this transmission coefficient is plotted on a similar graph in Figure 4.28, also indicating a low amplitude imbalance of 0.23dB at the same frequency. In

addition, it is clear that the signal now exhibits a maximum loss of 6.2dB, which is again not excessive. The input (S_{11}) and output (S_{22}) reflection coefficients are also plotted separately in Figures 4.29 and 4.30. It is clear that the reflection coefficients are still quite low, with magnitudes lower than -10dB over the entire bandwidth. These simulations provide a good indication on how the fabricated IC will perform when tested.

To simulate the modulator's carrier rejection, a time-domain simulation was run with a 2.4GHz, -20dBm sinusoidal signal source for the carrier, and a square wave source for each of the *I* and *Q* digital signals. The same square wave parameters were set for both I and Q sources, with an amplitude level of 1.8V (V_{dd}) in the high state and 0V (ground) in the low state. The frequency of the square wave f_{MOD} was also chosen to be 50MHz (time period $T = 1/f_{MOD} = 20$ns) for a 100Mbps data rate. It is important to note that the relatively high frequency of 50MHz was necessary because of the speed and memory constraints of the computer system. The difficulty arises from the widely different frequencies of the carrier and digital modulation signals, which was discussed in detail in Chapter 3. The generated time-domain plot for the modulator's output voltage is shown in Figure 4.31 using an eye diagram to focus on the 180º phase traversals of the carrier signal. It can be seen that the zero crossings of the two signals roughly coincide at the same point in time, indicating a phase shift very close to 180º. The frequency spectrum of this modulated signal over 20 periods (400ns) is also illustrated in Figure 4.32. The spectrum matches the theoretical one discussed in Chapter 3, with a high degree of symmetry around the centre frequency and well-defined nulls at even-order harmonics. As depicted from the plot, the carrier at 2.4GHz is also well suppressed by more than 32dB relative to the main spectral lines at 2.4GHz ± 50MHz.

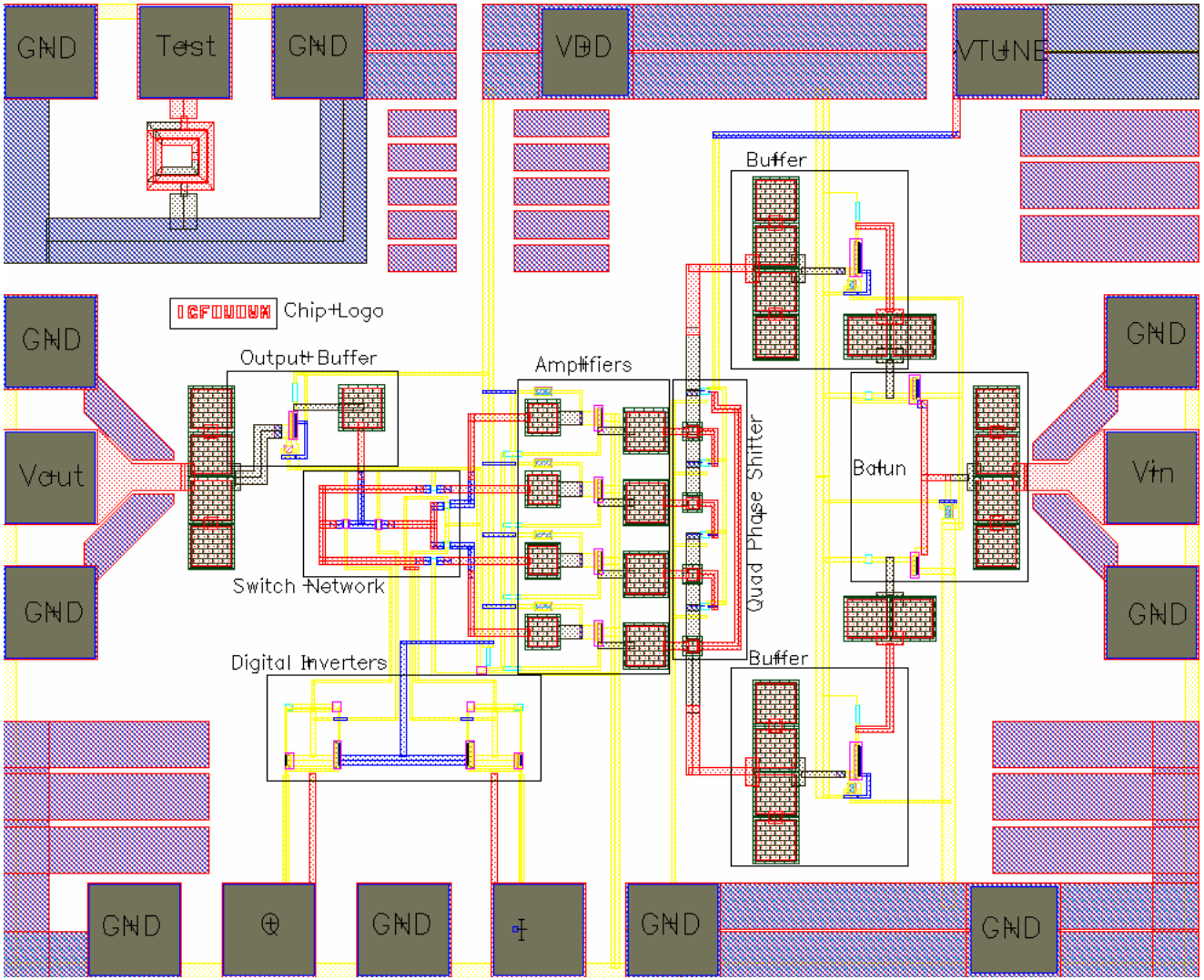

Figure 4.25: QPSK modulator IC layout in Cadence.

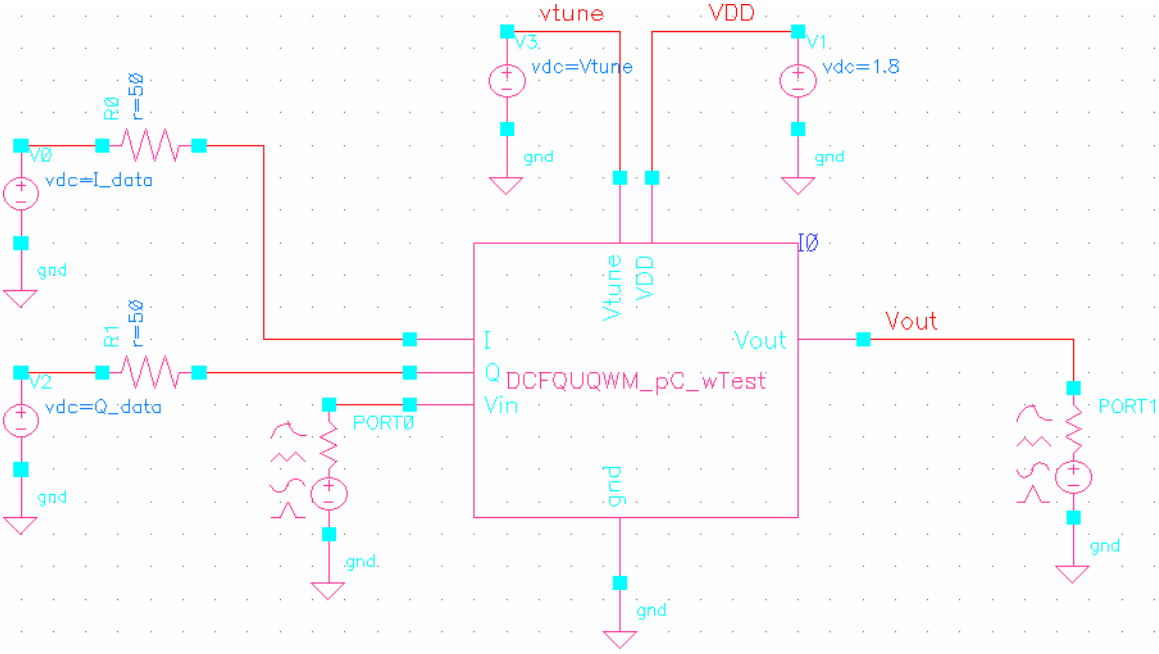

Figure 4.26: QPSK modulator extracted layout test bench.

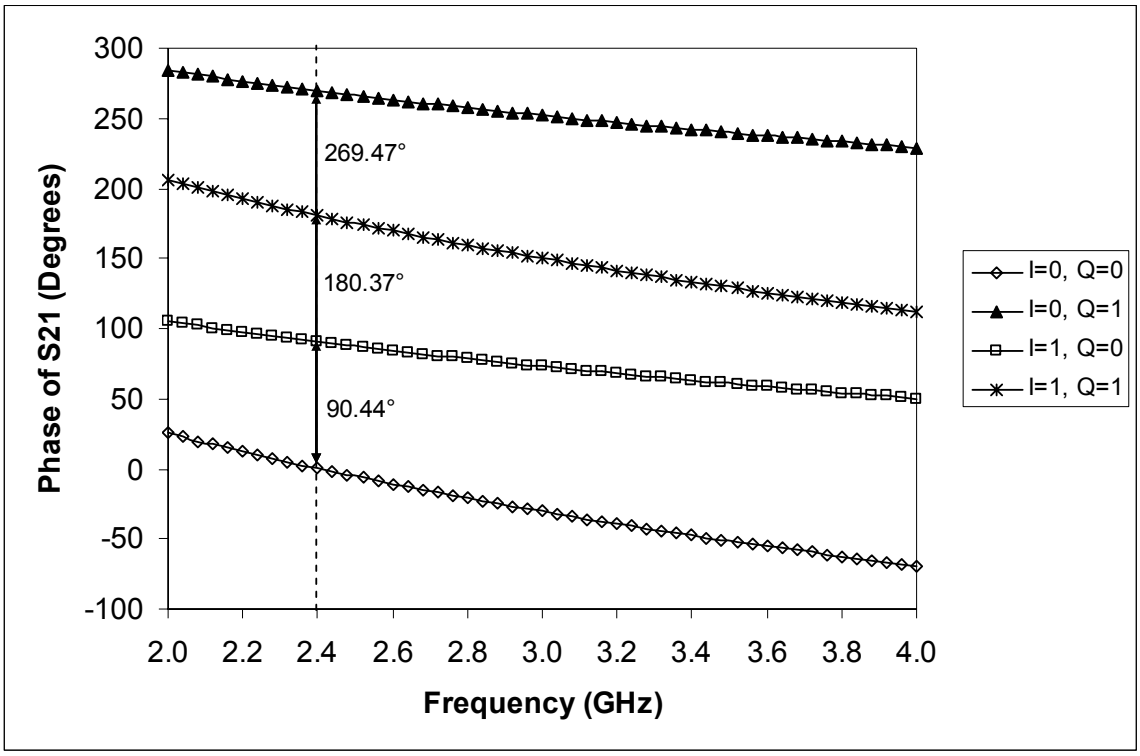

Figure 4.27: Phase balance for modulator IC layout with parasitic capacitance.

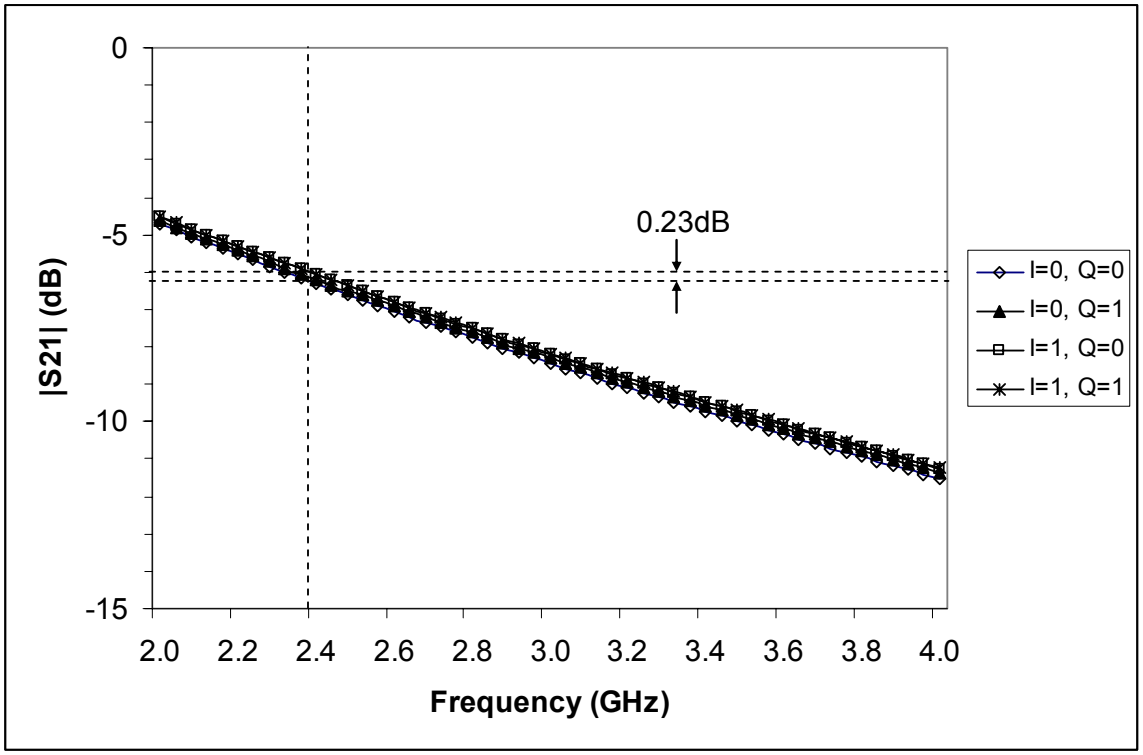

Figure 4.28: Amplitude balance for IC layout with parasitic capacitances.

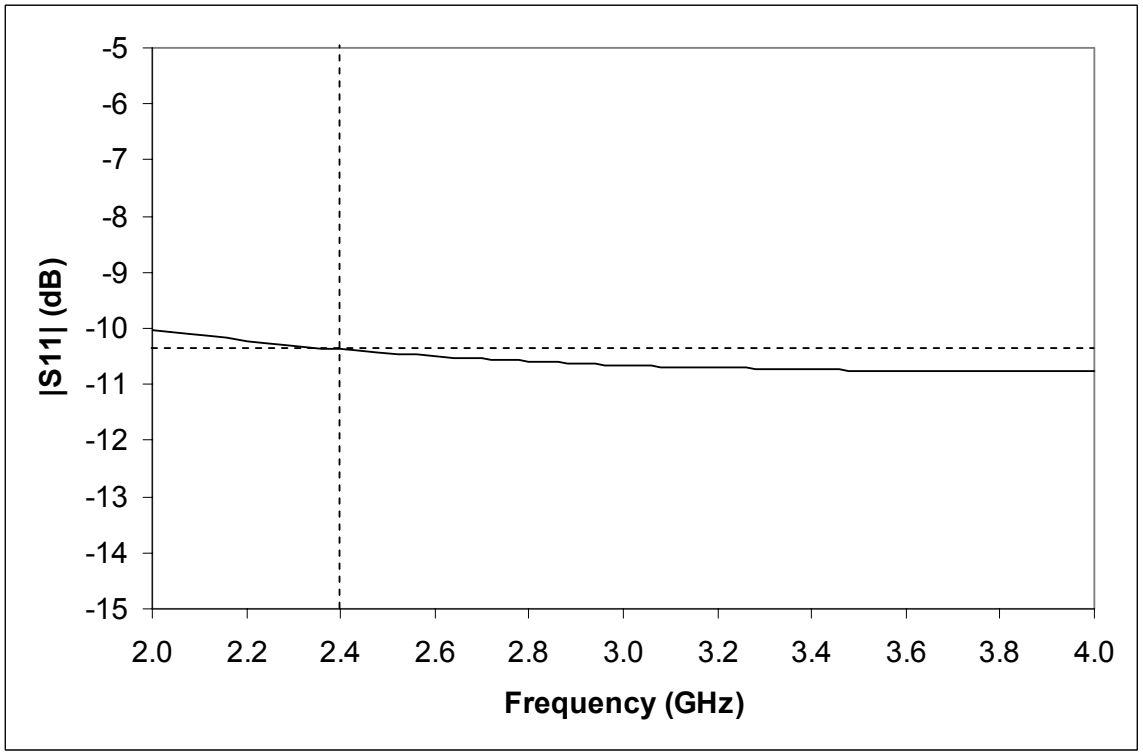

Figure 4.29: Input reflection coefficient S11 magnitude for modulator IC layout.

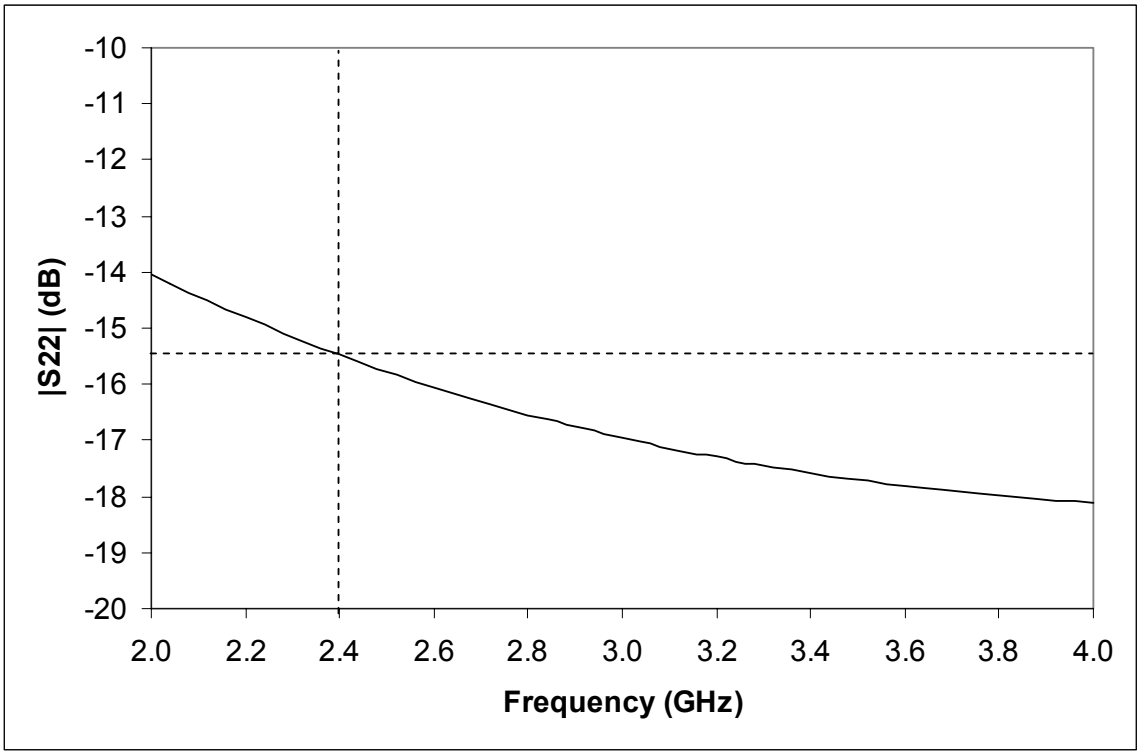

Figure 4.30: Output reflection coefficient S22 magnitude for modulator IC layout.

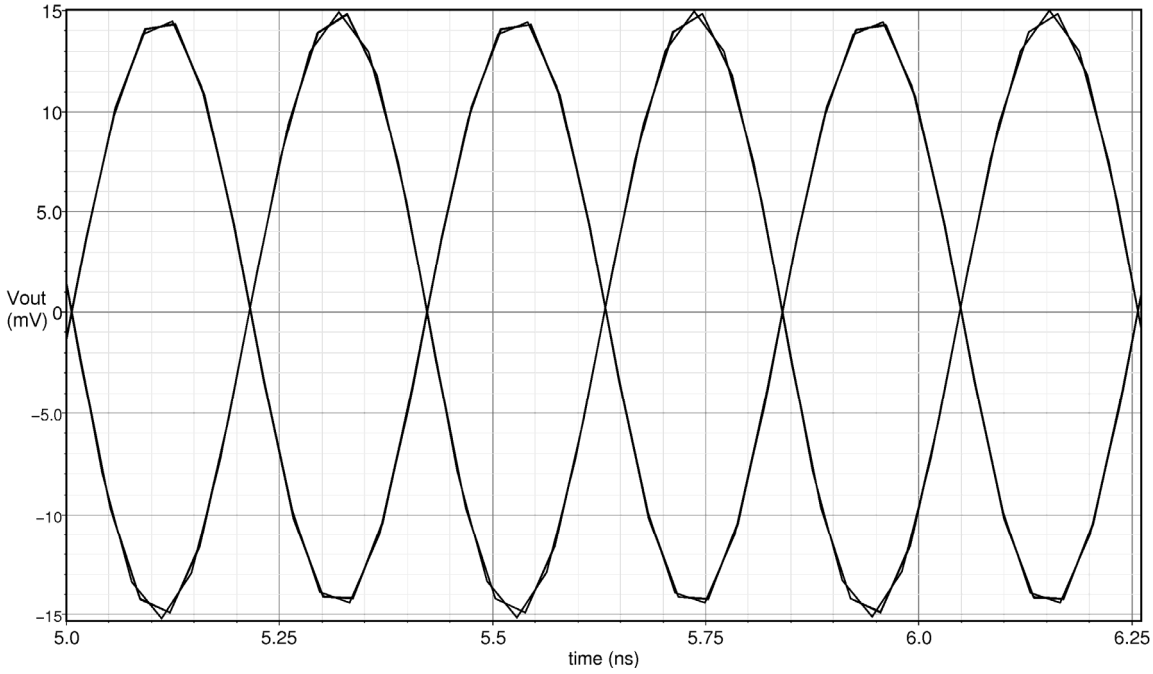

Figure 4.31: Time-domain eye diagram of modulator output.

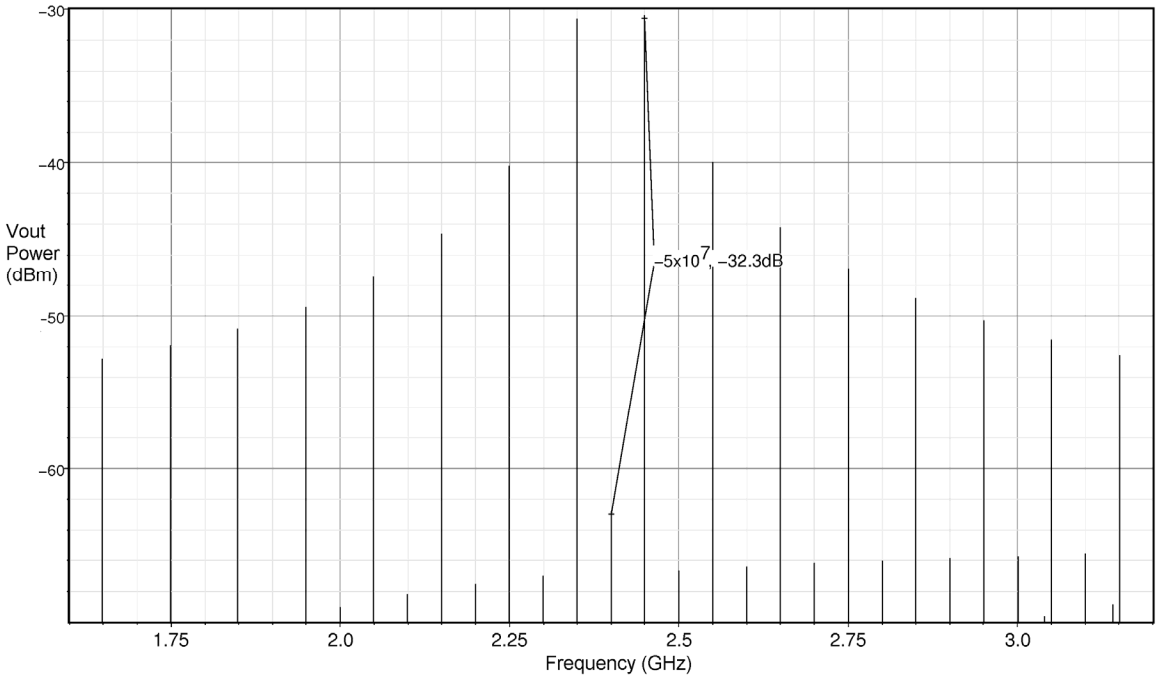

Figure 4.32: Carrier rejection frequency spectrum for modulator output.

4.4 QPSK Modulator Test and Measurement

The QPSK modulator was fabricated in a standard (six-metal, single-poly) 0.18μm CMOS process. A photograph of the IC is shown in Figure 4.33. It occupies a total die area of about 0.720 × 0.888 mm including test structures and bonding pads, but the active circuit area is only 0.505 × 0.610 mm. The circuit consumes less than 19mA of current from a 1.8V voltage supply, i.e. 34mW of power.

To test the QPSK modulator IC, a direct on-wafer measurement was carried out using Cascade Microtech coplanar waveguide (CPW) probes and DC probes on a Wentworth probe station. An Anritsu signal generator (model MG3694A) and Agilent pulse data generator (model 81130A) were used to apply the input carrier signal and digital data signals respectively. To examine the output signal spectrum, the Agilent E4446A spectrum analyzer was used. Finally, a vector network analyzer (Agilent

8510C) was employed for all S-parameter measurements including QPSK signal constellations and reflection coefficients. Prior to the VNA measurements, a full two-port SOLT calibration was performed using a SUSS MicroTec calibration substrate.

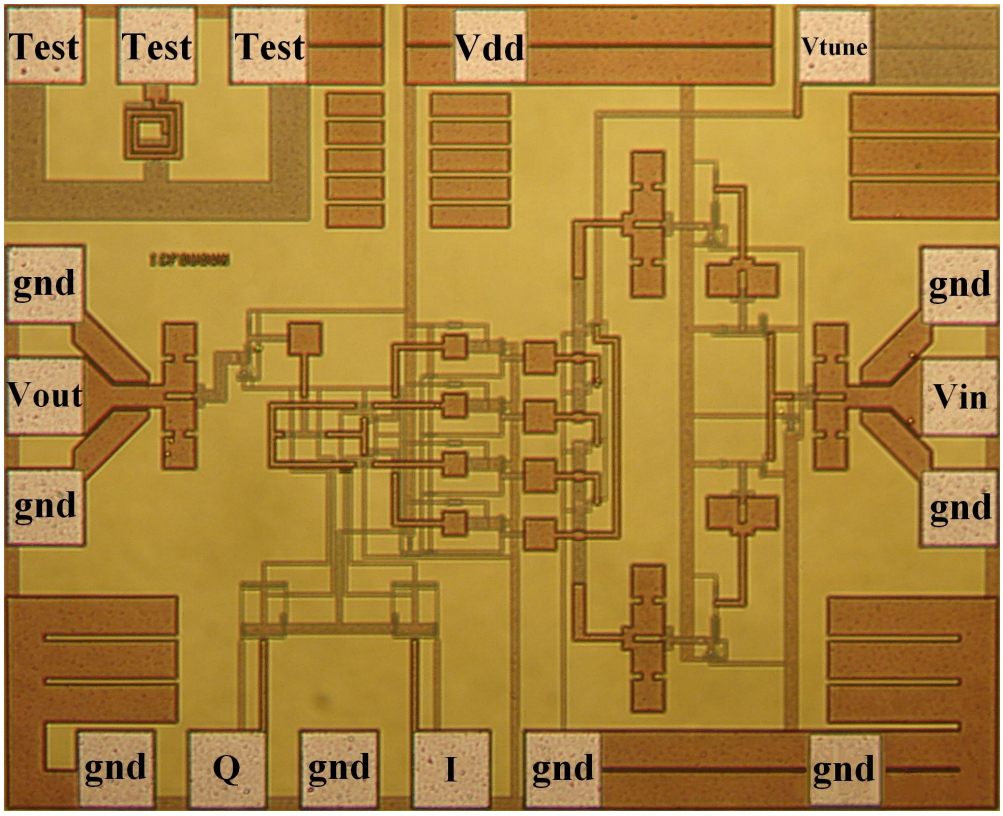

Figure 4.33: Photograph of S-Band QPSK modulator IC.

The first measurement performed was the signal constellation of the modulator with the I and Q data switches held at constant values corresponding to the four QPSK symbols (00, 10, 11, and 10). High (1.8V) and low (0V) voltage levels were applied to represent logic 1 and 0 respectively for the I and Q inputs depending on the constellation signal being measured. The magnitude of the transmission coefficient from the input to the output (S_{21}) in each of the four states is shown in Figure 4.34 from 2GHz to 3GHz. It is clear that the maximum loss exhibited at the centre frequency of 2.4GHz is about 5.5dB. In addition, the maximum amplitude balance is less than 0.3dB. The phase of the

transmission coefficient S_{21} in each of the four states is also shown in Figure 4.35 from 2GHz to 3GHz, indicating a maximum phase error of only 1.4° at the same frequency. These measurements were performed with the tuning voltage V_{TUNE} set to about 0.7V, as this was found to give the most accurate signal constellation at 2.4GHz. The measurements also reasonably agree with the simulation results in the previous section, with slight discrepancies due to component tolerances, device mismatch and other layout parasitics not accounted for during simulation.

The input (S_{11}) and output (S_{22}) reflection coefficients were also measured and similar plots of their magnitude are shown in Figures 4.36 and 4.37. At the centre frequency of 2.4GHz, the input and output reflection coefficients are less than -10 and -17dB respectively. These results are sufficiently low as desired, agreeing closely with our simulation results presented earlier.

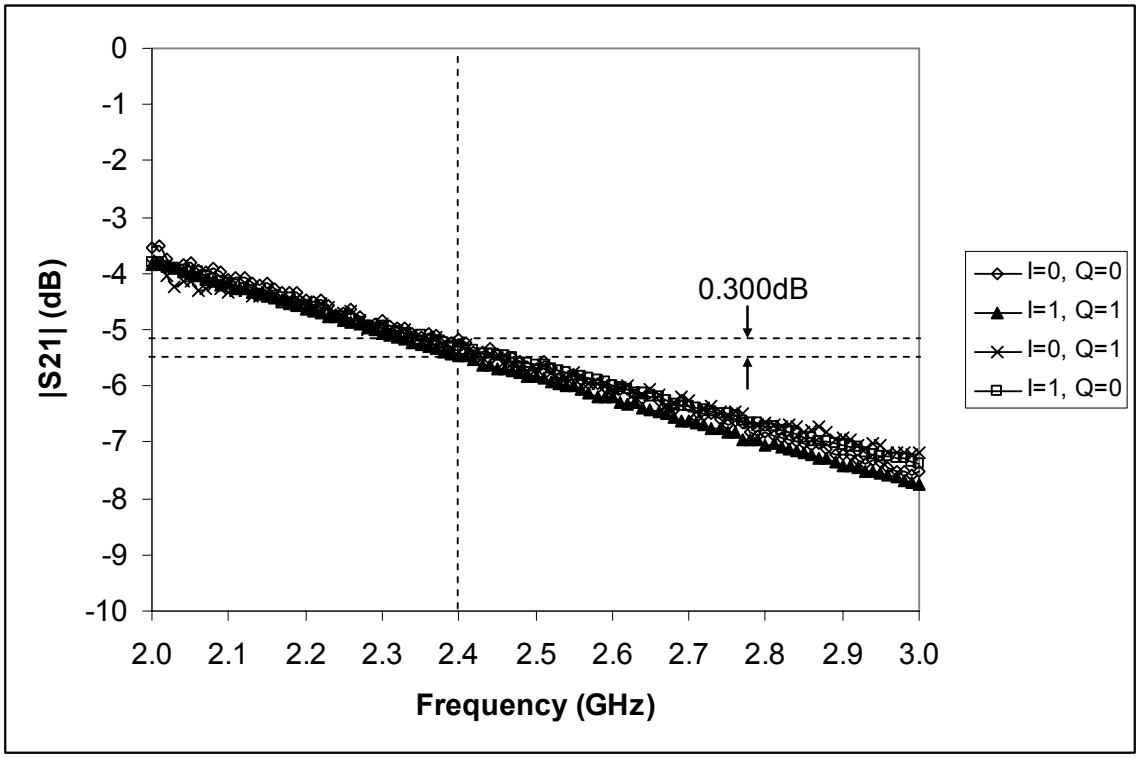

Figure 4.34: Measured transmission coefficient S21 magnitude for all I and Q.

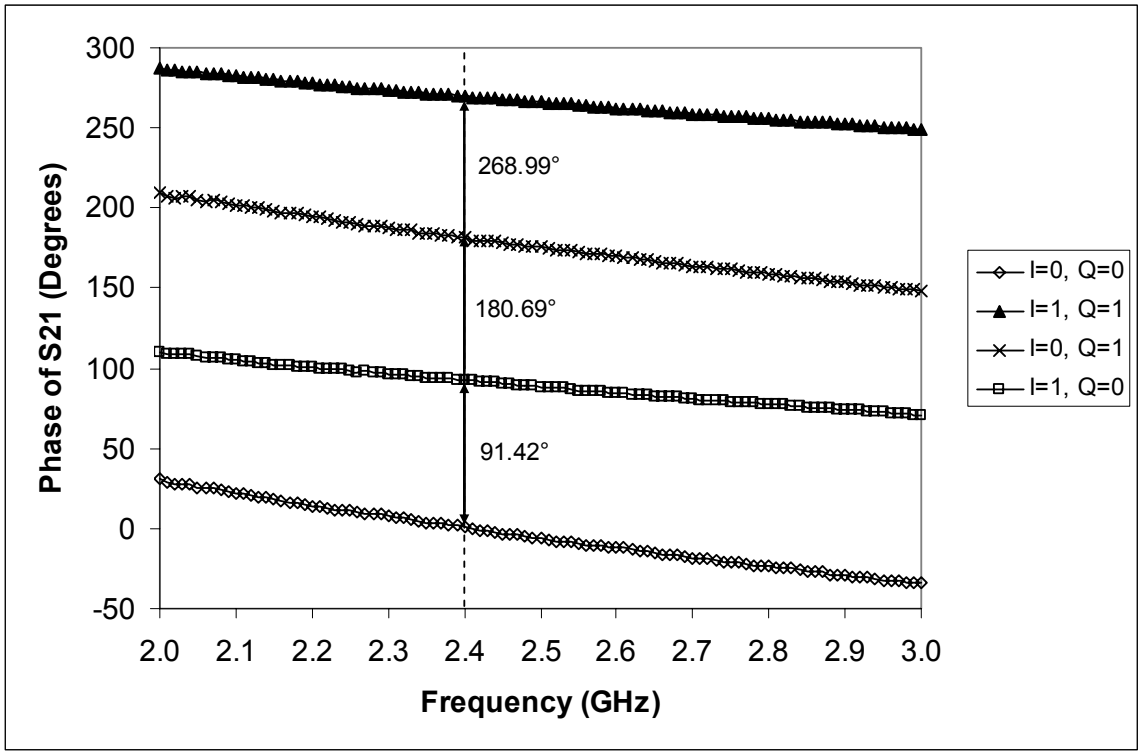

Figure 4.35: Measured transmission coefficient S21 phase for all I and Q.

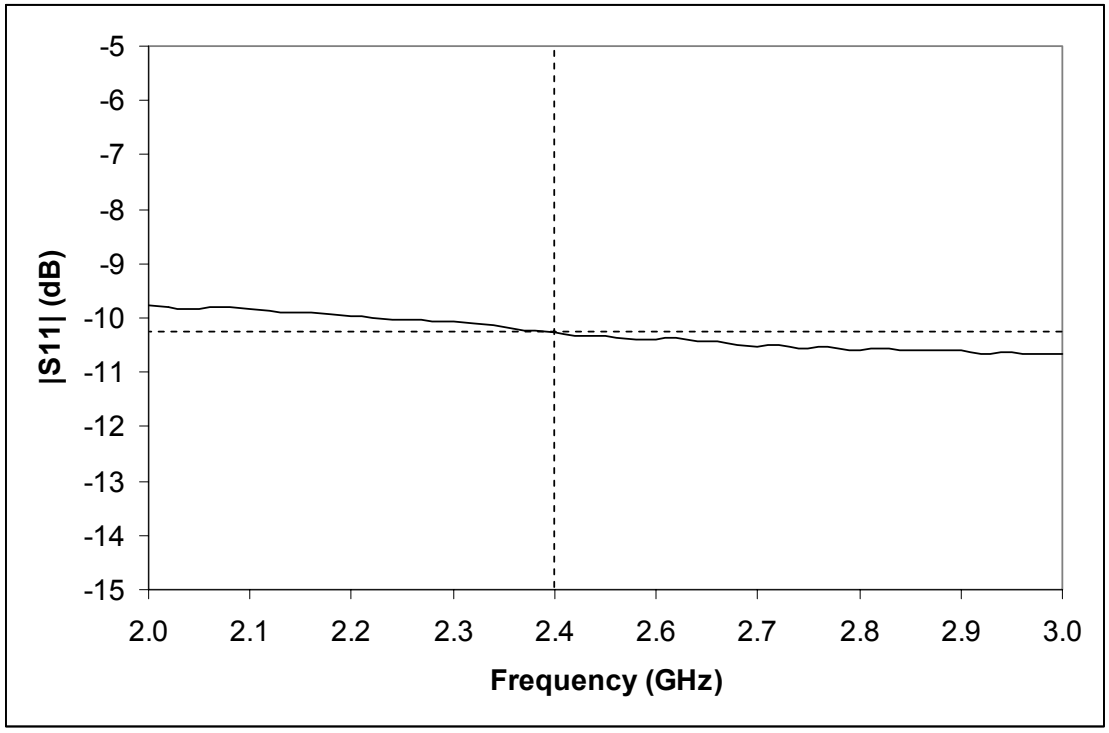

Figure 4.36: Measured input reflection coefficient S11.

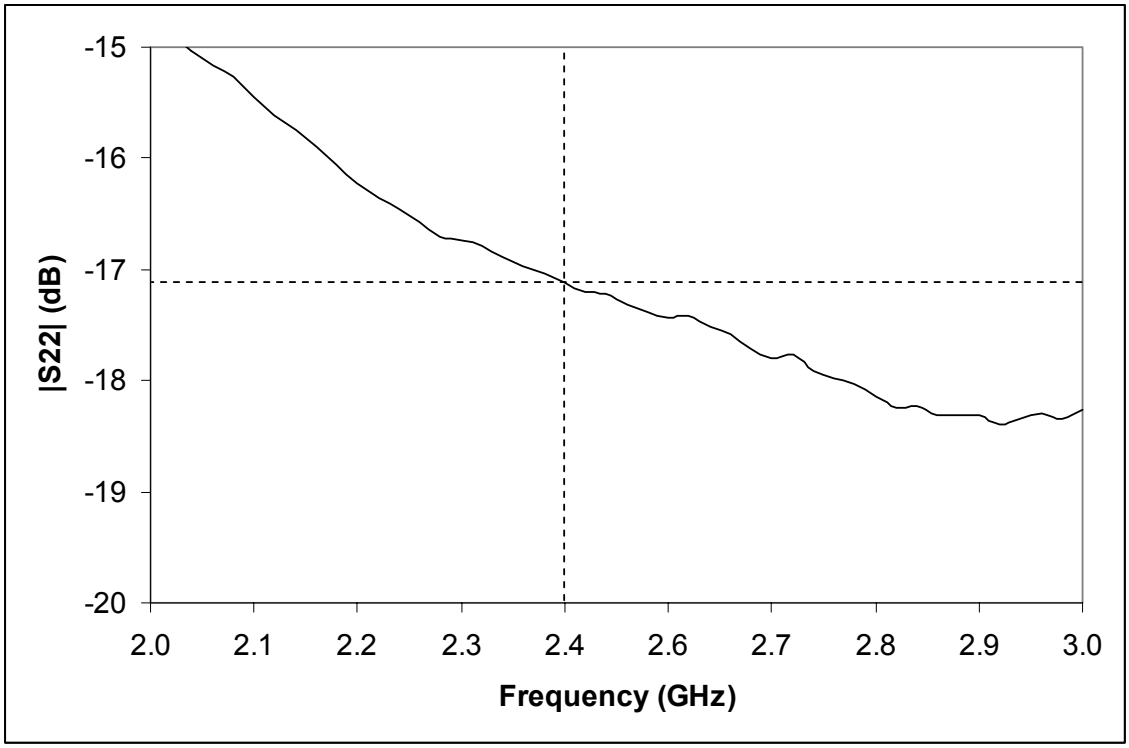

Figure 4.37: Measured output reflection coefficient S22.

To measure the QPSK modulator's carrier rejection, the same square wave is applied to both I and Q data channels, with an amplitude level of 1.8V (V_{dd}) in the high state and 0V (ground) in the low state. The output of the IC is then connected directly to the spectrum analyzer. The frequency of the square wave f_{MOD} is chosen to be 1MHz (time period $T = 1/f_{MOD} = 1\mu s$) for a 2Mbps data rate per channel or a total data throughput of 2Mbps × 2 channels = 4Mbps. Figure 4.38 shows the resulting output signal spectrum with a centre (carrier) frequency of 2.4GHz, a frequency span of 50 MHz and resolution bandwidth of 390kHz. The spectrum shape matches the theoretical one discussed in Chapter 3, with a high degree of symmetry around the centre frequency and well-defined nulls at the even-order harmonics. As depicted from the plot, the carrier is

also well suppressed by more than 32dB relative to the main lobes. This is close to the simulation result shown in Figure 4.32, albeit at a lower data rate.

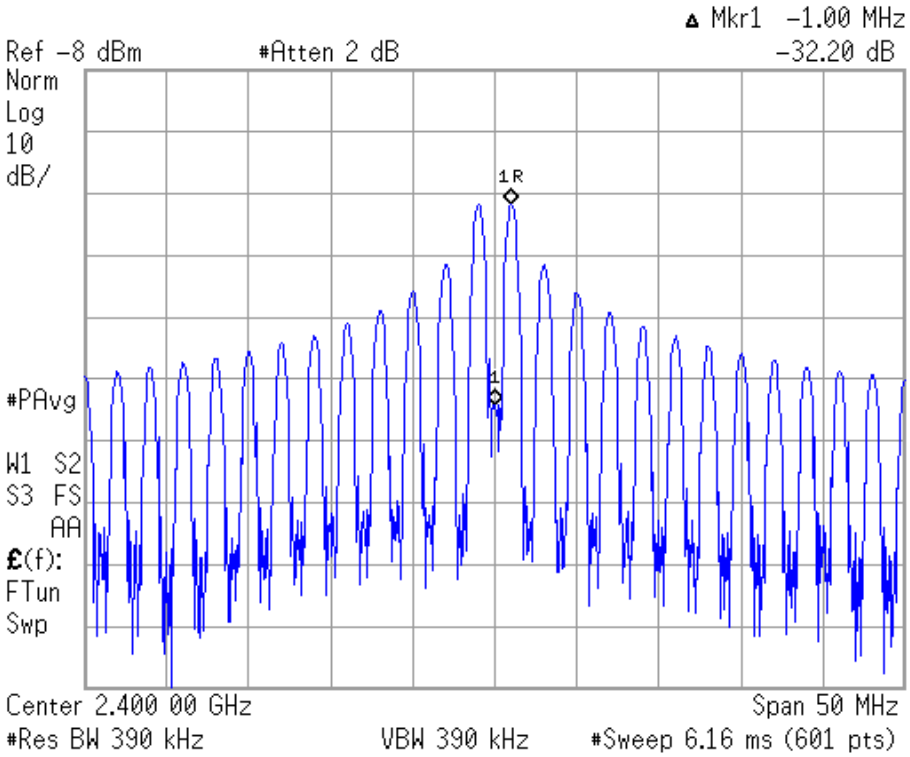

Figure 4.38: Measured carrier rejection with 1MHz square wave.

The carrier rejection of the QPSK modulator was also tested at higher speeds. The frequency of the square wave f_{MOD} was increased to 5MHz (time period $T = 1/f_{MOD} =$ 0.2µs) for a 10Mbps data rate per channel or a total data throughput of 10Mbps × 2 channels = 20Mbps. Figure 4.39 shows the resulting output signal spectrum with the same centre (carrier) frequency of 2.4GHz, a frequency span of 250MHz and resolution bandwidth of 2MHz. The spectrum shape is still quite good with the carrier suppressed by more than 32dB. However, although relatively small, a few imperfections are apparent including non-zero even-order components that are largely due to practical limitations. These may include the finite rise and fall times of the square wave signal, as

well as the finite switching time of the NMOS switches, which allow both paths in a complimentary pair to be simultaneously on. Such intervals become more significant as the symbol period is reduced, possibly leading to the discrepancies seen at higher frequencies.

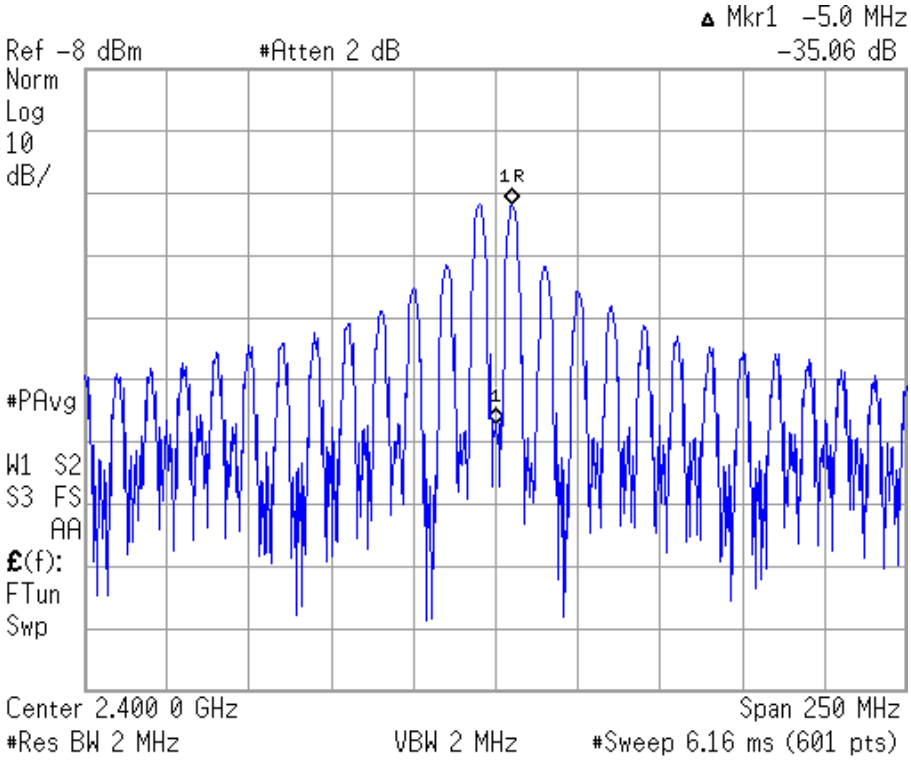

Figure 4.39: Measured carrier rejection with 5MHz square wave.

As the transmitted information in real-world communication systems is most often random as opposed to periodic, pseudo-random binary sequences (PRBS) with a 9-bit shift register were employed for the input *I* and *Q* data channels. The sequences were encoded in the non-return-to-zero (NRZ) format with rectangular pulses having an amplitude level of 0V (ground) in the low state and 1.8V (V_{dd}) in the high state. Their data rate was set to be 28Mbps (pulse width $T = 1/f_{MOD} \approx 36$ns) for a total data throughput of 28Mbps × 2 channels = 56Mbps. Finally, the output of the IC was directly connected to the spectrum analyzer. Figure 4.40 shows the resulting output signal spectrum with a

centre frequency of 2.4GHz and a frequency span of 280MHz. The resolution bandwidth and averaging of the spectrum analyzer were set to 3MHz and 100 points respectively. It is evident that the circuit operates as a QPSK modulator with its generated spectrum closely matching the theoretical QPSK power spectrum discussed in Chapter 2 (Figure 2.13). The output spectrum is also quite smooth with little or no imperfections in its sinc-squared shape.

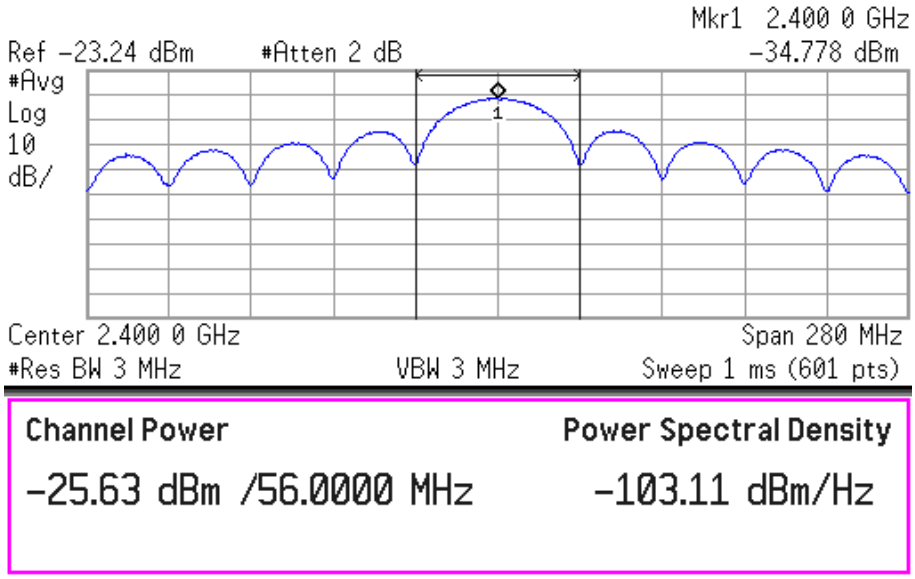

Figure 4.40: Measured output QPSK spectrum for 56Mbps.

Further tests were carried out to assess the modulator's performance at higher speeds. For data rates of 50 and 54Mbps per channel i.e. 100 and 108Mbps total, the measured output spectra of the modulator are shown in Figures 4.41 and 4.42. Both spectra are still quite smooth with only a few discrepancies that are relatively small. The data rate was then increased to 100Mbps per channel or 200Mbps total and the measured output spectrum in this case is shown in Figure 4.43. While the main (center) lobe of the spectrum remains mostly intact, there are visible discrepancies in the side lobes. This is most likely due to the intrinsic parasitics of the NMOS FETs and the associated coupling

between the I and Q digital data signals and the QPSK output signal. Other non-idealities include the finite rise and fall times of the generated square wave, along with the finite switching time of the NMOS switches, which allow both paths in a complimentary pair to be simultaneously on. Such intervals become more significant as the symbol period is reduced, possibly leading to the discrepancies observed at higher data rates.

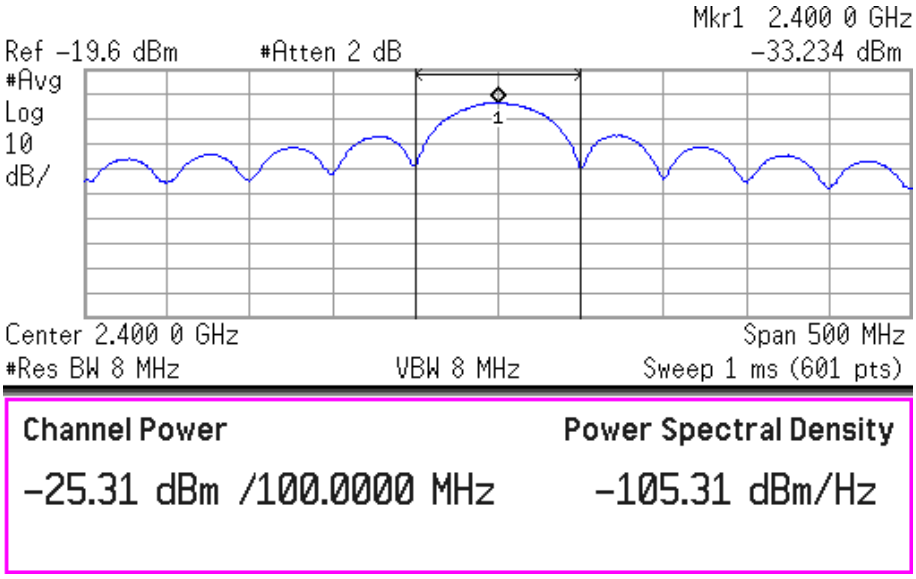

Figure 4.41: Measured output QPSK spectrum for 100Mbps.

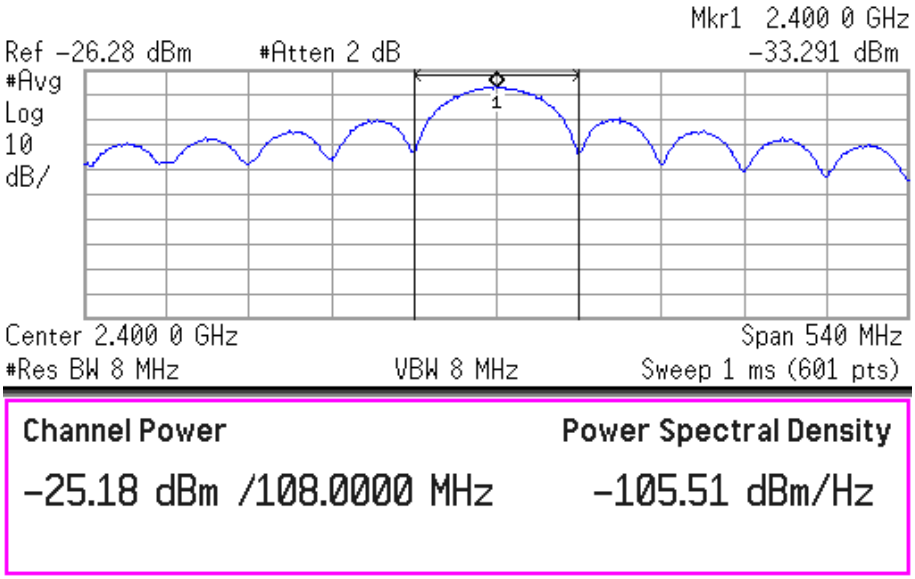

Figure 4.42: Measured output QPSK spectrum for 108Mbps.

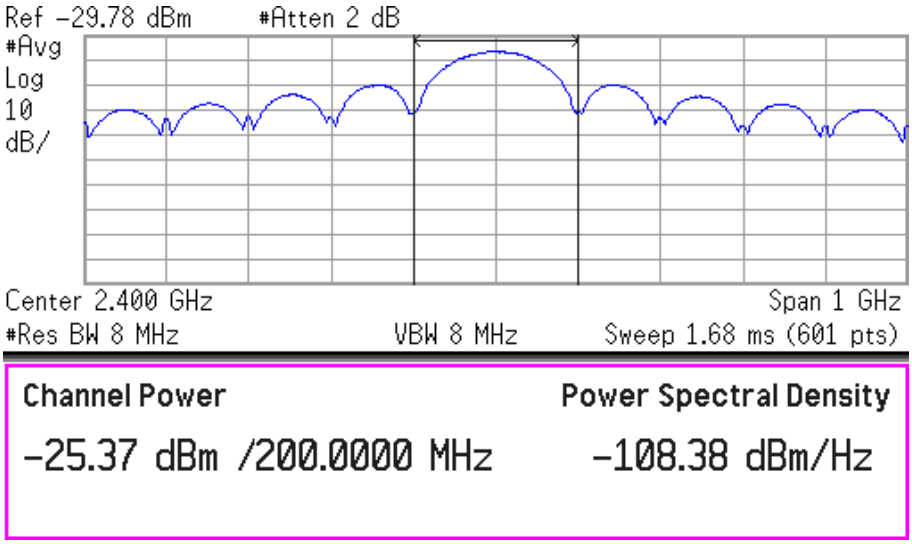

Figure 4.43: Measured output QPSK spectrum for 200Mbps.

Table 4.1 below summarizes the measured characteristics of the S-band QPSK modulator.

Table 4.1: Summary of measured characteristics of S-band QPSK modulator.

Characteristic	Results
Active Area	0.505 × 0.610mm
DC Power Consumption	34mW from 1.8V
Modulation Accuracy	Amplitude Error ≤ 0.3dB Phase Error ≤ 1.4°
Insertion Loss	< 5.5dB
Return Loss	Input: < -10dB Output: < -17dB
Carrier Rejection	> 32dB
Data Throughput	Nominal: 56Mbps Maximum: 200Mbps

The performance characteristics of our novel direct-digital QPSK modulators can now be evaluated against other work found in the literature. Table 4.2 below summarizes this work's performance in comparison with five other competitive direct-digital QPSK

modulators: [23], [25], [26], [59] and [60], that were designed for similar applications within the carrier frequency range of 1GHz to 4GHz.

Table 4.2: Comparison of the S-band QPSK modulator with other work.

	Characteristics				
	Technology	Area	DC Power	Accuracy (Errors)	Data Rate
[23]	0.5µm GaAs	$2.2\times2.4mm^2$	600mW at 8V	<0.8dB, <5°	4Mbps
[25]	0.8µm GaAs	$1.2\times1.2mm^2$	110mW at 3.1V	0.05dB, 1.1°	768Kbps
[26]	18GHz Si-Bipolar	$2.4\times0.68mm^2$	68mW at 2V	0.04dB, 1.6°	768Kbps
[59]	0.35µm CMOS	$0.85\times0.9mm^2$	188mW at 3.3V	0.09dB, 0.6°	15Mbps
[60]	0.18µm CMOS	$0.94\times0.94mm^2$	42mW at 1.8V	Not Available	14Mbps
This work	0.18µm CMOS	$0.51\times0.61mm^2$	33mW at 1.8V	<0.3dB, <1.4°	56Mbps

From Table 4.2 above, it is clear that our S-band QPSK modulator is superior in terms of size, power consumption and data rate, making it more suitable for portable high-speed wireless devices. However, the modulation accuracy seems to be only average compared to other work. It is important to note that for [25], [26] and [59] the modulation accuracy was characterized using single sideband (SSB) modulation where 90° out-of-phase sinusoids are applied at the I and Q data inputs, with the relative level of the suppressed sideband at the output (Image Rejection Ratio or IRR) being a function of the phase and amplitude imbalance of the quadrature RF carriers. In effect, this only includes errors between two quadrature vectors in the QPSK constellation, and not all four QPSK vectors are taken into account as performed in this work and [23].

Chapter 5

Conclusions

5.1 Summary

In this thesis, novel direct-digital QPSK modulators were proposed with new RF circuits devised in low-cost CMOS technology for portable wireless applications. First, a general overview of direct-digital modulators was given, demonstrating their potential benefits over the traditional heterodyne approach. The main advantage of direct-digital modulators is that several components in the traditional heterodyne architecture are not needed including the intermediate frequency (IF) oscillator, IF bandpass filter, IF amplifiers and the RF upconverter. Thus, direct-digital modulators can simplify the communication system and facilitate integration with existing digital CMOS circuits for a reduced size, cost and power consumption. To this end, a new direct-digital QPSK modulator concept was introduced where the carrier is modulated directly by the digital data using Pass-Transistor Logic (PTL) circuits consisting of NMOS switches. A major advantage of this topology is its relative simplicity in terms of size and power consumption compared to most other direct-digital QPSK modulators. The concept was demonstrated through the design of an L-band modulator followed by an enhanced tunable S-band version in 0.18μm CMOS technology showing very good performance with high data transmission rates.

The proposed L-band QPSK modulator first uses a 90° phase shifter to generate two quadrature signals from the RF carrier. The RC-CR network was chosen for this due to its small footprint and zero DC power consumption. Each quadrature signal is then split in a balun into balanced signals, yielding all four quadrature phases of the carrier: 0°, 90°, 180° and 270°. The baluns were implemented using an active circuit consisting of common-gate and common-source transistors (CG-CS) for compact area, ease of IC integration and wideband performance. One signal from the in-phase components of the carrier (0° and 180°) and another from the quadrature phase components of the carrier (90° and 270°) are later selected by two PTL circuits according to the in-phase (I) and quadrature-phase (Q) digital data values respectively. Finally, the chosen signals are subtracted to generate the resultant QPSK signal vector at the output, which is simply accomplished by using a differential pair of transistors. This eliminates the need for a passive structure, which would be prohibitively large at this frequency band.

A detailed analysis of the various components in the L-band modulator was performed and several simulations were carried out to verify its final design. The circuit was then experimentally demonstrated in a standard 0.18μm CMOS process with the measurements conducted at 1.7GHz showing good performance. The fabricated IC measured only 425μm by 850μm including bonding pads and consumed less than 43mW of power from a 1.8V supply. The supported data transmission rates exceeded 20Mbps, while the carrier suppression achieved was more than 40dB. However the small bandwidth of DC probes used to apply the I and Q digital data signals on the IC has limited the maximum data rate that can be tested. To alleviate this problem and facilitate

measurements at higher data rates, high-performance CPW probes should be used for the digital data signals as in the enhanced S-band modulator.

A new S-band direct-digital QPSK modulator was introduced that offers better performance and requires fewer components than the L-band modulator. A 180° balun first splits the input RF carrier into a pair of differential, balanced signals. The active CG-CS balun was also used here, providing a low input reflection coefficient over the entire 2GHz to 4GHz bandwidth without using any bulky matching networks. The 180° out-of-phase signals are then fed to the 90° phase shifter which generates differential quadrature signals, yielding all four quadrature phases of the carrier. The 90° phase shifter was implemented using an RC polyphase network for small footprint and zero DC power consumption. It also exhibits a lower signal loss compared to using two RC-CR circuits since it combines the two balanced signals in a quadrature fashion as opposed to splitting each signal separately. The resistors were implemented using NMOS FETs biased in the triode region with an effective voltage-controlled channel resistance. A definite advantage of this is that the RC polyphase network can be fine-tuned after process variations for the lowest possible phase error at our design frequency (2.4GHz). Equivalent circuit models and characteristic equations were developed for the NMOS FET in the triode region, from which the width and gate (tuning) voltage can be designed to yield the desired resistance value. Finally, only one of the four differential quadrature signals is selected by a Pass-Transistor Logic (PTL) circuit that consists of six NMOS switches, according to both I and Q digital data values. This eliminates the need for a summing junction to generate the QPSK signal.

The design of the S-band QPSK modulator circuit was verified with exhaustive simulations in Cadence using TSMC RF 0.18μm CMOS design kits. It was then experimentally demonstrated in a standard 0.18μm CMOS process with the measurements conducted at 2.4GHz showing very good performance. The fabricated IC occupied a die area of 0.720×0.888mm, with an active area of only 0.505×0.610mm. It consumed less than 19mA from a 1.8V voltage supply, i.e. 34mW of power. A very accurate QPSK signal constellation was achieved after tuning the RC polyphase filter as designed, with the phase and amplitude errors being less than 1.4° and 0.3dB respectively. The measured insertion loss was also lower than 5.5dB while the input and output return loss were better than -10 and -17dB respectively. The supported data transmission rates exceeded 56Mbps towards a maximum of 200Mbps, and a high carrier rejection of more than 32dB was achieved. These results are in close agreement with our simulations, indicating good design and predictability.

5.2 Future Work

A few additional enhancements and feature extensions for the direct-digital QPSK modulators can be suggested at this point as future work. For instance, two or three stagger-tuned stages of the RC polyphase filter can be cascaded with their cut-off frequencies logarithmically spaced out to achieve an accurate 90° phase shift over a wide frequency range. Since the active CG-CS balun also has a wideband frequency response with low amplitude and phase imbalance, the QPSK modulator can be potentially used over a broad range of carrier frequencies for various wireless communication systems. In addition, tunable components such as voltage-controlled resistors are no longer necessary in this case to adjust the polyphase filter's performance after fabrication, eliminating the

need for additional control voltages and DC bonding pads on the IC. Furthermore, careful circuit and device layout techniques, such as common-centroid layout for example, may be used to reduce component mismatch for lower amplitude and phase errors.

The proposed direct-digital QPSK modulator concept can also be extended for 8PSK modulation, which is used in some wireless communication technologies such as Enhanced General Packet Radio Service (EGPRS) to increase the spectrum efficiency for a higher data transmission rate or a narrower occupied bandwidth. In 8PSK modulation, the carrier phase takes on one of eight equally spaced values that are 45° apart depending on the binary value of three data bits. Therefore it can be implemented by adding a 45° phase shifter for example, along with additional 90° phase shifters, baluns and switches of course.

References

[1] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed., New Jersey: Prentice Hall, 2003.

[2] A. Joseph et al, "Status and Direction of Communication Technologies – SiGe BiCMOS and RFCMOS," *Proceedings of the IEEE*, vol. 93, no. 9, pp. 1539-1558, September 2005.

[3] J. Dunn et al, "Foundation of RF CMOS and SiGe BiCMOS Technologies", *IBM Journal of Research and Development*, vol. 47, no. 3, pp. 101-138, May 2003

[4] J. Weldon et al, "A 1.75-GHz Highly Integrated Narrow-band CMOS Transmitter with Harmonic-Rejection Mixers ," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 12, pp. 2003-2015, December 2001.

[5] A. Loke, and F. Ali, "Direct Conversion Radio for Digital Mobile Phones-Design Issues, Status, and Trends," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 11, pp. 2422-2435, November 2002.

[6] B. Razavi, *RF Microelectronics*, New Jersey: Prentice Hall, 1998.

[7] A. El-Gabaly, B. Jackson and C. Saavedra, "An L-Band Direct-Digital QPSK Modulator in CMOS," *URSI IEEE International Symposium on Signals, Systems and Electronics*, pp.563-566, July 2007.

[8] B. Razavi, "RF Transmitter Architectures and Circuits," *IEEE Custom Integrated Circuits Conference*, pp. 197-204, May 1999.

[9] J. Durec, "An Integrated Silicon Bipolar Receiver Subsystem for 900-MHz ISMband Applications," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 9, pp. 1352-1372, September 1998.

[10] N. Checka, D. Wentzloff, A. Chandrakasan and R. Reif, "The Effect of Substrate Noise on VCO Performance," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 526-526, June 2005.

[11] T. Liu and E. Westerwick, "5-GHz CMOS Radio Transceiver Front-End Chipset," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 12, pp. 1927-1933, December 2000.

[12] F. Stremler, *Introduction to Communication Systems*, 3rd ed., Upper Saddle River, NJ: Prentice Hall, 1990.

[13] S. Haykin, *Digital Communications*, 3rd ed., Mississauga, ON: John Wiley & Sons Canada, 1988.

[14] T. Rappaport, *Wireless Communications: Principles and Practice*, Upper Saddle River, NJ: Prentice Hall, 1996.

[15] J. Wu, F. Han, T. Horng, J. Lin, "Direct-Conversion Quadrature Modulator MMIC Design With a New 90° Phase Shifter Including Package and PCB Effects for W-CDMA Applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 6, pp. 2691-2698, June 2006.

[16] J. Itoh, M. Nishitsuji, O. Ishikawa, D. Ueda, "2.1GHz Direct-Conversion GaAs Quadrature Modulator IC for W-CDMA Base Station", *IEEE International Solid-State Circuits Conference*, pp. 226-227, February 1999.

[17] J.Itoh et al, "A Low Distortion GaAs Quadrature Modulator IC," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 55-58, June 1998.

[18] P. Eloranta, P. Seppinen, "Direct-Digital RF Modulator IC in 0.13µm CMOS for Wide-Band Multi-Radio Applications," *IEEE International Solid-State Circuits Conference*, pp. 532-533, February 2005.

[19] G. Carchon, D. Schreurs, W. De Raedt, P. Van Loock, and B. Nauwelaers, "A Direct Ku-Band Linear Subharmonically Pumped BPSK and I/Q Vector Modulator in Multilayer Thin-Film MCM-D," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 8, pp. 1374-1382, August 2006.

[20] W. Philibert and R. Verbiest, "A Subharmonically Pumped I/Q Vector Modulator MMIC for Ka-band Satellite Communication," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 183-186, June 2000.

[21] Y. Sun, A. Freundorfer and D. Sawatzky, "A QPSK Direct Digital Modulator in GaAs HBT at 28 GHz," *Canadian Conference on Electrical and Computer Engineering*, pp. 1882-1885, May 2005.

[22] P. Boutet, J. Dubouloy, M. Soulard and J. Pinho, "Fully Integrated QPSK Linear Vector Modulator for Space Applications in Ku-band," *European Microwave Conference*, pp. 389-392, October 1998.

[23] A. Boveda, F. Ortigoso and J. Alonso, "A 0.7-3 GHz GaAs QPSK/QAM Direct Modulator," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 12, pp. 1340-1349, December 1993.

[24] S. Altes, T. Chen and L. Ragonese, "Monolithic RC all-pass networks with constant-phase-difference outputs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 34, no. 12, pp. 1533-1541, December 1986.

[25] K. Yamamoto, K. Maemura, N. Andoh and Y. Mitsui, "A 1.9-GHz-Band GaAs Direct-Quadrature Modulator IC with a Phase Shifter," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 10, pp. 994-1000, October 1993.

[26] T. Tsukahara, M. Ishikawa and M. Muraguchi, "A 2-V 2-GHz Si-Bipolar Direct-Conversion Quadrature Modulator," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 2, pp. 263-267, February 1996.

[27] A. Teetzel, "A Stable 500 to 4000 MHz GaAs IQ Modulator IC," *IEEE International Solid-State Conference*, pp. 364-365, Feb 1997.

[28] R. V. Garver, "Broad-band diode phase shifters," *IEEE Transactions on Microwave Theory and Techniques*, vol. 20, no. 5, pp. 314–323, May 1972.

[29] C. Suckling, R. Pengelly, and J. Cockrill, "S-band Phase Shifter Using Monolithic GaAs Circuits," *IEEE International Solid-State Circuits Conference*, pp. 134–135, February 1992.

[30] M. Gingell, "Single Sideband Modulation Using Sequence Asymmetric Polyphase Networks", *Electrical Communication*, vol. 48, no. 1 and 2, pp. 21–25, 1973

[31] F. Behbahani, Y. Kishigami, J. Leete, and A. A. Abidi, "CMOS mixers and polyphase filters for large image rejection," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 6, pp. 873–887, June 2001.

[32] M. Borremans, M. Steyaert, and T. Yoshitomi, "A 1.5 V, Wide Band 3GHz, CMOS Quadrature Direct Up-converter for Multi-mode Wireless Communications," *IEEE Custom Integrated Circuits Conference*, pp. 79–82, May 1998.

[33] P. Khannur and K. Ling, "A 2.45GHz Fully-Differential CMOS Image-Reject Mixer for Bluetooth Application," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 439-442, June 2002.

[34] E. Tiiliharju and K. Halonen, "A 0.75-3.6GHz SiGE Direct-Conversion Quadrature-Modulator," *European Solid-State Circuits Conference*, pp. 565-568, Sept 2003

[35] D. Pozar, *Microwave Engineering*, 3rd ed., Hoboken, NJ: John Wiley and Sons Inc, 2005.

[36] B. Razavi, "Architectures and Circuits for RF CMOS Receivers," *IEEE Custom Integrated Circuits Conference*, pp. 197-204, May 1999.

[37] B. Gilbert, "A Precise Four-Quadrant Multiplier with Subnanosecond Response," *IEEE Journal of Solid-State Circuits*, vol. 3, no. 4, pp. 365-373, December 1968.

[38] T. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge, UK: Cambridge University Press, 1998.

[39] S. Wu and B. Razavi, "A 900-MHz/1.8-GHz CMOS Receiver for Dual-Band Applications," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, pp. 2178-2185, December 1998.

[40] B. Razavi, "A 5.2-GHz CMOS Receiver with 62-dB Image Rejection", *IEEE Journal of Solid-State Circuits*, vol. 36, no.5, pp. 810 – 815, May 2001.

[41] A. Carrera, M. Rodriguez, G. Rohmer, "A Comparison of 0.35-/spl mu/m CMOS Image-Reject Mixer Architectures for LV-LP operation", *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pp. 92 – 95, April 2003.

[42] H. Hashemi and A. Hajimiri, "Concurrent Multiband Low-Noise Amplifiers-Theory, Design and Applications", *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp.288-301, January 2002.

[43] P. Gould, C. Zelley, and J. Lin, "CMOS Resistive Ring Mixer MMIC's for GSM 900 and DCS 1800 Base Station Applications," in *IEEE MTT-S International Microwave Symposium Digest*, vol. 1, June 2000, pp. 521–524.

[44] A. Shahari, D. Shaeffer, and T. Lee, "A 12-mW Wide Dynamic Range CMOS Front-End for a Portable GPS receiver," *IEEE Journal Solid-State Circuits*, vol. 32, no. 12, pp. 2061–2070, Dec. 1997.

[45] S. Chehrazi, R. Bagheri, and A. Abidi, "Noise in Passive FET Mixers: A Simple Physical Model," *IEEE Custom Integrated Circuits Conference*, pp. 375-378, October 2004.

[46] S. Zhou and M. F. Chang, "A CMOS Passive Mixer With Low Flicker Noise for Low-Power Direct-Conversion Receiver," *IEEE Journal of Solid State Circuits*, vol. 40, no. 5, pp. 1084-1093, May 2005.

[47] C. E. Saavedra and Y. Zheng, "A BPSK Modulator Using a Ring Hybrid and HFET Switches," *Asia-Pacific Microwave Conference*, pp. 1665-1668, December 2006.

[48] B. R. Jackson and C. E. Saavedra, "2.4 GHz Direct-Digital Binary Phase Shift Keying Modulator using a MEMS Switch," *IEE Electronics Letters*, vol. 40, no. 24, pp. 1539-1540, November 2004.

[49] J. Long and M. Copeland, "A 1.9 GHz Low-Voltage Silicon Bipolar Receiver Front-End for Wireless Personal Communication Systems," *IEEE Journal of Solid State Circuits*, vol. 30, no. 12, pp. 1438-1448, December 1995.

[50] H. Chen et al., "A Novel LNA-Mixer Design with On-Chip Balun," *IEEE International Symposium on Circuits and Systems*, pp. 4971-4974, May 2006.

[51] J. Long, "A Low-Voltage 5.1–5.8-GHz Image-Reject Downconverter RF IC," *IEEE Journal of Solid State Circuits*, vol. 35, no. 9, pp. 1320-1328, September 2000.

[52] J. Long, "Monolithic Transformers for Silicon RF IC Design," *IEEE Journal of Solid State Circuits*, vol. 35, no. 9, pp. 1368-1382, September 2000.

[53] H. Koizumi, S. Nagata, K. Tateoka, K. Kanazawa, and D. Ueda, "A GaAs Single Balanced Mixer MMIC with Built-in Active Balun for Personal Communication Systems'. *IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium*, pp. 77–80, May 1995.

[54] B. Frank, "MOSFET Operation," in *ELEC-853 Notes*. Kingston, ON: Queen's University, 2003. [Online]. Available: Queen's University Learning Wiki Online, http://bmf.ece.queensu.ca/mediawiki/index.php/ELEC-853_Notes. [Accessed: July 1st, 2007].

[55] M. Kawashima, T. Nakagawa, and K. Araki, "A Novel Broadband Active Balun," 33rd European Microwave Conference, vol. 2, pp. 495-498, October 2003.

[56] J. Lin, C. Zelley, O. Boric-Lubecke, P. Gould, and R. Yan, “A Silicon MMIC Active Balun/Buffer Amplifier with High Linearity and Low Residual Phase Noise,” *IEEE MTT-S International Microwave Symposium*, vol. 3, pp. 1289-1292, June 2000.

[57] C. E. Saavedra and B. R. Jackson, "Voltage-Variable Attenuator MMIC using Phase Cancellation," *IEE Proceedings Circuits, Devices, and Systems*, vol. 153, no. 5, pp. 442-446, October 2006.

[58] R. Mukhopadhyay et al., “Reconfigurable RFICs in Si-Based Technologies for a Compact Intelligent RF Front-End,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 1, pp.81-93, January 2005.

[59] Y. Zhou and J.Yuan, “A 1 GHz CMOS Current-Folded Direct Digital RF Quadrature Modulator,” *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 25-28, June 2005

[60] T. Ou and C. Tzuang, “Direct Radio-Frequency Digital Angle Modulator,” *IEEE Electronic Letters*, vol. 39, no. 7, pp. 594-595, April 2003