

Pixel Architectures for Digital Imaging Using Amorphous Silicon Technology

by

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Abstract

This work extends amorphous silicon (a-Si) TFT technology from traditional switching applications to on-pixel small signal amplification for diagnostic medical digital imaging applications. The developed a-Si pixel amplifier offers improved signal-to-noise ratios, lower cost, and less off-panel circuit complexity compared to its (traditional) a-Si switch counterpart. The pixel amplifier advances the state-of-the-art by offering a large area real-time imaging solution for low-noise fluoroscopic medical imaging that is not viable with current a-Si switch based pixels. More significantly, the pixel (because of its circuit gain) offers potentially reduced patient x-ray doses for other medical imaging modalities, hence improving the safety standards associated with current x-ray imaging practices.

Investigations of additional noise due to the a-Si pixel amplifier indicate that this noise is minimized for small pixel capacitance implying the need for low capacitance detectors such as amorphous selenium (a-Se) photoconductors. However, in contrast with CMOS amplified pixels, the flicker noise added by the a-Si readout circuit is comparable to the traditionally prohibitive reset noise. Measurements on in-house TFTs and pixel readout circuits indicate the feasibility of amorphous silicon APS pixels for low noise, diagnostic medical imaging applications such as digital fluoroscopy.

Appropriate bipolar bias voltages in the TFT ON and OFF states minimize the characteristic threshold voltage shift of the a-Si TFTs in the amplified pixel. Due to intrinsic feedback, the developed amplified pixel readout circuit has a compensatory effect on the pixel's gain. This gain compensation, coupled with small (typically $< 0.1\%$) duty cycles for diagnostic medical imaging applications leads to a $< 5\%$ variation in circuit gain over a 10,000 hour array lifetime.

In order to obtain high fill factor, the three TFTs in the a-Si amplified pixel are assumed embedded under the sensor unlike the conventional co-planar layout of sensor and TFTs. The major challenge with vertically stacked architectures is an increase in TFT leakage current due to the presence of an overlying sensor back electrode. An in-house fabricated vertically stacked pixel based on a double gate TFT illustrates how a low leakage current can be obtained even in the presence of a bias on an overlying sensor back electrode.

Lastly, the integration of an in-house amplified pixel a-Si TFT array with a continuous layer a-Se photoconductor X-ray detector is detailed including its design, fabrication and custom test

setup. Results from double sampled array operation including x-ray sensitivity, gain and noise are promising and highlight the feasibility of a-Si amplified pixel arrays coupled with a-Se x-ray detectors for diagnostic medical x-ray imaging applications.

The research presented in this thesis indicates that proper circuit and pixel architecture design can overcome a-Si material shortcomings related to area, noise and metastability. The demonstrated gain, noise, and stability results indicate that a-Si on-pixel amplifiers, coupled with a low capacitance, well established x-ray detection technology such as a-Se, can meet even the stringent requirements of low noise, digital fluoroscopy (less than 1000 input referred noise electrons) without resorting to newer high x-ray absorption materials such as PbI. The results presented provide the impetus to expedite development of large area a-Si APS arrays for low noise, real-time medical imaging.

For my parents, my brother, and most importantly, for Ama

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Chapter 1. Introduction

Pixelated arrays of electronics in amorphous silicon (a-Si) technology, routinely used for liquid crystal displays, are now being extended to several new and significant application areas in large area digital imaging [1][2]. Interest in a-Si technology stems from a variety of desired material and technological attributes. The low temperature deposition ($<300^{\circ}\text{C}$), high uniformity over large area, few constraints on substrate size, material, or topology, standard integrated circuit (IC) lithography processes, and low capital equipment cost associated with the a-Si material, are some of the benefits of large area a-Si technology. Notable application areas include: contact imaging for document scanning, digital copiers, and fax machines; color sensors/imaging; position/motion detection; radiation detection/imaging of X-rays in biomedical applications, gamma-ray space telescopes, airport security systems, and non-destructive testing of mechanical integrity of materials or structures [1][3][4].

This thesis deals with circuit, process, and device architecture development for large area, digital imaging applications using amorphous silicon (a-Si) technology with a focus on diagnostic medical imaging. This chapter introduces fundamental challenges posed by diagnostic medical imaging to large area, a-Si digital imaging technology. In addition, an outline is presented of how these basic challenges are addressed in the bulk of the thesis.

1.1 Digital Imaging

The most commonly used method to detect x-rays is to convert the radiation to visible light through a phosphor screen, which is subsequently detected by a light sensitive film. Modern screen-film systems typically employ one or a pair of phosphor screens in combination with light sensitive film packaged in a light-tight cassette. This system, which

has been accepted by radiologists for nearly a century, provides for good quality x-ray images. The main drawbacks of the screen-film system are storage costs and digital incompatibility. Another method that is widely used particularly in real-time fluoroscopic imaging [5] is the image-intensifier tube, which is integrated with a CCD or CMOS camera. Here, x-rays first interact with the input phosphor to produce optical photons, which in turn eject electrons from the photocathode. The electrons are accelerated across the vacuum tube and are focused on an output phosphor to produce optical photons, which are then viewed by a camera. This method employs multiple transduction steps to convert x-rays to visible light, which compromises image quality. Moreover, the complex lens and mechanical systems, and the assembled arrays of CCD or CMOS lead to cost and size issues.

As an alternative to these conventional detection methods, large area active matrix flat panel digital x-ray imagers (AMFPIs) based on the a-Si technology have been developed over the past decade. The motivation for developing AMFPIs targeted towards medical imaging applications includes improved image quality, large area x-ray imaging capability, a compact flat panel structure, low storage cost, better waste management since photographic film is obviated, and computerized handling/storage of sensory information.

There are two architectures currently employed in large area AMFPIs: the linear architecture, used in photocopiers, fax machines, and scanners, and the two-dimensional array architecture, employed in digital (including video) lens less cameras as well as x-ray imaging systems. In both linear and array architectures, the basic imaging unit is the pixel, which consists of an image sensor and a switch. The pixel is accessed by a matrix of gate and data lines, and operated in storage (or integration) mode. Here, during the off-period of the switch, the sensor charge is integrated, and when the switch is turned on, the charge in the sensor is transferred to the data line where it is detected by a charge sensitive amplifier. There are various metallic lines used to control the readout of the imaging information from the array of pixels. The imaging system is completed with peripheral circuitry that amplifies, digitizes, and synchronizes the readout of the image and a computer that manipulates and distributes the final image to the appropriate soft- or hard-copy device. A schematic diagram of a complete flat-panel x-ray imaging system is shown in Figure 1. Recently, a-Si AMFPIs using the sensor-and-switch pixel architecture with areas of $30 \times 40 \text{ cm}^2$ were demonstrated for diagnostic medical chest radiography [6].

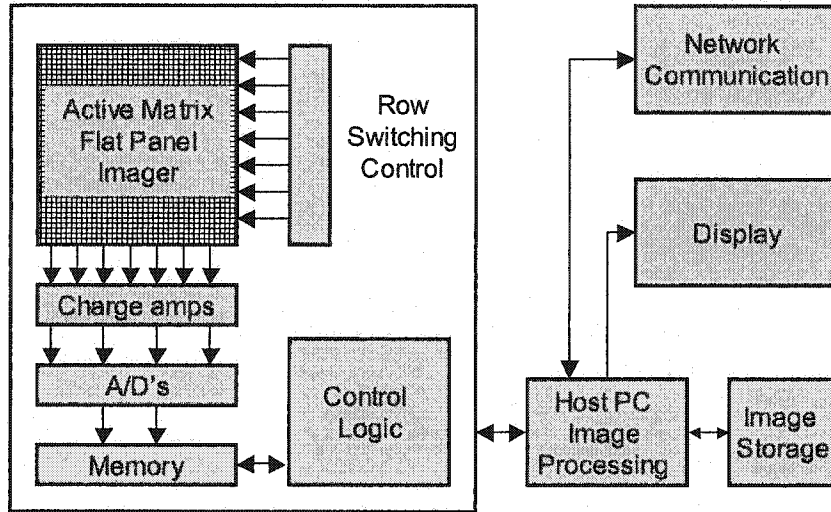


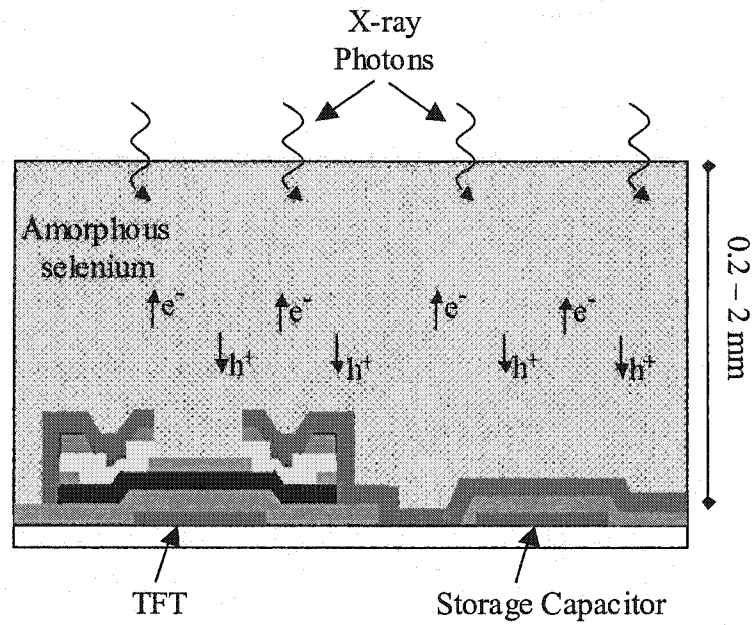
Figure 1. AMFPI Imaging System diagram [5]

1.2 Detection Schemes

The detection schemes for x-rays are divided into two categories: direct detection, where the x-rays are directly absorbed and converted to electrical charge in the detector; and indirect detection, where the x-rays are first converted into visible light by a phosphor layer, which in turn is converted to electrical charge in the photodetector. The electrical charge is read out by means of an a-Si active matrix thin film transistor (TFT) array.

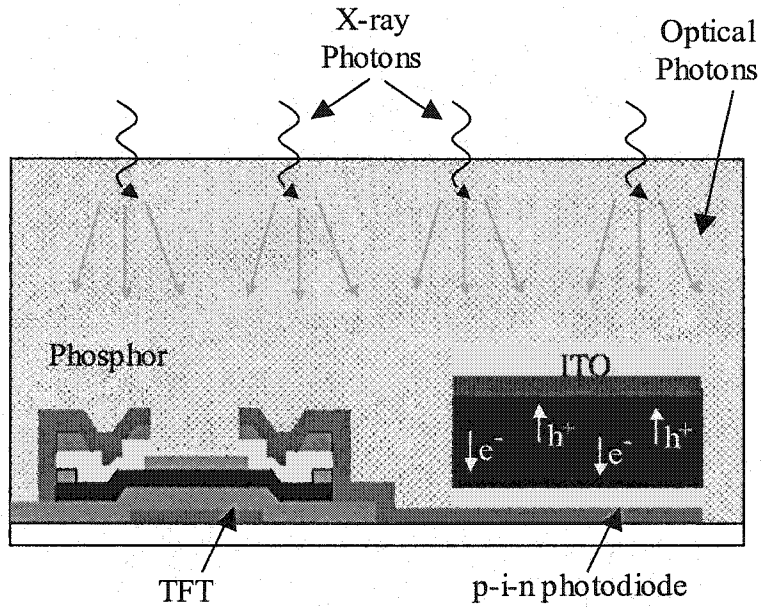
In the direct detection scheme, a thick photoconductor, such as amorphous selenium (a-Se), is deposited over the a-Si active matrix [5], as depicted in Figure 2(a). Incident x-rays are absorbed in the a-Se film and directly converted to electron-hole (e-h) pairs, which are then collected by an electric field that is applied across the photoconductor layer. A high electric field ($\sim 10 \text{ V}/\mu\text{m}$) is required to separate the e-h pairs. Normally, a $500 \mu\text{m}$ thick a-Se layer is required to absorb all of the x-rays, and a bias voltage as high as 5-10 kV is applied across the a-Se film for efficient charge collection. The indirect detection scheme, as shown in Figure 2(b), relies on a phosphor layer that is either assembled or integrated with the photodetector. The phosphor film absorbs the incident x-ray photons and produces high energy electrons, which in turn generate many electron-hole pairs in the phosphor. Visible

light is emitted from the phosphor when the electrons and holes recombine, and is detected by a-Si image sensor arrays located beneath the phosphor film.



X-ray $\rightarrow$ e-h pairs $\rightarrow$ q

(a)



X-ray $\rightarrow$ visible light $\rightarrow$ e-h pairs $\rightarrow$ q

(b)

Figure 2. (a) Direct x-ray detection method using a-Se and (b) Indirect x-ray detection method based on ITO/a-Si Schottky photodiode integrated with phosphor [5].

To be able to replace and improve upon current medical imaging techniques, the digital counterparts must meet the same performance criteria as existing x-ray imaging technologies. For example, the digital imager must cover the same field of view as conventional techniques as well as meet the appropriate resolution requirements for each modality. Also, the digital imager must meet the requirements on x-ray spectrum and mean exposure to the detector as determined from current clinical practices. The constraints on detector and pixel size are summarized in Table 1.

Table 1. Design requirements for digital x-ray detectors [5].

	Radiography	Mammography	Fluoroscopy
Imager size(cm)	35 x 43	18 x 24	25 x 25
Pixel size (μm)	100-150	50	150-200
Pixel count	1750 x 2150	3600 x 4800	1000 x 1000
Readout time(s)	< 5	< 5	0.033/frame
X-ray energy (kVp)	80-130	25-50	80
Exposure (mR)	0.03 – 3	0.6 – 240	0.0001 – 0.01
Patient thickness (cm)	20	5	20
Object size	0.5 mm (bone detail)	50-100 μm ($\mu\text{calcifications}$)	2 mm

Attention is drawn to three specific items in Table 1 that comprise the major challenges posed by diagnostic medical imaging applications to the current generation of large area, a-Si flat panel digital imagers. First, fluoroscopy is a real-time modality with very low patient exposure. The minimum x-ray input signal yields merely 1000 signal electrons (for both direct and indirect x-ray detection schemes) making the input vulnerable to noise added by the external readout electronics. Next, the pixel size for mammography must be less than or equal to $50 \times 50 \mu\text{m}$ while maintaining high fill factor for adequate resolution in breast imaging. Lastly, the pixel count for all modalities is greater than 1000×1000 making the AMFPI interface to off-panel external electronics bulky unless some form of on-panel multiplexing is implemented. Of the three modalities presented in Table 1, fluoroscopy has the most stringent requirements of low noise and real-time operation while mammography needs small area pixels for high-resolution imaging.

1.3 Thesis Organization

The focus in this thesis is primarily on a large area a-Si technology imaging solution for digital fluoroscopy. First, alternatives to the traditional a-Si TFT switch based pixel readout circuit architecture are examined in Chapter 2. Here, a current mode amplified pixel architecture (C-APS) is innovated that provides on-pixel gain to boost the noise-vulnerable fluoroscopic x-ray input signal. The C-APS gain is programmable via choice of supply voltage and sampling time and larger gains can be achieved by decreasing pixel capacitance. More significantly, the pixel gain can potentially reduce the x-ray dose to the patient hence improving the safety standards for other diagnostic medical imaging modalities. In addition, the C-APS is capable of real-time readout and its amplified output is amenable to on-panel multiplexing.

The C-APS pixel has three *in situ* TFTs as compared to traditional single TFT switch based readout circuits. Thus, the large sizes of a-Si TFTs could undermine fill factor for C-APS pixels if conventional co-planar methods of placing the sensor and TFTs are used. To achieve high fill factor pixels, we investigate vertically stacked pixel architectures in Chapter 3. Here, two aspects of vertical stacking are examined: avoiding high TFT leakage when the sensor back electrode overlaps the underlying TFTs and minimizing parasitic capacitance by using a thick, low-k insulating layer as an interlevel dielectric between the pixel TFTs and sensor. The vertically stacked pixel architecture developed and tested in Chapter 3 also holds the promise of achieving near 100% fill factor pixels for mammography that is challenging to achieve with current co-planar methods of placing the sensor and TFT. Lastly, the current in-house TFT process was extended to a reliable imaging array process for integration with a continuous layer a-Se photoconductor for x-ray detection.

Amorphous silicon TFTs suffer from a bias stress related characteristic threshold voltage shift (ΔV_T) that was previously characterized for TFT switch applications. In the C-APS however, the TFTs are used as both switches and amplifiers. In addition, TFTs used in large area imagers suffer from pulsed bias voltages rather than simply dc bias stress. To address these issues, dc and pulse bias characterization of a-Si TFTs used as switches and amplifiers is presented in Chapter 4, in order to facilitate ΔV_T device models to predict C-APS performance over a 10,000 hour imager lifetime. The developed a-Si TFT ΔV_T models

predict a lifetime variation in gain of less than 5% for the C-APS pixel architecture and can also be used to predict ΔV_T for many circuits in emerging analog applications of a-Si TFTs such as OLED displays.

The C-APS is particularly promising for digital fluoroscopy because its on-pixel gain can amplify the noise vulnerable fluoroscopic input signal above the noise floor of the external off-panel readout circuitry. However, additional noise due to the a-Si on-pixel amplifier readout circuit can potentially degrade the noise performance of the C-APS. In order to determine the overall noise added by the C-APS pixel readout circuit, fundamental studies were undertaken in Chapter 5 to determine and model low frequency (thermal and flicker) a-Si TFT noise. In addition, reset noise, which is traditionally the largest noise source in CMOS APS imaging pixels, was measured and modeled for a-Si TFT switches. Finally, small-signal noise analysis of the C-APS readout circuit along with measurements presented in Chapter 5 conclude the feasibility of a-Si TFT based C-APS circuits for large area, digital fluoroscopic imaging. The a-Si TFT thermal, flicker, and reset noise models developed in this chapter enable the determination of noise performance for a large variety of a-Si TFT imaging pixel readout circuits.

Chapter 6 describes the integration of an a-Si TFT-based C-APS array with a direct x-ray detection scheme employing an a-Se photoconductor. Here, the design, fabrication and test of an a-Se C-APS imager is presented. Measured data is in good agreement with simulations and includes x-ray sensitivity, gain and imager noise performance results. Lastly, Chapter 7 concludes this research and summarizes the contributions of this thesis to the field of amorphous silicon technology.

Chapter 2. Pixel Architectures

This chapter describes different pixel readout circuit architectures for digital imaging applications. The basic operation of the architectures is presented with a focus on gain, linearity and readout rate. The chapter starts by introducing the currently popular a-Si TFT switch based passive pixel sensor (PPS) architecture and highlights some benefits and difficulties. Then, two a-Si TFT based active pixel sensors (APS) are introduced that attempt to address the shortcomings of the PPS for diagnostic medical imaging applications.

For those readers unfamiliar with the operation of a-Si TFTs, an introduction is provided in Appendix A. In addition, a number of simulations carried out in this research were based on an in-house physical model [46] implemented by the author in VHDL-AMS [47]. A brief description of the model as well as the model code is included in Appendix B. Lastly, parameter extraction for TFTs is required for simple hand calculations throughout this chapter and the rest of the thesis. Unless explicitly specified, TFT parameters are extracted using the saturation method described in Appendix C.

2.1 Passive Pixel Sensor

2.1.1 Introduction

The passive pixel, first introduced by Gene Weckler in 1967, is the workhorse of the digital x-ray imaging industry. A PPS (see Figure 3) consists of a sensing element (e.g. a-Se photoconductor or a-Si photodiode biased in the integration mode) and a switch. The data line is connected to a column charge amplifier to convert the accumulated signal on the charge detection node, V_x , into a stable voltage for image processing by external electronics.

For the PPS architecture, the TFT gate is connected to a common row gate signal line and a scanning clock generator addresses all the rows. During read-out, a row of TFT switches is activated via a gate line by the clock generator sequentially. The signal charge from each pixel is transferred through common data lines into column charge amplifiers. The amplified signals are then digitized by an A/D converter and sent for image processing.

2.1.2 Operation

There are three modes of operation for the PPS:

- Integration Mode: Signal charge accumulates on C_{PIX} (sum of sensor and parasitic capacitances at node V_x) proportional to the amount of x-ray radiation.
- Readout/Reset Mode: Following integration, the accumulated signal charge is transferred from C_{PIX} to the column charge amplifier simultaneously causing pixel readout and reset to occur. The pixel capacitance, C_{PIX} , is reset to some steady state value determined by the charge integrator positive input before the next signal integration begins.

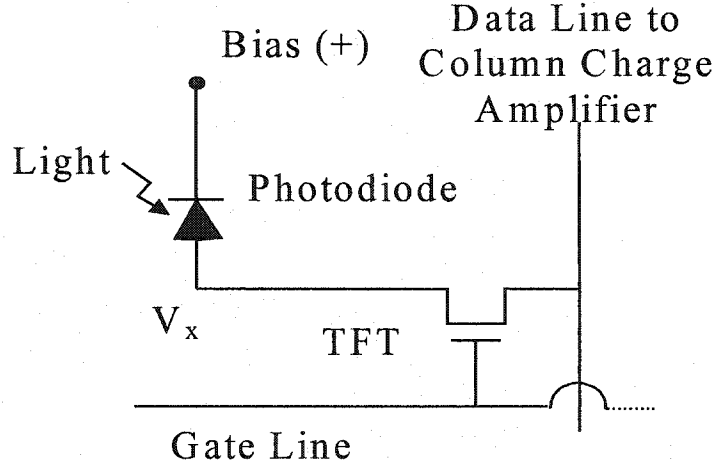


Figure 3. Passive pixel sensor architecture.

Charge accumulated on C_{PIX} is read out through the TFT ON resistance and converted to a voltage via the column charge amplifier. During readout, the TFT is biased in the linear region to provide a low ON resistance for quick readout. When the TFT is OFF, it is biased to be non-conducting. However, a small leakage current (on the order of fA for a-Si TFTs)

flows from TFT drain to source and decreases the charge on C_{PIXEL} . Choosing an optimal TFT OFF voltage can reduce the leakage current.

An a-Se photoconductor based PPS pixel with associated parasitic capacitances is shown in Figure 4 below [37]. Both, a large sensor bias and an additional capacitance, C_{st} , between the node V_x and ground are required for a-Se based x-ray detection technology. These requirements stem from the large a-Se film thickness (0.2 to 1 mm) necessary for detecting x-rays. The large sensor thickness reduces the sensor capacitance and a larger detector bias (in kV) is necessary in order to have a sufficiently strong electric field across the sensor for charge collection.

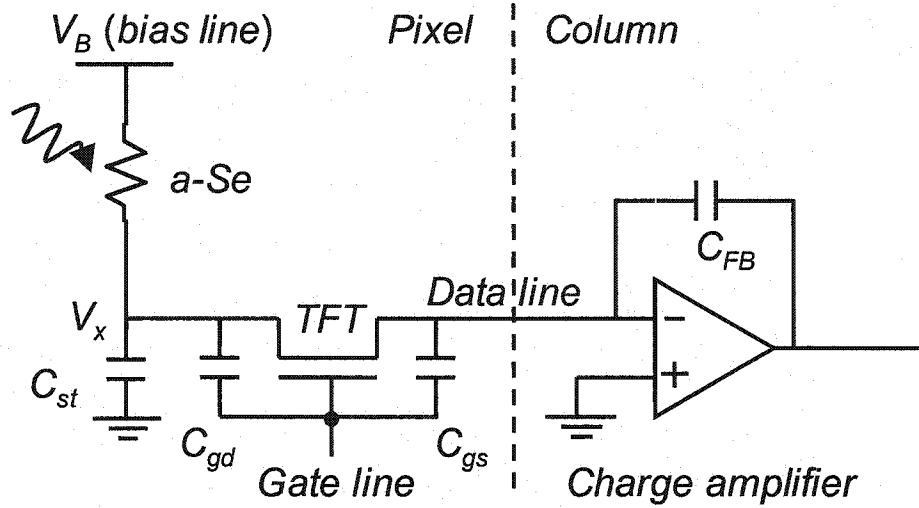


Figure 4. Analysis model for PPS architecture.

One shortcoming of the thick a-Se film and the consequently small a-Se sensor capacitance and higher detector bias is that a large voltage can build up on the integration node, V_x as the x-ray input photons generate signal electrons. Since V_x is connected to the TFT drain, a large voltage can cause TFT breakdown. For very small sensor capacitances (such as tens of fF), the voltage can become fatal to the TFT even at low intensity inputs. Thus, an additional capacitance, C_{st} of about 1 pF, is usually designed into the pixel at the charge detection node in order to prevent the V_x voltage from rising up to a value fatal to TFT operation. Since C_{st} comprises the majority of capacitance at the integration node, the pixel capacitance, $C_{PIX} \sim C_{st}$.

The output voltage on the charge amplifier is obtained directly from the charge (Q_P) accumulated on C_{PIX} as,

$$V_{OUT} = \frac{Q_P}{C_{FB}}. \quad (1)$$

Here, C_{FB} is the integrator's feedback capacitance. If C_{FB} equal to C_{PIX} , V_{OUT} equals V_x .

2.1.3 Charge sensing or voltage sensing?

With a PPS architecture, either charge can be read out or a voltage can be sensed. From past studies done in literature [40], voltage-sensitive amplifiers shown in the figure below are not suited for very small input signals such as the ones encountered in diagnostic medical x-ray imaging applications. In the voltage amplifier configuration, the signal charge from C_{PIX} is transferred to the data line capacitance, C_{LINE} at the input of the amplifier creating a tradeoff between the charge sensitivity of the amplifier and the charge transfer efficiency (CTE) from C_{PIX} to C_{LINE} .

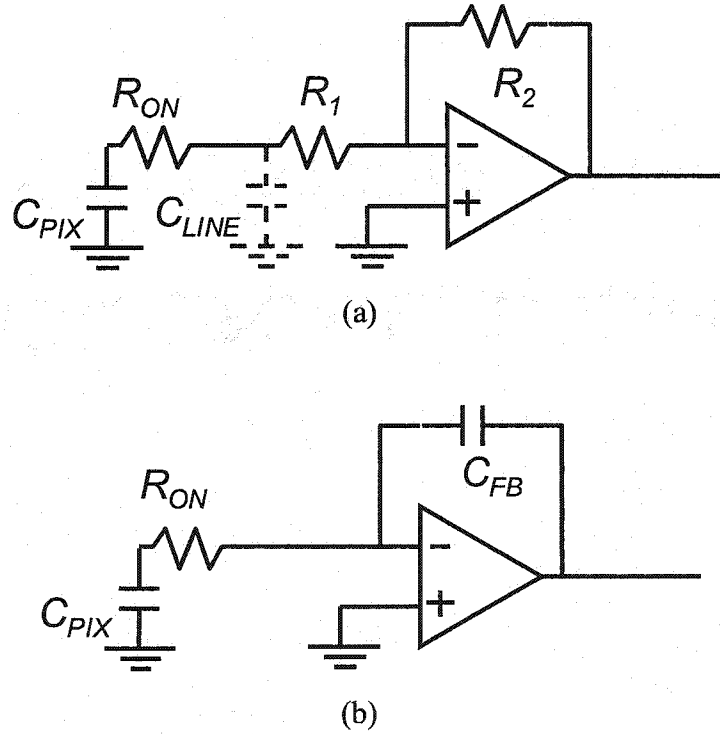


Figure 5. (a) voltage and (b) charge sensing amplifiers

If the C_{LINE} is small compared to C_{PIX} , then insufficient charge, Q_{LINE} , will be transferred from C_{PIX} to C_{LINE} and the CTE will be degraded.

$$Q_{LINE} = Q_P \times \left[\frac{C_{LINE}}{C_{LINE} + C_{PIX}} \right] \quad (2)$$

From the above eqn. (2), to move half of Q_P onto C_{LINE} , C_{LINE} must be equal to C_{PIX} . Thus, $C_{LINE} \gg C_{PIX}$ is needed for almost complete charge transfer. Conversely, if C_{LINE} is large, most of Q_P will be transferred but the voltage, V_{LINE} , developed at the input of the amplifier will be smaller than V_x since C_{LINE} needs to be at least 10 times greater than C_{PIX} for good CTE and hence, charge sensitivity is degraded. A better solution is to connect the integrator directly to the pixel output in order to collect the entire signal charge on the integrator's feedback capacitor as is implemented in current PPS architectures.

2.1.4 Gain and linearity

Since the passive pixel readout circuit is a simple switch, it does not provide any inherent gain to the signal on the charge detection node. However, voltage gain can be achieved by using a charge amplifier with a C_{FB} less than the C_{PIX} although there is a corresponding increase in noise too. Also, as long as the sensing element behaves linearly, the pixel output is linear.

2.1.5 Readout rate

During image readout, the pixel is discharged exponentially with a time constant τ_{ON} given by:

$$\tau_{ON} = R_{ON} C_{PIX}, \quad (3)$$

where R_{ON} is the ON resistance of the switching TFT and C_{PIX} is the pixel capacitance. R_{ON} can be approximated by the following equation for $V_{DS} \ll V_{GS} - V_T$,

$$R_{ON} = \left[\frac{W}{L} \mu_{EFF} C_G (V_{ON} - V_T) \right]^{-1}, \quad (4)$$

Here μ_{EFF} is the effective carrier mobility, V_{ON} is the TFT ON voltage, V_T is the threshold voltage and C_G is the gate capacitance per unit area of the TFT. For a $W/L = 160/20$, $\mu_{EFF} =$

$0.5 \text{ cm}^2/\text{V.s}$, $V_{ON} = 12 \text{ V}$, $V_T = 2 \text{ V}$, and $C_G = 25 \text{ nF/cm}^2$, $R_{ON} \sim 1.1 \text{ M}\Omega$. Next, the intrinsic photo-detector capacitance, C_{a-Se} is given as,

$$C_{a-Se} = \frac{(\epsilon_0 \times \epsilon_{a-Se} \times A_{PD})}{t_{a-Se}}, \quad (5)$$

For $\epsilon_0 = 8.85 \times 10^{-12} \text{ F/m}$, $\epsilon_{a-Si:H} = 6.5$, $A_{PD} = 250 \times 250 \mu\text{m}^2$, $d_{a-Se} = 500 \mu\text{m}$, C_{a-Se} is around 7 fF. Hence, $C_{PIX} \sim C_{st} = 1 \text{ pF}$ as noted previously where the TFT parasitic capacitances have been neglected for now.

τ_{ON} can then be calculated to be $1.1 \mu\text{s}$. For complete charge readout (95% - 99.3%), about 3-5 time constants are usually sufficient which gives a total pixel readout time of $5.5 \mu\text{s}$ (for 5 time constants). The result implies that for a PPS based 1000×1000 x-ray imaging array with column parallel readout, a frame rate of 181 frames/second can be achieved, which is sufficient for real-time operation (30 frames/second).

2.2 Voltage Mediated Active Pixel Sensor

2.2.1 Introduction

One of the reasons for the popularity of the voltage mediated APS in recent CMOS image sensors [44] is that a stable output voltage is formed on the column load resistance in the absence of an off-chip voltage or charge amplifier. For a densely integrated technology like sub-micron CMOS, this output voltage can be easily manipulated with on-chip signal processing giving rise to monolithic circuit systems e.g. single chip cameras.

Even for a technology like a-Si that has comparatively larger minimum dimensions, the V-APS can potentially provide the benefit of direct integration with an on-chip multiplexer to reduce the off-chip amplifier count and hence, off-panel circuit complexity. This is in contrast to the PPS, where the multiplexing can degrade the x-ray signal related small pixel output considerably.

2.2.2 Operation

Central to the voltage mediated APS (V-APS) illustrated in Figure 6 is a source follower circuit, which produces an output current that is converted to a voltage by a resistive load.

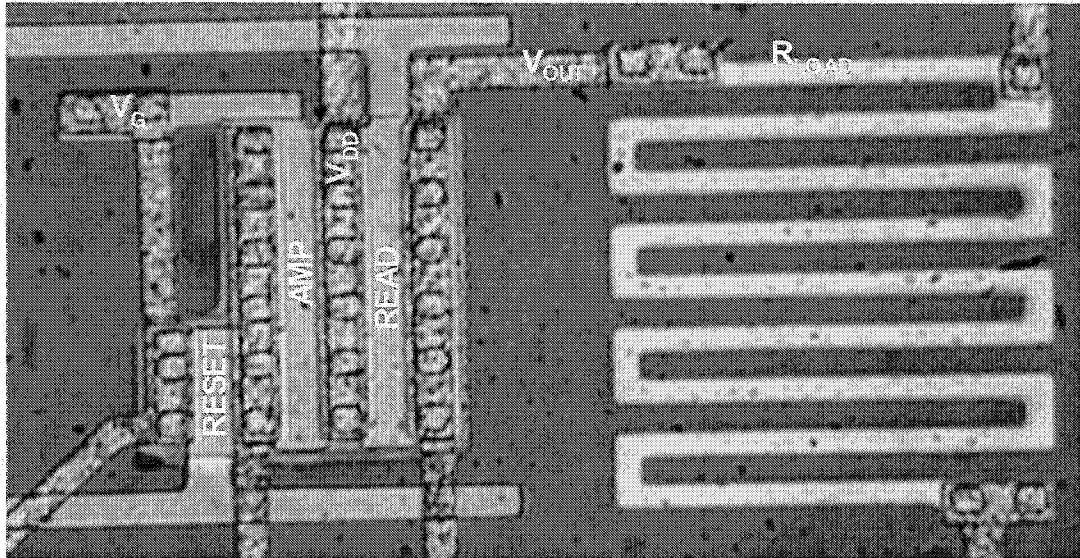
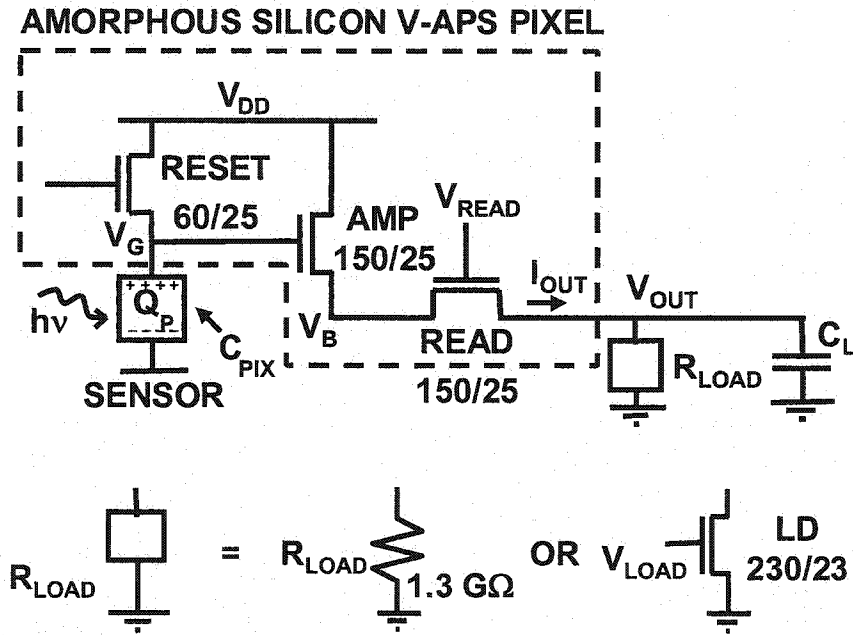


Figure 6. V-APS schematic and associated a-Si circuit micrograph. Here, the n+ a-Si film resistor acts as a column load resistance.

The V-APS circuit operates in three modes:

- Reset: The RESET TFT is switched ON and the pixel capacitance, C_{PIX} charges up to Q_P through this TFT's ON resistance, R_{ON_RESET} .
- Integration: After reset, the RESET TFT is switched OFF for an integration period, T_{INT} . During T_{INT} , the x-ray input signal, $h\nu$, generates photo-carriers discharging C_{PIX} by ΔQ_P decreasing V_G .
- Readout: After integration, the READ TFT is switched ON for a sampling time T_S where a load resistance (arising from a TFT in saturation or a physical resistor) converts the output current into a voltage.

2.2.3 Load Resistance

In CMOS digital imaging, it is common to provide the load resistance using a transistor operating in saturation, i.e. as an active load. This is done to obtain the benefits of both a large resistance as well as current sink like behavior for fast transient responses. The load transistor, with a gate bias of V_{LOAD} , is designed to operate in the saturation regime (i.e. $V_{OUT} \geq V_{LOAD} - V_T$) since its channel resistance stays relatively constant and is insensitive to any variations in V_{OUT} . V_{OUT} is the voltage that appears across the drain and source of the load transistor. A V_{OUT} insensitive load is necessary for linearity as will be shown in the following section. The channel resistance of a TFT operated in the linear region is dependent on V_{OUT} which implies non-linear V-APS operation.

For the a-Si V-APS, both an active load TFT and a large physical column resistor are implemented for comparison purposes. While active loads are superior in terms of resistance and current sinking ability to physical resistors, they require a constant gate bias. Constant gate bias stress is not feasible for a-Si TFTs due to their inherent metastability, discussed in a later chapter, that causes the threshold voltage (V_T) to change sizably even in a few hours. In contrast, physical resistors implemented in an n^+ a-Si film exhibit much better stability over the long term [50].

2.2.4 Linearity and Gain

While simulations are useful for design optimization, it is insightful to use simple MOS Level 1 model equations to predict the V-APS performance trends for initial development. Referring to Figure 6, the large signal expression below relates the V-APS readout circuit intermediate node voltage, V_B to the input, V_G . Here, the drain current of the saturated AMP TFT during V-APS readout has been set equal to the current through R_D , defined as the sum of the READ switch ON resistance, R_{ON_READ} (approximated as a constant) and R_{LOAD} ,

$$V_B = \frac{K_{AMP}}{2} (V_G - V_B - V_T)^2 R_D, \quad (6)$$

where K_{AMP} denotes the usual product of parameters, $(\mu_{EFF} C_G W/L)$. Solving eqn. (6) and differentiating V_B with respect to V_G yields,

$$\frac{\Delta V_B}{\Delta V_G} = 1 - \frac{1}{(1 + 2K_{AMP} R_D (V_G - V_T))^{1/2}}. \quad (7)$$

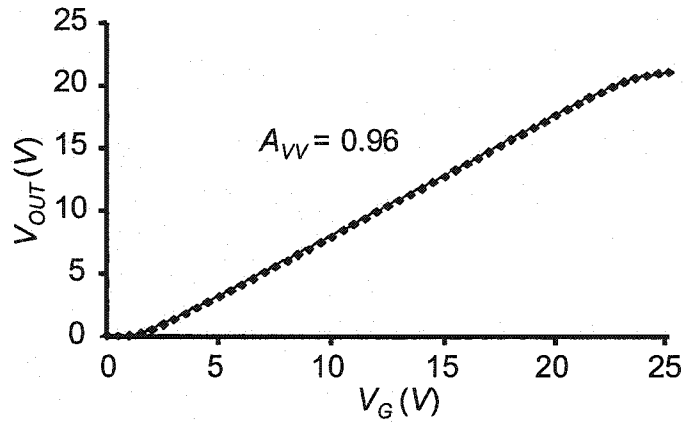
From eqn. (7), the large signal voltage gain of the AMP TFT source follower approaches unity for a large $(K_{AMP} R_D)$ product and $V_G > V_T$. In addition, a constant value for eqn. (7) implies linearity and a large $(K_{AMP} R_D)$ product minimizes gain variations for different values of the input, V_G . Lastly, the voltage divider formed between R_{ON_READ} and R_{LOAD} , causes an additional linear drop in gain so the overall V-APS voltage gain, A_{VV} becomes,

$$A_{VV} = \frac{\Delta V_{OUT}}{\Delta V_B} \cdot \frac{\Delta V_B}{\Delta V_G} = \frac{\Delta V_{OUT}}{\Delta V_G} \approx \frac{R_{LOAD}}{R_{LOAD} + R_{ON_READ}} \left(1 - \frac{1}{(1 + 2K_{AMP} R_D (V_G - V_T))^{1/2}} \right). \quad (8)$$

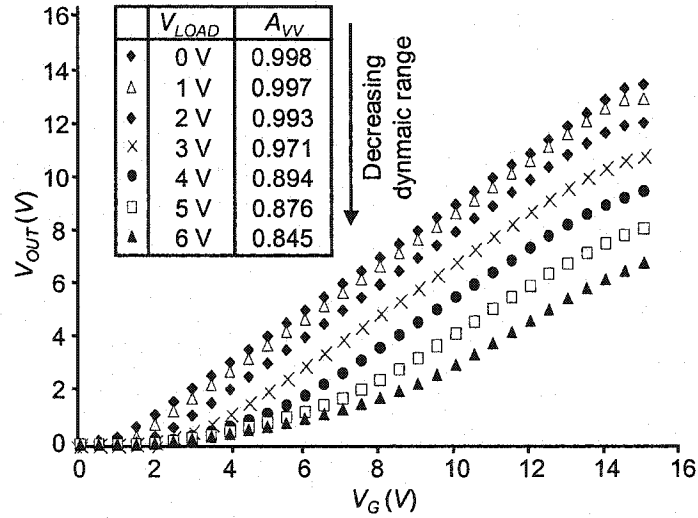
In general, R_{LOAD} is designed to be much larger than R_{ON_READ} so the drop in gain is minimal. For an active load V-APS, the gain and linearity conditions are met since R_{LOAD} (given by the ON resistance of the load TFT in saturation in this case) is much larger than the linear READ TFT switch ON resistance. It is impractical to design the load TFT to be linear at equilibrium since the channel resistance is small and sensitive to V_{OUT} . In contrast, a saturated load TFT gives a large channel output resistance that is independent of V_{OUT} to a first order approximation. Note that channel length modulation can introduce some non-linearity in the APS but it is a second order effect.

The V-APS test pixel, consisting of an integrated a-Si amplifier circuit in a $250 \times 250 \mu\text{m}^2$ pixel area was fabricated in-house and is shown in Figure 6. Large signal linearity

measurements of the V-APS with a $1.3 \text{ G}\Omega$ resistor are shown in Figure 7(a) where the large R_{LOAD} gives an almost ideal gain, $A_{VV} = 0.96$ in the linear region of the curve. Here, Keithley Model 236 SMUs are used to supply and measure the input and output voltages, respectively. The measured data matches simulations using a previously developed in-house a-Si TFT model to within 5%. In Figure 7(a), V_{OUT} levels off at lower voltages (around V_T) due to the AMP TFT not turning on. At higher voltages, V_{OUT} levels off at $(V_{DD} - V_T)$ as V_G approaches the supply voltage, V_{DD} .



(a)



(b)

Figure 7. Gain and linearity results for V-APS with (a) load resistor ($V_{DD} = 25 \text{ V}$) and (b) TFT active load ($V_{DD} = 15 \text{ V}$)

For the V-APS with an active load, the load TFT gate voltage was varied and the result is plotted in Figure 7(b). For very small V_{LOAD} values, the load TFT is barely ON so the output behaves as in the case of a $1.3 \text{ G}\Omega$ resistor. As V_{LOAD} is increased, V_{OUT} becomes more non-linear at lower voltages since the load TFT stays in the ohmic region for a longer duration. Hence, for wide dynamic range, V_{LOAD} must be kept small so that the load TFT enters saturation at a lower V_G .

2.2.5 Readout Time

Large area medical imaging applications such as mammography have been reported to require imaging arrays with 3600×4800 pixels and a maximum readout time of 2-5 seconds per frame [5]. The readout time requirements arise from the sensor dark current degrading the integrated signal charge stored on each pixel's C_{PIX} over time. These requirements pose a challenge to the a-Si V-APS since TFTs have large resistances (in $M\Omega$) and large area arrays have big column bus capacitances.

The array column bus capacitance (C_{LINE}) of the traditional PPS switch based arrays comprises primarily of the sum of the gate to source capacitances (C_{GS}) of the pixel readout TFTs connected to a particular column in addition to the gate/data line overlap capacitances. C_{LINE} usually ranges from 10 pF to 100 pF for typical large area PPS imaging arrays. In contrast, C_{LINE} is estimated to be about 2-3 times larger for APS arrays in the same a-Si technology since the additional bias lines cause an increase in interconnect overlap capacitance.

2.2.5.1 Rise time estimation

The V-APS readout time consists of a rise and fall time component. To estimate the V-APS rise time, t_{rise} , KCL equations at node B and V_{OUT} yield a second order non-linear differential equation, which can be numerically solved using a circuit simulator (e.g. Hspice). However, a simplified form of the equation can be obtained to provide insight into the circuit by neglecting the READ TFT altogether during readout. For a resistor load, the sum of currents at the V_{OUT} node (READ TFT omitted) can be written as,

$$K'_{AMP}(V_G - V_{OUT} - V_T)^2 = \frac{V_{OUT}}{R_{LOAD}} + C_{LINE} \frac{dV_{OUT}}{dt}, \quad (9)$$

where $K'_{AMP} = (\mu_{EFF} C_G W_{AMP} / 2L)$ and R_{LOAD} is the column load resistor. The above eqn. can be rearranged as,

$$\int dt = \int \left[\frac{C_{LINE}}{K'_{AMP}(V_G - V_{OUT} - V_T)^2 - \frac{V_{OUT}}{R_{LOAD}}} \right] dV_{OUT}. \quad (10)$$

The first boundary conditions for eqn. (10) is at $V_{OUT} = 0$ V where readout begins. The second boundary condition comes from the V_{OUT} value when readout is complete. Here, the current through R_{LOAD} and the saturated AMP TFT must be set equal at equilibrium,

$$V_{OUT} = \frac{2K'_{AMP}R_{LOAD}(V_G - V_T) + 1 - \sqrt{4K'_{AMP}R_{LOAD}(V_G - V_T)}}{2K'_{AMP}R_{LOAD}} \quad (11)$$

The V_{OUT} value can be estimated by simplifying eqn. (11) as,

$$V_{OUT} = (V_G - V_T) - \sqrt{\frac{(V_G - V_T)}{K'_{AMP}R_{LOAD}}} \quad (12)$$

Using the boundary condition described above to solve eqn. (10),

$$t_{rise} = \frac{2R_{LOAD}C_{LINE}}{\sqrt{4K'_{AMP}R_{LOAD}(V_G - V_T)} - 1} \left(\tan^{-1} \left(\frac{2K'_{AMP}R_{LOAD}(V_G - V_T) - 1}{\sqrt{4K'_{AMP}R_{LOAD}(V_G - V_T)} - 1} \right) - \tan^{-1} \left(\frac{2K'_{AMP}R_{LOAD} \sqrt{\frac{V_G - V_T}{K'_{AMP}R_{LOAD}}} - 1}{\sqrt{4K'_{AMP}R_{LOAD}(V_G - V_T)} - 1} \right) \right) \quad (13)$$

For example, choosing the AMP TFT for large drive current and minimizing the load capacitance, C_{LINE} , will reduce t_{rise} , which is also intuitive. Choosing a large R_{LOAD} can be beneficial since most of the AMP TFT current goes into charging C_{LINE} . However, a smaller R_{LOAD} decreases the equilibrium value of V_{OUT} as defined in eqn. (12), and hence dynamic range drops. The reduced dynamic range causes the AMP TFT to charge C_{LINE} up to a lower V_{OUT} , which consequently speeds up t_{rise} .

Much like the load resistor, the sum of currents at the V_{OUT} node for an active load can be written as,

$$K'_{AMP}(V_G - V_{OUT} - V_T)^2 = I_{LOAD} + C_{LINE} \frac{dV_{OUT}}{dt}, \quad (14)$$

where $K'_{AMP} = (\mu_{EFF}C_G W_{AMP}/2L)$ and I_{LOAD} is the current in the load TFT. The analysis is complicated somewhat because the load TFT swings through the linear mode before it reaches saturation. Thus, two first order ordinary differential equations (ODE) have to be solved: one when the load TFT is in linear and the other when it is in saturation. For the linear mode estimation, the equation shown below is used,

$$I_{LOAD_LIN} = \frac{K_{LOAD}}{2} (2(V_{LOAD} - V_T)V_{OUT} - V_{OUT}^2) \quad (15)$$

However, the result is quite cumbersome. Averaging the V_{OUT}^2 term with $V_{OUT} = \frac{1}{2}(V_{LOAD} - V_T)$ simplifies the situation considerably by reducing eqn. (15) to a linear ordinary differential equation. Then, the t_{rise} for the V-APS with a load TFT in the linear mode becomes,

$$t_{rise_lin} = \frac{-C_{LINE} \cdot \ln \left(\frac{1}{2} K_{AMP} (V_G - V_T)^2 + \frac{1}{2} K_{LOAD} \left(\frac{1}{2} V_{LOAD} - \frac{1}{2} V_T \right)^2 - \frac{1}{2} K_{LOAD} (2V_{LOAD} - 2V_T) V_{OUT} \right)}{K_{LOAD} (V_{LOAD} - V_T)} \quad (16)$$

where $K_{AMP} = (\mu_{EFF}C_G W_{AMP}/L)$ and $K_{LOAD} = (\mu_{EFF}C_G W_{LOAD}/L)$. The two boundary conditions for eqn. (8) are simply, $V_{OUT} = 0$ initially and increases until $V_{OUT} = V_{LOAD} - V_T$ where the load TFT leaves saturation. Substituting these in eqn. (16),

$$t_{rise_lin} = \frac{-C_{LINE}}{K_{LOAD} (V_{LOAD} - V_T)} \ln \left(1 - \frac{2K_{LOAD} (V_{LOAD} - V_T)^2}{K_{AMP} (V_G - V_T)^2 + \frac{K_{LOAD}}{4} (V_{LOAD} - V_T)^2} \right) \quad (17)$$

Note that the logarithmic term in eqn. (17) is going to be less than unity (and hence negative) and the closer it is to unity, the smaller it is and the faster the rise time. So, from eqn. (17), if the AMP TFT is designed to source much more current than the load TFT can sink, then C_{LINE} should charge up in lesser time. To obtain the second part of t_{rise} , the following equation is used for the saturated load TFT.

$$I_{LOAD_SAT} = \frac{K_{LOAD}}{2} (V_{LOAD} - V_T)^2. \quad (18)$$

Note that eqn. (18) is not dependent on the value of V_{OUT} since the transistor is in saturation. The solution to eqn. (14) is of the form,

$$t_{rise_sat} = \frac{C_{LINE}}{\sqrt{K'_{AMP} I_{LOAD_SAT}}} \tanh^{-1} \left[\frac{K'_{AMP}}{\sqrt{K'_{AMP} I_{LOAD_SAT}}} (V_G - V_{OUT} - V_T) \right] + const, \quad (19)$$

The first boundary condition on eqn. (19) is defined at the initial value of V_{OUT} where the TFT enters saturation: $V_{OUT} = V_{LOAD} - V_T$. The final boundary condition is given by the steady state value of V_{OUT} . This is estimated by noting at equilibrium, the current through the AMP TFT, I_{AMP} must equal I_{LOAD} . Equating the saturation currents of the two TFTs,

$$K'_{AMP}(V_G - V_{OUT} - V_T)^2 = K'_{LOAD}(V_{LOAD} - V_T)^2. \quad (20)$$

Solving eqn. (20) for V_{OUT} gives,

$$V_{OUT} = V_G - V_T - \sqrt{\frac{K'_{LOAD}}{K'_{AMP}}}(V_{LOAD} - V_T). \quad (21)$$

Eqn. (10) can be simplified for the second boundary condition as,

$$t_{rise_sat} = \int_{V_{LOAD}-V_T}^{V_G-V_T-\sqrt{\frac{K'_{LOAD}}{K'_{AMP}}}(V_{LOAD}-V_T)} \frac{C_{LINE}}{\left[\frac{K_{AMP}}{2} (V_G - V_{OUT} - V_T)^2 - I_{LOAD} \right]} dV_{OUT} \quad (22)$$

$$t_{rise_sat} = \frac{\sqrt{2}C_{LINE}}{\sqrt{K_{AMP}I_{LOAD_SAT}}} \left[\tanh^{-1} \left[\frac{\sqrt{2}K'_{AMP}(V_G - V_{LOAD})}{\sqrt{K_{AMP}I_{LOAD_SAT}}} \right] - \tanh^{-1} \left[\frac{\sqrt{2}K'_{AMP}(V_{LOAD} - V_T)\sqrt{K_{LOAD}/I_{LOAD}}}{\sqrt{K_{AMP}I_{LOAD_SAT}}} \right] \right] \quad (23)$$

To speed up the saturation component of t_{rise} , a large load TFT and AMP TFT may be used while maintaining a large V_{LOAD} bias. In general for a fast t_{rise} , C_{LINE} should be minimized and the current driving ability of the AMP TFT should be maximized. Note that if V_{LOAD} and K_{LOAD} are made large, the load TFT ON resistance decreases and the dynamic range of the APS suffers along with the linearity and gain from eqn. (8). The optimal values of the AMP and load TFT aspect ratios and biasing are determined through simulation. In contrast, the load resistor based V-APS does not have the same design flexibility where a smaller R_{LOAD} gives a faster rise time but trades off dynamic range, linearity and gain.

2.2.5.2 Fall time estimation

For the V-APS fall time, t_{fall} , the situation is considerably simpler since the READ TFT is turned OFF disabling the AMP TFT too. As before, the active load TFT initially behaves as a constant current source discharging the V_{OUT} node until it enters the linear region of

operation (at $V_{OUT} = V_{LOAD} - V_T$) where it approximates the discharging of a single RC time constant circuit.

In saturation mode, the discharge time depends on the V_{OUT} value present on the output node. The worst case for the discharge time during saturation can be written, noting eqn. (21) represents the voltage at the beginning of the discharge cycle and $(V_{LOAD} - V_T)$ is where the load TFT leaves saturation,

$$t_{fall_sat} = \frac{\Delta V \cdot C_{LINE}}{I_{LOAD_SAT}} = \frac{\left(V_G - V_{LOAD} - \sqrt{\frac{K'_{LOAD}}{K'_{AMP}}} (V_{LOAD} - V_T) \right) \cdot C_{LINE}}{I_{LOAD_SAT}}, \quad (24)$$

where I_{LOAD_SAT} is a constant defined in eqn. (18).

For the second component of fall time where the load TFT is in linear mode, the differential equation can be written as,

$$t_{fall_lin} = \int_{V_{LOAD}-V_T}^{V_{final}} \frac{C_{LINE}}{K'_{LOAD} (2(V_{LOAD} - V_T)V_{OUT} - V_{OUT}^2)} dV_{OUT} \quad (25)$$

where eqn. (15) has been used to represent the load TFT current in the linear mode. V_{final} simply represents the value when the V_{OUT} node is effectively discharged (usually to 1% or less of its initial value). Eqn. (25) can be consequently solved as,

$$t_{fall_lin} = \frac{C_{LINE}}{2K'_{LOAD} (V_{LOAD} - V_T)} \ln \left(\frac{(2V_{LOAD} - V_T - V_{final})}{(V_{final})} \right) \quad (26)$$

Thus, the total fall time can be written as,

$$t_{fall} = \frac{\left(V_G - V_{LOAD} - \sqrt{\frac{K'_{LOAD}}{K'_{AMP}}} (V_{LOAD} - V_T) \right) \cdot C_{LINE}}{I_{LOAD_SAT}} + \frac{C_{LINE}}{2K'_{LOAD} (V_{LOAD} - V_T)} \ln \left(\frac{(2V_{LOAD} - V_T - V_{final})}{(V_{final})} \right), \quad (27)$$

For the n^+ a-Si film resistor, R_{LOAD} , t_{fall} is simply given by noting that C_{LINE} and R_{LOAD} form an RC pair which would require about five time constants to discharge almost completely,

$$t_{fall} = 5R_{LOAD}C_{LINE}. \quad (28)$$

Depending on the value of R_{LOAD} , t_{fall} can be several times larger than t_{rise} . In general, R_{LOAD} is made large for high gain, linearity and dynamic range but this has the adverse effect of increasing the t_{fall} drastically.

2.2.5.3 Design Summary

Using the derived equations in the previous section, some general design strategies are highlighted in the table below.

Table 2. Design constraint summary

	Design Conditions
Gain	$K_{AMP} R_{LOAD} (V_G - V_T) \gg 1, R_{LOAD} \gg R_{ON_READ}$
Linearity	$K_{AMP} R_{LOAD} (V_G - V_T) \gg 1, R_{LOAD} \gg R_{ON_READ}$
t_{rise}	Maximize $K_{LOAD} (V_{LOAD} - V_T), I_{AMP} \gg I_{LOAD}$
t_{fall}	Maximize I_{LOAD} , minimize $V_{OUT(max)}$

From the above table, there are some tradeoffs in designing the V-APS for fast operation, unity gain and linearity. Assuming the READ TFT switch is biased and designed to give the lowest possible ON resistance, the conditions above can be translated into circuit design parameters as,

Table 3. TFT and biasing parameter tradeoffs

	$(W/L)_{AMP}$	V_G	$(W/L)_{LOAD}$	V_{LOAD}
Gain	<i>large</i>	<i>large</i>	<i>small</i>	<i>small</i>
Linearity	<i>large</i>	<i>large</i>	<i>small</i>	<i>small</i>
t_{rise}	<i>large</i>	<i>large</i>	<i>large</i>	<i>small</i>
t_{fall}	<i>small</i>	<i>small</i>	<i>large</i>	<i>large</i>

Intuitively, having a large load TFT ON-resistance improves gain and linearity since most of the output voltage drops across the load TFT. Have a smaller load TFT ON current, improves the output rise time since most of the AMP TFT current charges up C_{LINE} . Unfortunately, both smaller ON currents and larger ON resistances for the load TFT serve to increase the output fall time. In general, a compromise can be attained by using a large AMP TFT with a moderate V_G bias balanced by a large load TFT with a small V_{LOAD} . The

moderate V_G bias is obtained by reducing the power supply voltage and serves to reduce the maximum output voltage, $V_{OUT(max)}$. Since the saturated AMP TFT current source charges the output node and the load TFT current source is responsible for discharging the output node, reducing $V_{OUT(max)}$ is a particularly effective method of improving t_{rise} and t_{fall} . Thus, dynamic range is traded off for faster rise and fall times while the gain and linearity are not compromised.

2.2.5.4 Measurements

The measurement setup for readout time tests performed on the V-APS is shown in Figure 8. Here, a Burr-Brown instrumentation amplifier INA116 was connected in a unity gain configuration at the V-APS output node to facilitate transient measurements of V_{OUT} . The unity gain opamp buffer eliminated the loading effect of the 1.3 G Ω resistor and the load TFT on the oscilloscope input probe, which was essential for accurate measurement of V_{OUT} . The load capacitance, C_{LINE} , was supplied by the opamp's input capacitance of 7 pF.

For the V-APS with a load resistor, the READ pulse was operated at 10 Hz (100 ms period) to allow for complete measurement of rise and fall times. This is mainly because of slow fall times due to the large load resistor. From Figure 9, it can be seen that $t_{rise} \sim 700 \mu s$ while $t_{fall} \sim 50 \text{ ms}$. Both measurements agree with Cadence simulations to within 5%. In addition, t_{fall} can also be estimated from eqn. (28) as being 45.5 ms.

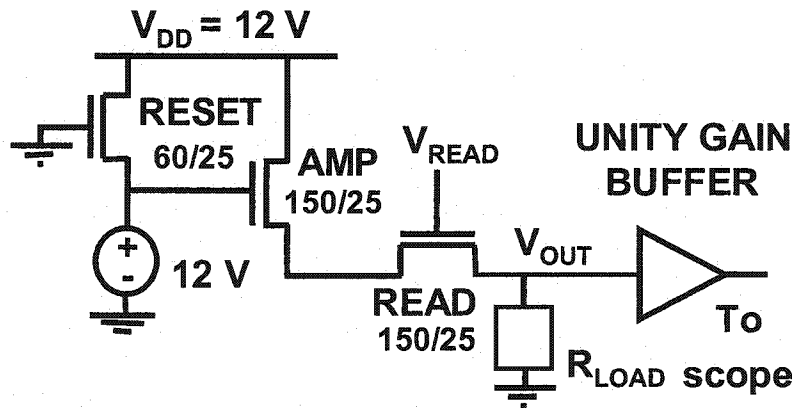
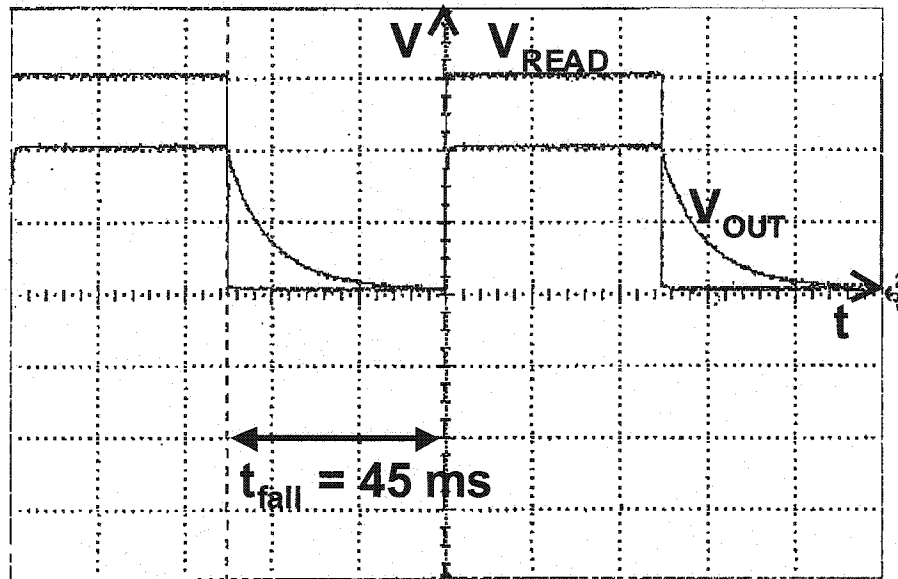


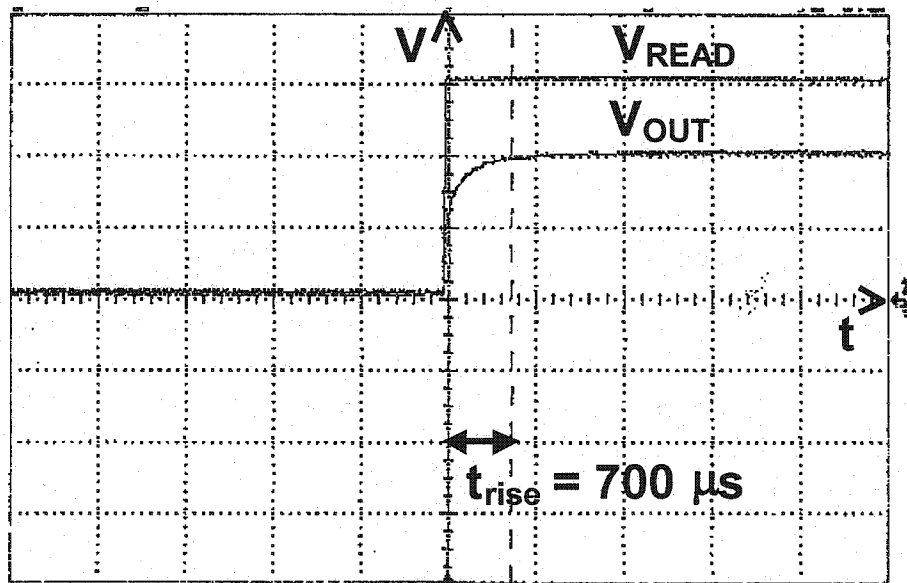
Figure 8. V-APS transient performance measurement setup ($V_G = 12 \text{ V}$, $V_{READ} = 15 \text{ V}$)

5 V/div 10 Hz READ pulse 20 ms/div



(a)

5 V/div 10 Hz READ pulse 1 ms/div



(b)

Figure 9. Transient response of V-APS (a) fall time for load resistor, (b) rise time for load resistor.

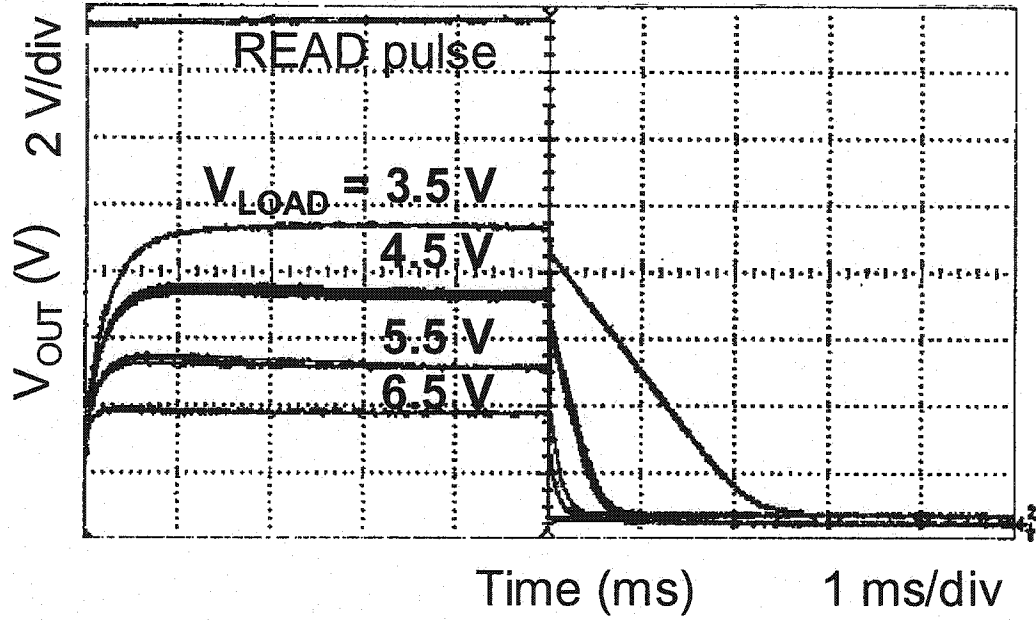


Figure 10. Transient response of V-APS with an active load TFT.

Transient results from the V-APS with a load TFT shown in Figure 10 illustrate the benefits of an active load: faster readout times while maintaining high dynamic range, near unity gain and linearity shown in Figure 7(b).

2.2.6 Discussion

A challenging aspect about the a-Si V-APS circuit seen in the previous section is attaining fast readout times for large area applications. One general method of doing so is by scaling down the TFT process. Scaling can reduce the column capacitance, C_{LINE} by shrinking interconnect overlaps as well as by reducing the size of the READ TFT in each APS pixel, thereby decreasing the overlap capacitance (C_{GS}), a major contributor to C_{LINE} .

For t_{rise} , using a large AMP transistor to provide a big charging current is sufficient. Using the in-house $18\mu\text{m}$ a-Si technology, rise times as little as 0.25 ms were achieved for a V-APS with active load and 0.7 ms for a V-APS with load resistor. These readout times can be lessened by either reducing the supply voltage $V_{DD} = V_G$ or using small load resistances.

Both methods reduce the maximum achievable V_{OUT} and hence, dynamic range. However, this may be acceptable depending on the application the APS is used for.

The primary advantage of using an active load TFT instead of a load resistor is attaining fast fall times without sacrificing linearity or gain. This is mainly because the load TFT is a constant current source discharging V_{OUT} and can be appropriately designed to achieve fast fall times. In addition, the load TFT in saturation provides a very large output resistance that serves to improve the voltage gain.

For comparison, Figure 11 below shows the voltage gain (A_{VV}) and t_{fall} for the fabricated a-Si V-APS plotted against various R_{LOAD} values. As evident, A_{VV} falls off sharply as R_{LOAD} decreases below a certain threshold ($K_{AMP} R_{LOAD} \gg 1$). The fall time has a linear dependence on R_{LOAD} since the READ TFT switch effectively disconnects the output node from the remainder of the circuit.

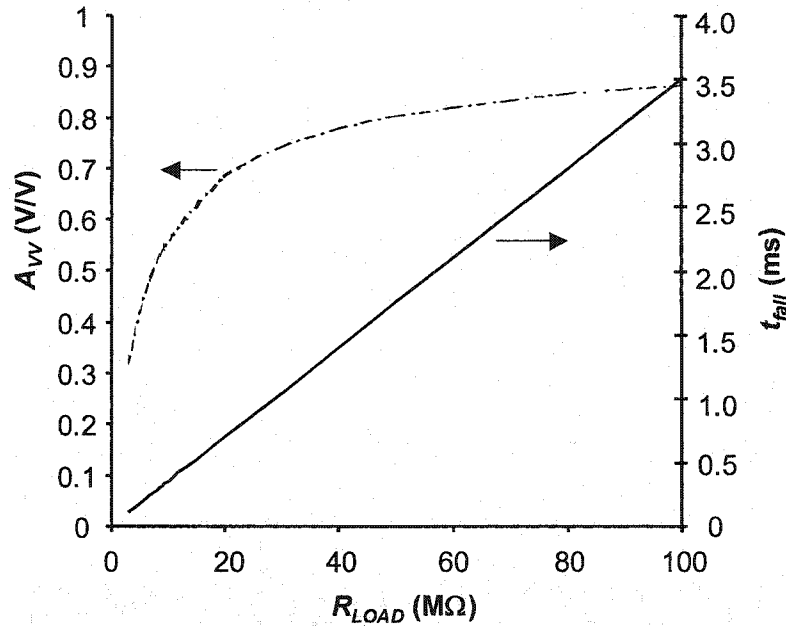


Figure 11. Theoretical gain and fall time tradeoffs for a V-APS with load resistor

In contrast, for a V-APS with active load, the gain is maintained even for small fall times. This is shown in Figure 12 below where data from the active load V-APS gain and transient curves has been plotted.

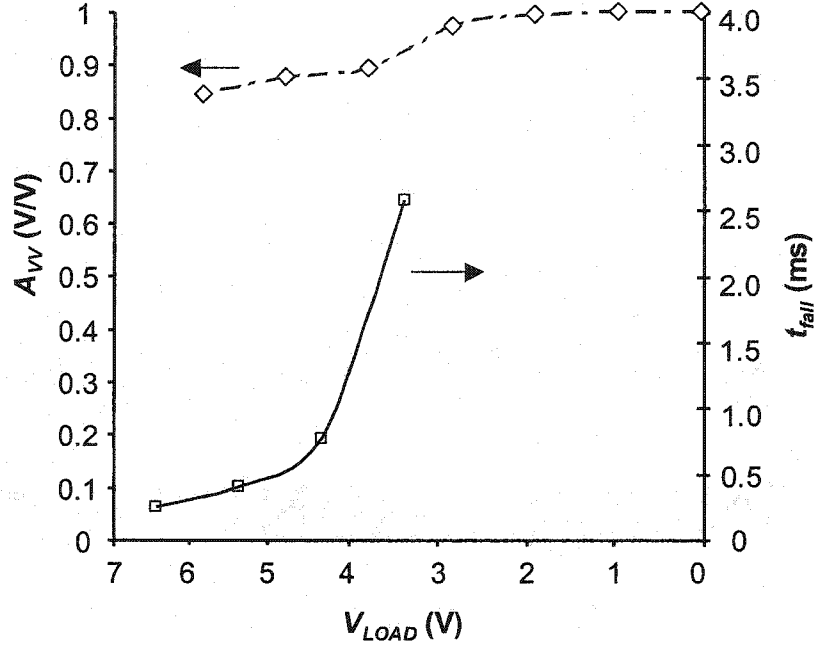


Figure 12. Measured gain and fall time tradeoff for a V-APS with active load.

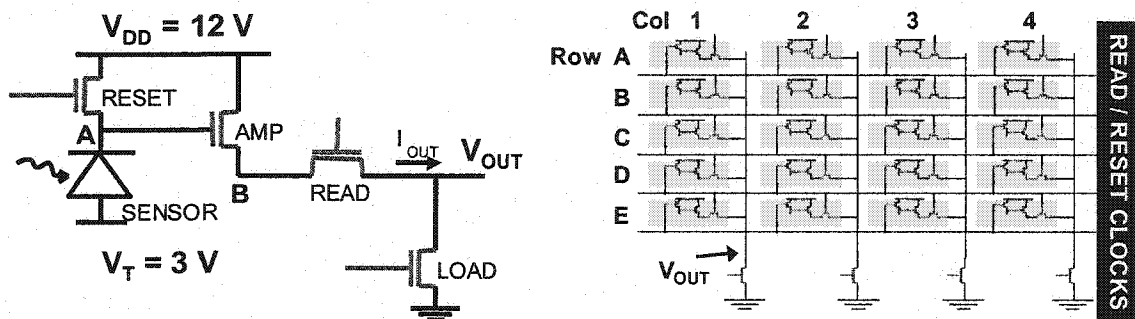
The main benefit of using an n^+ a-Si film resistor over an a-Si load TFT is the resistor's relative immunity to metastability [50]. For the TFT, a continuous V_{LOAD} bias at the gate causes a time dependent shift in the threshold voltage, which serves to (a) reduce the dynamic range by increasing the minimum linear V_{OUT} voltage as well as (b) increasing the fall time by decreasing I_{LOAD} . In contrast, initial stress tests conducted on an n^+ a-Si film resistor [50] for different biases revealed a maximum change in resistance of 6% over 15 hours. These results indicate better stability than a-Si TFTs where the ΔV_T shifts much more over a similar time period.

In a typical mammographic digital imaging array, there are 3600 x 4800 pixels and an x-ray induced signal charge of 1.8×10^4 to 7.2×10^6 electrons. For a nominal 1 pF pixel capacitance, the input signal voltage ranges from 3.84 mV to 1.536 V which implies that a V-APS dynamic range of 2 V is acceptable. Similarly, the dynamic range required for chest radiography is less than 1 V. In calculations of readout time, a column parallel readout architecture (i.e. a row of pixels read out simultaneously) is assumed. Also, V-APS column load resistances are assumed to exist at both ends of the column in order to facilitate readout of two rows simultaneously. Since two rows can be read concurrently, 1800 effective pixel

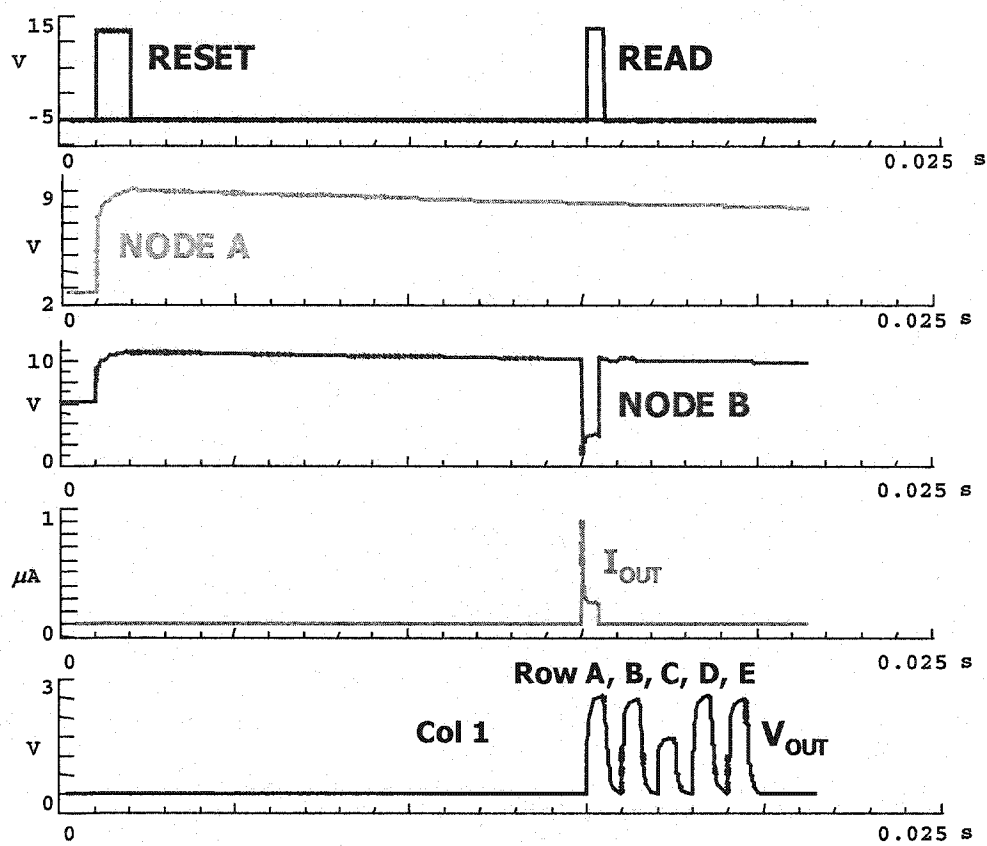
rows need to be read out per frame. For a maximum frame time of 5 seconds, at least 2.77 ms of readout time per row of pixels is available.

For a V-APS array using a state-of-the-art 6 μm a-Si TFT process, C_{LINE} is estimated to be less than 40 pF (where the READ TFT C_{GS} and two bias/data line overlaps were considered for each of the 1800 pixels in each column). Extending the measured results for the active load V-APS, a readout time of 1.4 ms per column of pixels is required. For 1800 pixels, this leads to a frame readout time of 2.5 seconds, which is acceptable for large area mammography or radiography. A sample a-Si V-APS array simulation (in VHDL-AMS) based on the in-house TFT process (with load TFTs at only one end of the column) is shown in Figure 13 where theoretical readout times of 5 ms are achieved per pixel for a 100 pF column capacitance implying a frame readout time of 9 s. Understandably, some process improvements are required.

The primary advantage of the V-APS circuit over traditional PPS circuits is that external charge amplifiers are not required to obtain a readable output voltage. Also, the output is suitable for direct connection to an integrated multiplexer, which can reduce the external bond pad connections and hence, array component count and cost. However, the speed of operation of the V-APS circuit (~ 1 kHz) makes it suitable for static x-ray imaging modalities such as chest radiography or mammography. Details of integrating the V-APS pixel circuit array with a multiplexer are not included in this thesis and the readers are referred to [84][85] for further information. The operation and performance of a-Si V-APS pixels has been published in [50][51][56].



(a)



(b)

Figure 13. Simulation results of a 5 x 4 a-Si V-APS imager.

2.3 Current Mode Active Pixel Sensor

2.3.1 Introduction

While the V-APS offers the advantage of direct integration with an on-panel multiplexer, its implementation in a-Si technology is unsuitable for real time performance posing a challenge to some medical imaging applications such as fluoroscopy. In addition, since the V-APS does not perform input amplification, noise introduced by the external electronics and the additional transistors in the V-APS pixel readout circuit can further corrupt the weak x-ray input of 1000 electrons for fluoroscopy. Hence, it is necessary to modify the pixel readout circuit to one that offers real time readout with some gain to combat noise.

2.3.2 Operation

Central to the current mediated active pixel sensor (APS) illustrated in Figure 14 is a source follower circuit, which produces a current output (C-APS) to drive an external charge amplifier. Much like the V-APS, the C-APS operates in three modes:

- Reset mode: The RESET TFT switch is pulsed ON and C_{PIX} charges up to Q_P through the TFT's on resistance. C_{PIX} is usually dominated by the detector (e.g. a-Se photoconductor or a-Si photodiode detection layer [5]) capacitance.
- Integration mode: After reset, the RESET and READ TFT switches are turned OFF. During the integration period (T_{INT}), the input signal, $h\nu$, generates photo-carriers discharging C_{PIX} by ΔQ_P and decreases the potential on C_{PIX} by a small signal voltage, ΔV_G .
- Readout mode: After integration, the READ TFT switch is turned ON for a sampling time T_S , which connects the APS pixel to the charge amplifier and an output voltage, V_{OUT} , is developed across C_{FB} proportional to $V_G + \Delta V_G$ and T_S .

Operating the READ and RESET TFTs in the linear region reduces the effect of inter-pixel threshold voltage (V_T) non-uniformities. Although the saturated AMP TFT causes the C-APS to suffer from FPN, using CMOS-like off-chip double sampling [44] and offset and gain correction techniques (discussed further in Chapter 6) can alleviate the problem.

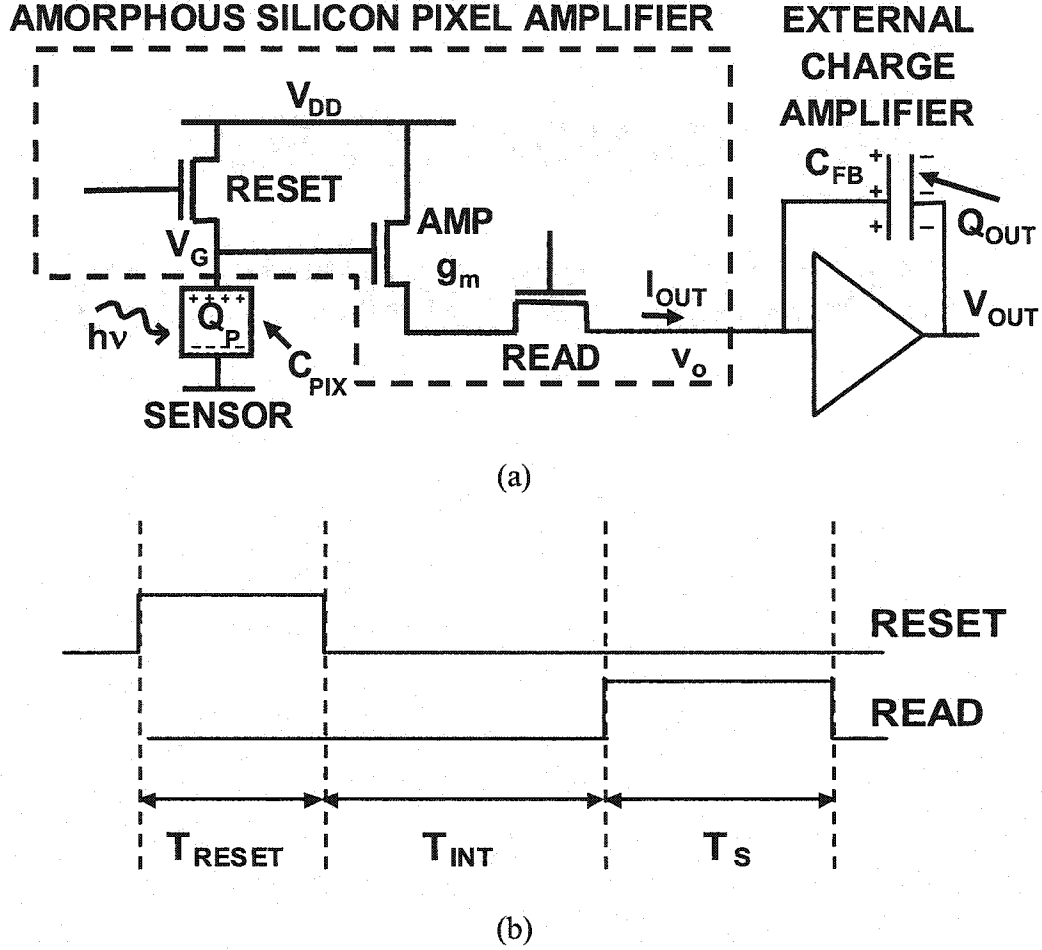


Figure 14. C-APS (a) Readout circuit schematic and (b) Timing diagram

Some observations can be made for the circuit shown in Figure 14. First, there is no load resistance so problems such as gate-bias induced metastability for a load TFT are obviated and the slow rise/fall times due to charging/discharging a load resistance are also eliminated. Secondly, the lower limit on the readout rate is determined by the switching speed of the READ TFT, which is usually around $1 \mu s$ in a-Si technology depending on the TFT size. Also, since the readout circuit outputs a current via a field effect transistor, there is a quadratic relationship between the C-APS input (V_G) and output (I_{OUT}).

2.3.3 Linearity

The linearity of the C-APS readout circuit is obtained from a sensitivity analysis [48] of the change in output current, I_{OUT} , with respect to the input illumination, $h\nu$ in Figure 14,

$$\gamma = \frac{dI_{OUT}}{dh\nu} = \frac{dQ_P}{dh\nu} \frac{dV_G}{dQ_P} \frac{dI_{OUT}}{dV_G}, \quad (29)$$

where γ is a constant for a linear sensor. The first term is linear if the detector gives a linear change in the charge on C_{PIX} , ΔQ_P with changing $h\nu$. The second term is linear if the voltage change ΔV_G across C_{PIX} is linearly dependent on ΔQ_P where,

$$\Delta Q_P = \Delta V_G C_{PIX}, \quad (30)$$

Eqn. (30) is linear provided C_{PIX} stays constant under the changing bias conditions where the TFT parasitic capacitances have been neglected. The last term in eqn. (29) imposes a linear small signal condition on the allowable change in the AMP TFT gate bias, V_G . For a MOS device, the I - V relationship can be written as,

$$I_{OUT} + \Delta I_{OUT} = K/2 (V_G + \Delta V_G - V_T)^2 \quad (31)$$

This can be expanded to,

$$I_{OUT} + \Delta I_{OUT} = (K/2)(V_G - V_T)^2 + K(V_G - V_T)\Delta V_G + (K/2)(\Delta V_G)^2 \quad (32)$$

Separating the dc bias and focusing only on the small signal ac components,

$$\Delta I_{OUT} = K(V_G - V_T)\Delta V_G + (K/2)(\Delta V_G)^2 \quad (33)$$

Here, for linear circuit operation, the $(\Delta V_G)^2$ non-linearity must be minimized giving,

$$\Delta V_G \ll 2(V_G - V_T), \quad (34)$$

For the APS, V_G is the DC bias voltage at the AMP TFT gate and V_T is its threshold voltage. Thus, for linear C-APS operation, the change in voltage at the integration node due to the x-ray input (ΔV_G) must be kept small. The equations above also serve to illustrate that both biasing and signal components exist in the output current. The bias current component (I_{OUT}) comes from the steady state value of the gate voltage (V_G) while the signal current (ΔI_{OUT}) comes from the small signal change at the AMP TFT gate (ΔV_G).

2.3.4 Gain

2.3.4.1 Theory

When photons are incident on the detector, electron-hole pairs are created leading to a change in the charge on the integration node. In small signal operation, the change in the amplifier's output current with respect to a small change in gate voltage, ΔV_G is,

$$\Delta I_{OUT} = g_m \Delta V_G, \quad (35)$$

where g_m is the transconductance of the AMP and READ TFT composite circuit and ΔV_G represents the small signal voltage at the gate of the AMP TFT. Again, simple MOS Level 1 models are used here to obtain insight although more exact results are obtained via simulation using a previously developed a-Si TFT model [46][47]. The composite circuit g_m is obtained by equating the current through the AMP TFT operating in saturation and READ TFT operating in linear as shown in eqn. (36). This is done to derive $V_{DS} = V_B$ across the READ TFT, which then enables the determination of R_{ON} , I_{OUT} , and g_m .

$$(K_{AMP}/2)(V_{GA} - V_B - V_{TA})^2 = (K_{RD}/2)(2(V_{GRD} - V_{TRD})V_B - V_B^2) \quad (36)$$

Here, V_{GA} is the AMP TFT gate voltage, V_{TA} is the AMP TFT threshold voltage, V_{GRD} is the READ TFT gate voltage, V_{TRD} is the read TFT threshold voltage and R_{ON} is the ON resistance of the READ TFT. Solving and extracting the correct root for V_B ,

$$V_B = \frac{\left[K_{AMP}(V_{GA} - V_{TA}) + K_{RD}(V_{GRD} - V_{TRD}) - \left[K_{RD} \left(\frac{-2K_{AMP}V_{GA}(V_{GRD} - V_{TRD} + V_{TA}) + 2K_{RD}V_{GRD}V_{TRD}}{+K_{AMP}(V_{GA}^2 - V_{TA}^2) - K_{RD}(V_{GRD}^2 + V_{TRD}^2)} \right)^{1/2} \right] \right]}{(K_{RD} + K_{AMP})} \quad (37)$$

Given V_B , substituting back into the I_{DS} equation for the AMP or READ TFT gives I_{OUT} in the APS readout circuit branch. Then, dividing V_B by I_{OUT} gives the switch resistance, R_{ON} , for the READ TFT. To quantify some results, Table 4 consists of sample values of APS circuit parameters at different bias values. Note the inherent feedback in the circuit that causes V_B to increase for increasing supply voltage, V_{DD} hence limiting the V_{GS} across the AMP TFT, thereby reducing I_{OUT} and g_m .

Table 4. Sample values of APS circuit parameters for different supply voltages

$$V_{GRD} = 15 \text{ V}, W/L = 150/25, \mu_{EFF} = 0.17 \text{ cm}^2/Vs$$

	$V_{DD} = 6 \text{ V}$	$V_{DD} = 8 \text{ V}$	$V_{DD} = 12 \text{ V}$
$V_B (V)$	0.48	1.0	2.43
$I_{OUT} (\mu A)$	0.23	0.46	0.98
$R_{ON} (M\Omega)$	2.08	2.17	2.47
$g_m (\mu S)$	0.067	0.096	0.145

Particular care must be taken in designing the C-APS to ensure that bias component, I_{OUT} does not saturate the column charge amplifier. For example, if the maximum output voltage that a charge amplifier, with a feedback capacitance of 5 pF , can hold is 15 V , then an I_{OUT} of $2.5 \mu A$ for $30 \mu s$ will saturate the output. Since g_m is related to V_{DD} , charge amplifier saturation for high V_{DD} values limits the maximum achievable g_m . Using eqn. (30) and eqn. (35), the charge gain, G_i , stemming from the drain current modulation is:

$$G_i = |\Delta Q_{OUT}/\Delta Q_P| = (\Delta I_{OUT} \cdot T_S)/\Delta Q_P = (\Delta I_{OUT} \cdot T_S)/(\Delta V_G C_{PIX}) = (g_m T_S)/C_{PIX}. \quad (38)$$

The charge gain amplifies the input signal making it resilient to external noise sources. The corresponding voltage gain can be calculated using eqn. (35) and assuming a constant ΔI_{OUT} . Then, ΔV_{OUT} for the charge integrating circuit in Figure 14 becomes,

$$\Delta V_{OUT} = -\frac{1}{C_{FB}} \int_0^{T_S} \Delta I_{OUT} dt = \frac{\Delta I_{OUT} T_S}{C_{FB}} = \frac{(g_m \Delta V_G) T_S}{C_{FB}}. \quad (39)$$

Thus, the voltage gain, A_V , can be written as,

$$A_V = \Delta V_{OUT}/\Delta V_G = (g_m T_S)/C_{FB} \quad (40)$$

So for high charge and voltage gain, it is necessary to maximize $g_m T_S$. It will also be shown in Chapter 5 that decreasing C_{FB} , increases the voltage gain but it also increases the noise gain. In contrast, decreasing C_{PIX} is beneficial both from a signal gain and noise reduction point of view. However, a tradeoff exists for the traditional co-planar layout of TFTs and sensor where decreasing C_{PIX} requires decreasing sensor area, which degrades pixel fill-factor. For medical imaging applications using C-APS readout circuits, a small C_{PIX} in addition to a high fill factor is required. Thus, continuous layer, thick a-Se sensors are discussed in Chapter 3 to achieve low pixel capacitance, high fill factor pixels.

2.3.4.2 Measurements and Discussion

The APS test pixel, consisting of an integrated a-Si amplifier circuit in a $250 \times 250 \mu\text{m}^2$ pixel area, was fabricated in-house and is shown in Figure 15.

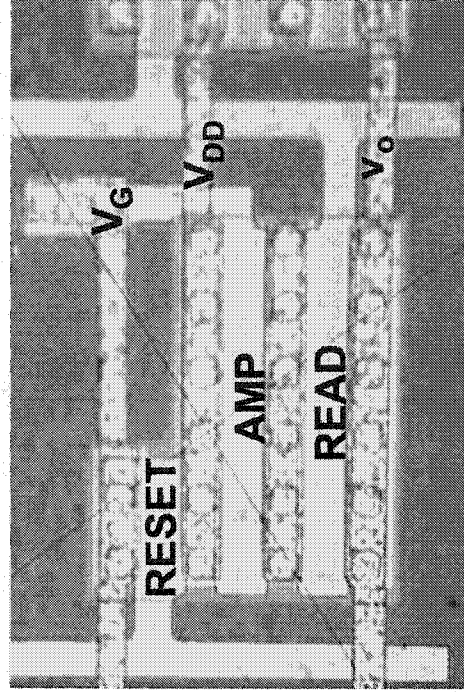


Figure 15 Die micrograph of current mode APS pixel

The small signal linearity is within 5% of the theoretical value and is shown in Figure 16. In addition, small signal voltage gain (A_V) measurements were performed on the APS test circuit using the charge amplifier of Figure 14 (a Burr-Brown IVC102 model), $V_{RD} = 20 \text{ V}$, $V_G = V_{DD}$ and a $C_{FB} = 10 \text{ pF}$ for various READ pulse widths, T_S and supply voltages, V_{DD} . The results are also shown in Figure 16.

Theoretical voltage gain, A_V (based on eqn. (5) where $A_V = \Delta V_{OUT} / \Delta V_G$) and experimental results agree reasonably well with a maximum discrepancy of about 10 %. The verified theoretical model of eqn. (5) was extended to predict charge gain in Figure 17 using eqn. (6) for different values of C_{PIX} , $C_{FB} = 10 \text{ pF}$ and $A_V = 1.33$ (for $T_S = 30 \mu\text{s}$ in Figure 16). Theoretically, using a low sensor capacitance (i.e. small C_{PIX}) provides a higher charge gain, which minimizes the effect of external noise. In addition, minimizing C_{PIX} also reduces the

reset time constant (which comprises mainly of the RESET TFT on-resistance and C_{PIX}) leading to faster pixel resets and hence, reducing image lag [49]. Like other current mode circuits [48], the C-APS, operating at a maximum of 30 kHz (for diagnostic fluoroscopy), is susceptible to sampling clock jitter. However, off-chip low-jitter clocks using crystal oscillators can alleviate this problem.

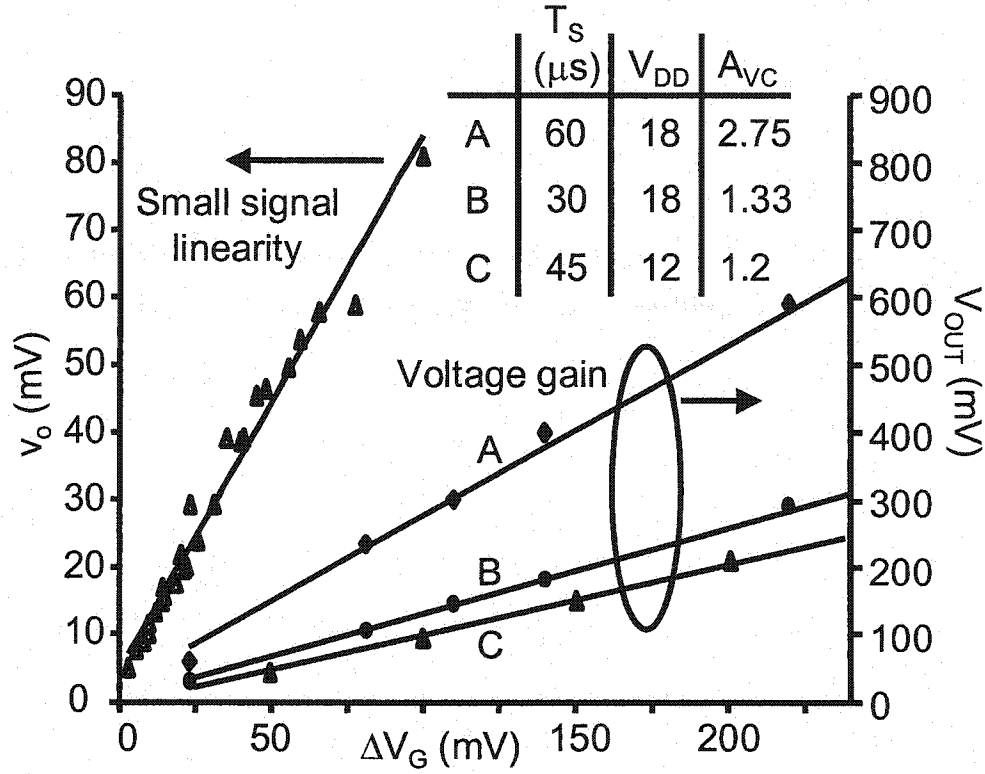


Figure 16. Small signal linearity and voltage gain for an in-house fabricated C-APS.

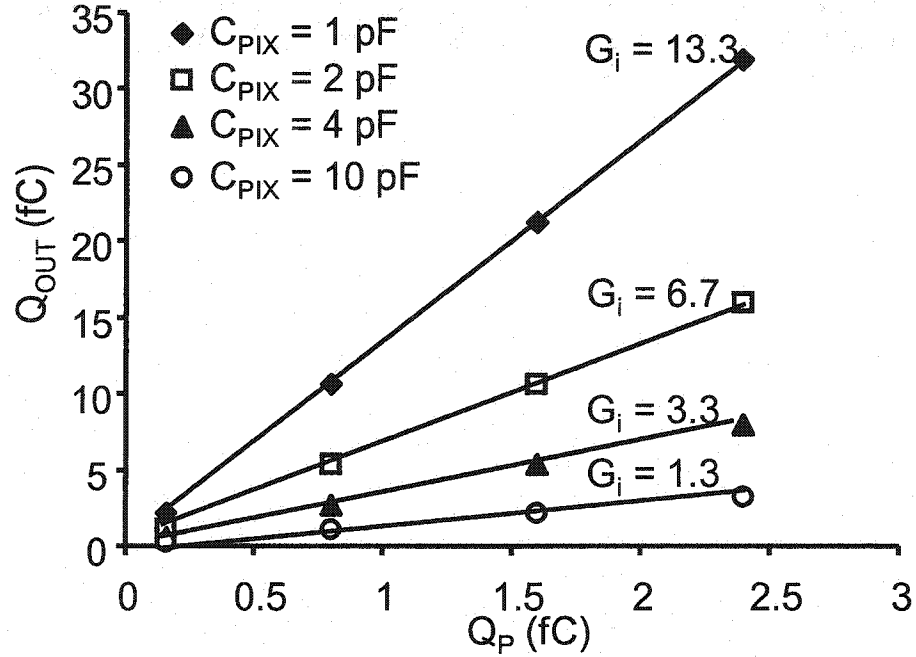


Figure 17. Theoretical charge gain (G_i) based on eqn. (38) for the fabricated C-APS.

2.3.5 Transient performance of C-APS

The transient performance of the C-APS must be considered since the circuit node voltages can significantly change due to the large gate pulse voltages and TFT capacitances. A large change in the circuit node voltage at the AMP TFT gate can cause the C-APS dc operating point to change during circuit operation and thus transient node voltage performance must be included into design considerations from the very beginning.

2.3.5.1 Charge injection and feed-through

Charge injection, also commonly called clock feed-through is responsible for error due to unwanted charges being injected into the circuit when transistors turn OFF. When a transistor is turned OFF, charge errors can occur via two mechanisms. The first is due to channel charge, which must flow out from the transistor channel to either the drain or source junctions. The channel charge of a transistor with a $V_{DS} = 0$ (i.e. in the switch mode of operation) is simply given as,

$$Q_{CH} = WLC_G V_{EFF} = WLC_G (V_{GS} - V_T) \quad (41)$$

If the drain and source terminals are at the same voltage and the gate pulse has a very sharp transition (i.e. a fast fall time), it can be approximated that half of the channel charge goes towards the source and the other half goes towards the drain terminal [124]. The second mechanism for charge error is due to the transistor overlap capacitances between the gate and source/drain junctions. The error due to overlap capacitance is generally smaller than the error caused by channel charge unless the transistor's dimensions are very small or it is being operated at a small gate voltage. The next section will discuss how charge injection errors occur in a C-APS circuit and their effect on circuit performance.

2.3.5.2 C-APS

During normal operation with a positive voltage at the gate, electrons have accumulated in the TFT channel. When the RESET TFT in the APS circuit of the figure below is turned OFF, the channel charge will flow out equally through both junctions if the clock waveform is very fast [125].

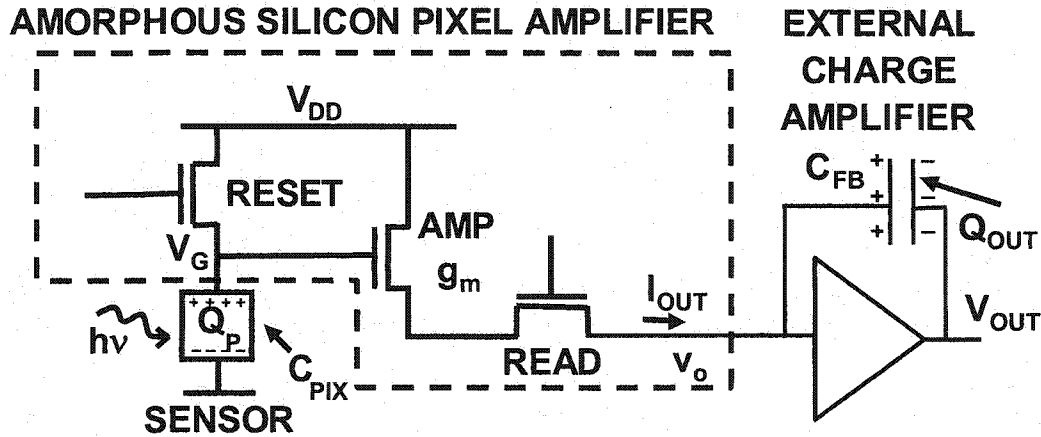


Figure 18. C-APS readout circuit schematic. The READ and AMP TFT are designed with a W/L of 150/25 each while the RESET TFT has a W/L of 60/25.

Note that for linearity in diagnostic medical imaging applications, the node V_G changes by at most, 10% of $(2(V_{GS} - V_T))$ as noted by the small signal linearity constraint presented in eqn. (34). Thus, a reasonable assumption would be that $V_D \sim V_S$ for the RESET TFT and the channel charge can be written as,

$$Q_{CH} = WLC_G V_{EFF} = WLC_G (V_{RESET} - V_T) \quad (42)$$

Half of the charge Q_{CH} goes to the V_{DD} supply and is of no consequence. However, the other half of Q_{CH} that goes to the integration node can affect the biasing point of the AMP TFT and must be determined. ΔV_{CHAN} , or the change in V_G due to the channel charge injection error, can be written as,

$$\Delta V_{CHAN} = (1/2)((V_{RESET} - V_T).C_G.W.L)/C_{PIX} \quad (43)$$

For a $V_{RESET} = 15$ V, $C_G = 25$ nF/cm², $W = 60$ μ m, $L = 25$ μ m, and a nominal $C_{PIX} = 1$ pF, $\Delta V_{CHAN} = 2.44$ V. Similarly, if a state-of-the-art TFT is used where $L = 5$ μ m and W is scaled down to 12 μ m, and maintaining the rest of the parameter values, the ΔV_{CHAN} is less than 0.1 V.

Noting that the C_{GS} of the RESET TFT and C_{PIX} are in series from the V_{RESET} node to ground allows an approximation of the charge feed-through due to overlap capacitance. When the RESET pulse at the TFT gate changes, the charge flowing into C_{GS} is the same as the change flowing into C_{PIX} since they are series capacitors. ΔV_{OV} , or the change in V_G due to the overlap capacitance charge injection error, can now be written as,

$$\Delta V_{OV} = |V_{RESET_ON} - V_{RESET_OFF}|(C_{GS}/(C_{GS} + C_{PIX})) \quad (44)$$

where V_{RESET_ON} and V_{RESET_OFF} are the ON and OFF values of the RESET TFT gate pulse. Thus for $C_{GS} \ll C_{PIX}$, the charge injection due to overlap capacitance can be made negligible. As an example, for a 60/25 TFT with a 2 μ m overlap, $C_{GS} = 23$ fF. Then for a +15/-5 RESET gate pulse and a $C_{PIX} = 1$ pF, $\Delta V_{OV} = 0.45$ V. Scaling the 60/25 TFT to a state-of-the-art 12/5 TFT as before, the C_{GS} becomes less than 5 fF and ΔV_{OV} is now less than 0.09 V.

In general, it can be said that feedthrough at the RESET TFT will not affect the C-APS performance for a state-of-the-art process since the error is deterministic (unlike random noise processes) and is accounted for in double sampling techniques. Even for the in-house process, the error is manageable by choosing a sufficiently large C_{PIX} and a large value for the power supply, V_{DD} that accounts for any dips or increases in V_G due to feed-through.

A similar analysis can be performed on the READ TFT for examining the transient voltages at the V_B terminal. The situation is somewhat different from the RESET TFT since there is no large capacitor at the V_B node to reduce the effect of feed-through error and the transient voltages can be quite large. Since there is no C_{PIX} equivalent at node B, the node

capacitance comprises of parasitics such as the overlap capacitance of the AMP TFT and TFT channel capacitance components. In contrast to the READ TFT at node B, the situation with the RESET TFT at the integration node, V_G was simplified considerably because of the large C_{PIX} . Simulation results using the highly accurate in-house TFT model of the C-APS circuit's transient performance due to a READ TFT pulse are shown below.

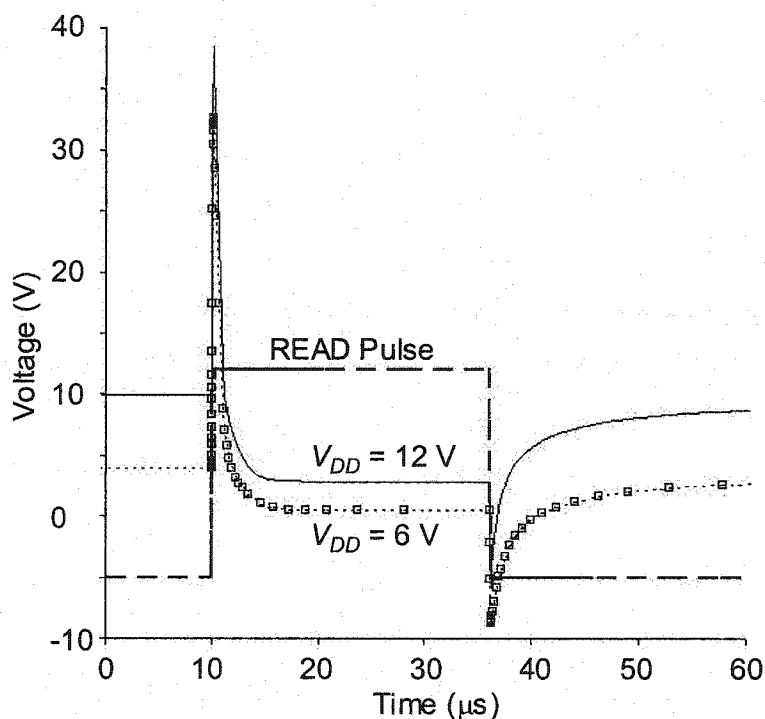


Figure 19. Node B transients for two supply voltages (V_{DD}). Here, a +12/-5 V READ TFT pulse is used.

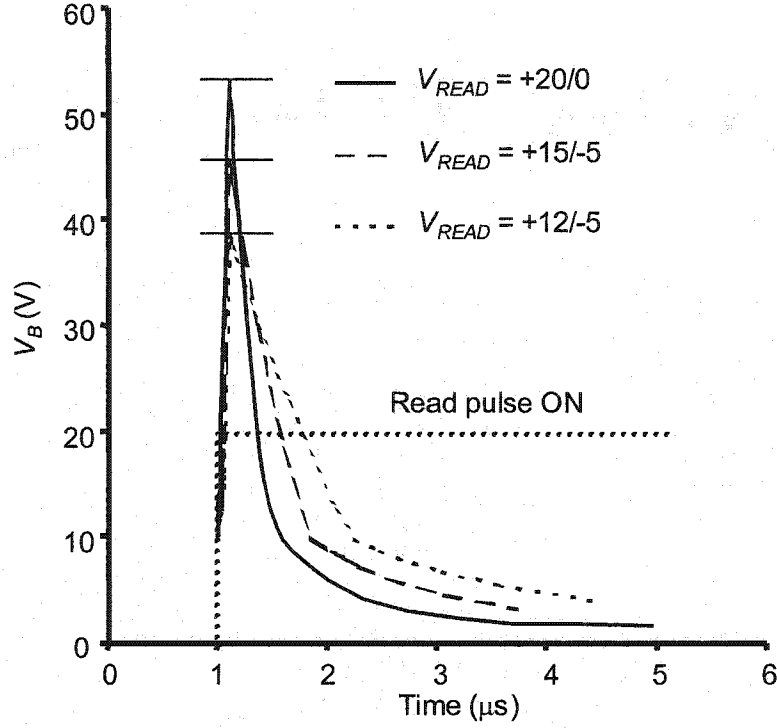


Figure 20. Node B transient voltage for different READ TFT gate pulse voltages.

The above transients are not necessarily troublesome since they disappear after a few μs even for the in-house TFT process. Their duration, when the READ TFT pulse turns ON, is governed mainly by a time constant formed by the node B capacitance and the READ TFT ON resistance. Note that in Figure 20, as the READ TFT pulse ON voltage is made larger (hence reducing the READ TFT ON resistance), the duration of the transient decreases. For a state-of-the-art process, the transients can be reduced both in magnitude and duration by scaling down the TFT sizes and by designing the AMP to READ TFT aspect ratios appropriately. When the READ TFT is turned OFF, the main charging path for node B is via the AMP TFT which charges up node B until the AMP TFT turns OFF to a maximum voltage of $(V_G - V_T)$. Since the AMP TFT is turning OFF as the voltage at node B rises, the rise time is relatively independent of the AMP TFT size. The effect is illustrated in Figure 19 where, as the supply voltage V_{DD} is increased (hence increasing the AMP TFT's drive current), node B charges up at around the same rate for the both V_{DD} values.

During C-APS readout, the steady state current I_{OUT} contains the necessary image information and the transients are irrelevant. Therefore, in order to eliminate any negative

effects of transients on the charge amplifier's output voltage, the READ TFT can be turned ON before I_{OUT} integration on the charge amplifier begins in order to let the node voltage, V_B and hence I_{OUT} settle. Waveforms that avoid transients for proper C-APS operation are shown in Chapter 6 where they are implemented on an in-house developed 2 x 2 C-APS imaging array. Of course, neglecting transients will add further delay to readout slowing down the overall speed of the circuit and thus it is preferable to minimize the duration of the transient voltages by scaling down the TFT process and designing proper AMP TFT to READ TFT aspect ratios. Most of the work presented on the C-APS readout circuit has been published in [45][52][54][55].

2.4 Feasibility for diagnostic medical x-ray imaging

While the PPS architecture has the advantage of being compact and thus amenable to high-resolution imaging, reading the low output signal of the PPS requires column charge amplifiers that can complicate circuitry. More importantly, these charge amplifiers add a large external noise component to the PPS that reduces the minimum readable input signal of the detector. In addition, the numerous gate and data lines characteristic of large area arrays, make the interfacing of the imaging array to off-panel readout circuit bulky and error-prone. Therefore, the benefits of a pixel architecture that performs on-pixel input signal amplification as well as interfacing with on-panel multiplexers are evident.

2.4.1 Linearity

In terms of linearity, the PPS and V-APS depict large signal linearity and hence are suitable for imaging applications requiring linear behavior. The C-APS, however, is only linear for small signal input voltages as discussed earlier. The small signal condition on the C-APS is shown again for convenience below as,

$$\Delta V_G \ll 2(V_G - V_T), \quad (45)$$

For a typical diagnostic x-ray medical imaging array, using eqn. (30) with a $C_{PIX} = 0.75$ pF and the table above, a maximum ΔV_G of 0.77 V chest radiography, 1.54 V for mammography, and 8 mV for fluoroscopy can appear on the integration node. To maintain

the C-APS in small signal mode via eqn. (41), a minimum V_G gate bias of 7.7 V is required for radiography and 15.4 V for mammography. The choice of V_G for fluoroscopy is governed more by gain requirements since the maximum input signal is quite small. Thus, the C-APS can provide adequate linearity for diagnostic medical imaging applications by appropriate biasing. Note also that assuming area requirements are met, the same C-APS circuit could be used for all three modalities since the gain is programmable via the supply voltage and the readout sample time.

2.4.2 Gain and Noise

In terms of gain, both the PPS and V-APS provide almost unity gain barring non-ideal parasitics. In terms of noise, the PPS appears superior to the V-APS since the larger count in the V-APS readout circuit increases the noise floor. In contrast to the PPS and V-APS, the C-APS can be designed to provide gain to overcome the noise due to the extra TFTs in the pixel as well as the external readout circuitry hence, improving the overall pixel SNR. The noise performance of the C-APS is discussed in a later chapter in more detail.

2.4.3 Readout rate

As discussed in previous sections, the amorphous silicon PPS provides rapid readout for the C_{PIX} values used in diagnostic medical imaging applications. Unlike the PPS, the V-APS is slower due to the need to fully charge the prohibitively large array column C_{LINE} . However, the amorphous silicon V-APS appears feasible for static diagnostic medical imaging modalities such as chest radiography and mammography if the technology is scaled appropriately (mainly to reduce parasitic capacitance).

In contrast to the other pixel readout circuits, the readout rate for the C-APS is mostly determined from the minimum gain requirements. Since the C-APS gain is a direct function of readout sampling time, increasing the readout time gives a larger gain. For amorphous silicon TFTs, it appears that the C-APS can satisfy the gain and readout time requirements for all diagnostic medical imaging modalities.

2.4.4 Area constraints

Unlike a conventional PPS, which has one TFT switch, there are three TFTs in the both APS pixel readout circuits. This could undermine fill factor if conventional methods of placing the sensor and TFTs are used. Therefore, in an effort to optimize fill factor, the TFTs can be embedded underneath the sensor (vertically stacked pixel architecture) to provide high fill factor imaging systems.

In comparison to the PPS where a gate, data and sensor bias line is required per pixel, both APS circuits require two additional bias lines for pixel reset and the pixel power supply. This adds to the circuit complexity as well as increasing parasitic capacitance. However, using an appropriately thick low-k dielectric for the stacked architecture can reduce the parasitic components. Progress and results for an in-house developed vertically stacked pixel architecture is presented in Chapter 3.

2.4.5 Summary

The characteristics of the pixel readout circuit architectures examined are compiled in the table below. Evidently, the C-APS demands further investigation particularly because the circuit gain can be beneficial in other medical imaging applications by offering potentially reduced patient x-ray doses. Therefore, the remainder of the thesis will focus on C-APS development, characterization and integration with an x-ray sensor.

Table 5. Comparison of various pixel architectures

	PPS	V-APS	C-APS
Linearity	Large signal	Large signal	Small Signal
Gain	Unity	Unity	> unity
Area	1 TFT, 3 bias lines	3 TFTs, 5 bias lines	3 TFTs, 5 bias lines
Readout time	Real-time	Static	Real-time
MUX interface	No	Yes	Yes

Chapter 3. Fabrication of TFT circuits and arrays

An inverted staggered fully wet-etch a-Si TFT process developed previously [62] at the University of Waterloo forms the basis for array fabrication in this research. While the previously developed process provided good TFT characteristics (low leakage currents and high ON/OFF current ratios), it needed modification for interfacing with sensors in imaging pixels and reliability for arrays. This chapter starts with TFT process improvements and then moves on to the additional steps required to interface a sensor with APS pixels and arrays. It concludes with an overall process flow for an implemented 2 x 2 C-APS pixel array for integration with an a-Se X-ray detecting photoconductor.

3.1 Reliable High Voltage TFT for large area arrays

3.1.1 Introduction

Amorphous silicon (a-Si) thin film transistors (TFTs) are widely used as low voltage pixel addressing elements in large area flat panel displays on account of their low cost and low processing temperatures. Many applications, however, require drive voltages as high as a hundred volts or more in the area of ferroelectric liquid crystals and electrographic plotters [59]. More recently, in direct detection x-ray imaging, where a high voltage detection architecture is implemented [60], a fault condition can occur on the drain of the readout TFT switch. The fault causes a potentially fatal voltage buildup on the TFT drain that can cause

dielectric breakdown. For these applications, a high-voltage TFT (HVTFT) is beneficial over conventional TFTs.

For a TFT to be useful in large area applications, device reliability and yield are two important factors that determine the complexity of the circuit design and the final cost. For example, in active matrix liquid crystal displays (AMLCD), which is one of the biggest application areas of a-Si TFTs, it is common practice to divide a pixel into four sub-pixels each with its own driver TFT [61]. This is done to ensure that even if one TFT is faulty, the pixel still operates using the redundant TFTs.

In addition, TFT size is becoming increasingly important in typical large area a-Si TFT applications such as imaging and displays. With conventional co-planar pixel architectures where the TFT is placed alongside a sensing or display element, an important figure of merit is the fill factor or aperture ratio. This is defined as the area of the pixel that is capable of sensing or emitting photons. Generally, a larger fill-factor/aperture ratio is preferable for high performance pixels and hence, the size of the TFT must be minimized.

This section examines the performance of conventional, high voltage and soft contact high voltage TFT (SCTFT) designs and their feasibility for use in large area applications. Factors such as high voltage operation, reliability and TFT size are discussed in the following sections.

3.1.2 TFT structures and process

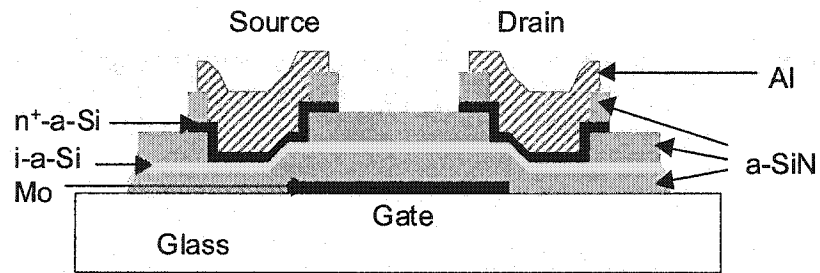
The four basic types of planar TFTs are defined by the order of deposition of the gate electrode, gate insulator, semiconductor and drain/source contact layers [62][63]. For a-Si TFTs, the most widely used structure is the bottom gate, inverted staggered TFT, which uses amorphous silicon nitride as the gate insulator. In contrast, the staggered TFT structures have the drain/source and gate contacts on opposite sides of the semiconductor layer. The inverted staggered approach with a top passivation nitride is preferred because it minimizes the defect states at the top interface and improves device performance [62]. In this research, the inverted staggered TFT structure is experimented upon for high voltage applications by varying the location of the drain/source electrodes and their ohmic contacts to the a-Si semiconductor layer.

Different TFTs fabricated on the same die are shown in Figure 21. The fabrication steps, at 260°C, can be described using Figure 21(a) as an example. First a 120 nm molybdenum (Mo) layer is deposited and patterned to form the gate metallization. This is followed by PECVD deposition of a 250 nm gate nitride (a-SiN), a 50 nm a-Si semiconductor layer and a second 250 nm a-SiN layer all within the same vacuum pump down. The source and drain contact layers are defined by photolithography and etched using a buffered HF acid solution. The etching is immediately followed by deposition of a 50 nm n⁺ a-Si contact layer and a masking a-SiN layer in the same vacuum pump down. The masking nitride is required for the proper etching of the contact layer. The third step involves patterning the masking nitride via photolithography and HF etching. The patterned a-SiN nitride layer then becomes the mask (for KOH etching) used to pattern the silicon based contact layer (for separation of the TFT drain and source) as well as the a-Si film (for TFT to TFT isolation). A fourth photolithographic step is used to define contacts in the masking nitride layer and Aluminum (Al) is deposited as the final metal layer. The fifth and final photolithographic mask is used to pattern the TFT source/drain Al metal. Further details of this TFT process can be found in [64].

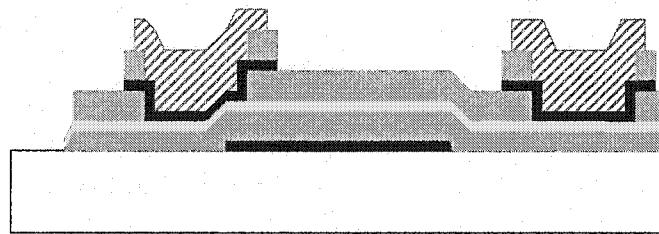
Conventionally, a-Si inverted staggered TFTs are fabricated using a four mask process where the n⁺ a-Si contact layer and the top source/drain Al metal are patterned simultaneously using only one photolithographic mask. Introduction of the masking nitride layer into the TFT process increases the mask count to five. However, the masking nitride provides flexibility in positioning the n⁺ a-Si and Al source/drain contacts to the TFT a-Si channel layer.

Four different types of TFTs are fabricated to examine the effect of positioning drain/source contacts on TFT performance. The first, shown in Figure 21(a) is a conventional design where the metal and n⁺ a-Si contact layers overlap the gate metal. In Figure 21(b), a conventional high voltage design is depicted which is a natural extension of the conventional TFT design. Here, to decrease the likelihood of breakdown, the TFT drain electrode and its n⁺ a-Si ohmic contact are placed some distance away from the gate in order to drop the electric field over a larger distance. Figure 21(c) contains a TFT similar to Figure 21(a) where the n⁺ a-Si contact layer has been extended to prevent the gate metal from

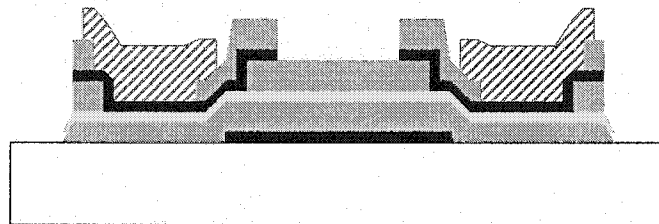
overlapping with the drain-source metallization. Figure 21(d) is a similar TFT with the drain ohmic contact layer being extended further to permit the application of larger drain voltages.



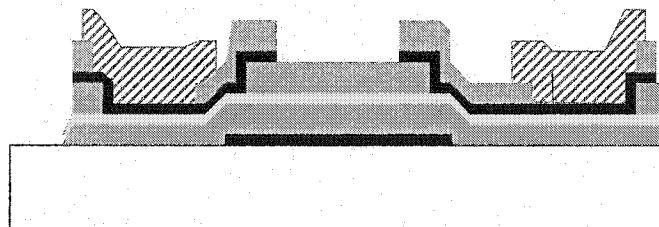
(a)



(b)



(c)

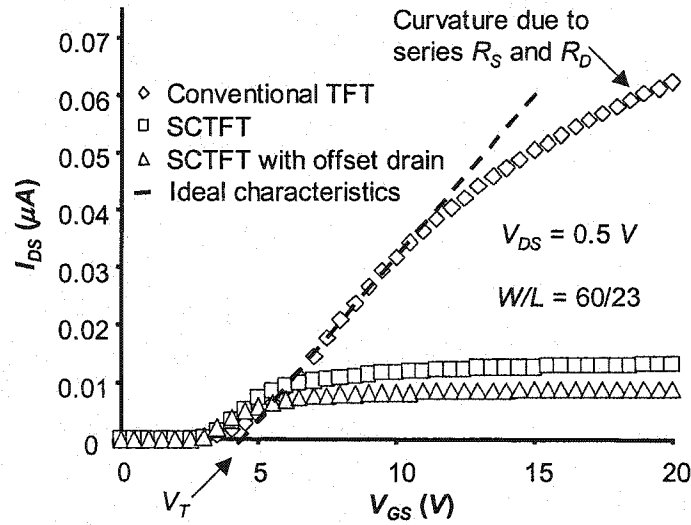


(d)

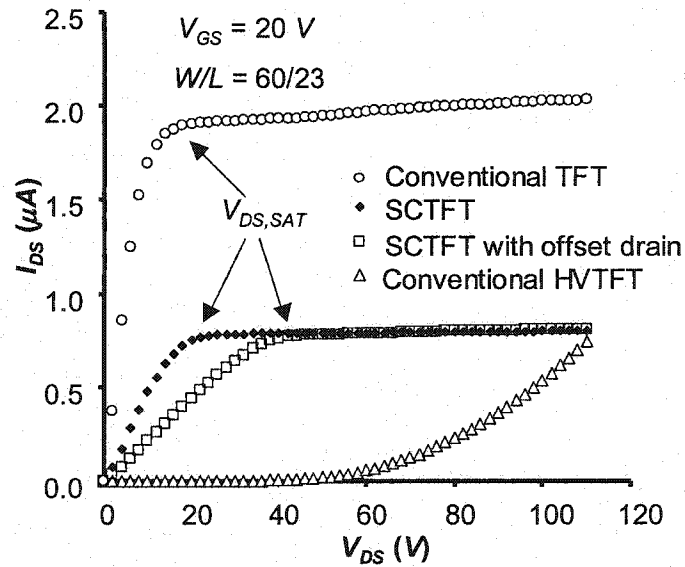
Figure 21. Different TFT structures fabricated for high voltage performance testing. (a) Conventional TFT, (b) Conventional High Voltage TFT (HVTFT), (c) Soft Contact High Voltage TFT (SCTFT), (d) SCTFT with offset drain.

3.1.3 Results

The fabricated amorphous silicon TFTs were wire bonded in a ceramic package and placed in a grounded metallic box during the measurement. The device characteristics were measured for TFTs with a W/L ratio of 60/25. Consistent results were obtained for all four TFTs in the four die samples tested. TFT transfer and I-V characteristics are shown in Figure 22 below.



(a)



(b)

Figure 22. (a) Transfer and, (b) I-V characteristic for the various TFTs fabricated.

Before measurement, the samples were annealed to 180 °C and allowed to cool for three hours to “initialize” their threshold voltage (V_T) values. V_T was measured after annealing and was 4.5 V for both the linear mode (Figure 22 (a)) and saturation mode measurement (Figure 22 (b)). The V_T values hold true for all devices other than the conventional HVTFT. One effect of using an n^+ a-Si contact layer is its non-negligible series resistance, especially for the TFTs with extended source and drain regions. This non-ideal effect is examined for the conventional and the SCTFTs in the next section.

3.1.4 Extraction of TFT series resistance

From Figure 22 (a), it can also be seen for all TFTs that there is some series resistance that causes the I_{DS} - V_{GS} curve to not be completely linear for large values of V_{GS} . This non-ideal resistance is distinctly different for the various TFT structures. For comparison purposes between the different fabricated TFTs, series resistance was extracted for both linear and saturation mode data. One method of extracting source and drain series resistance is to represent the TFT by the equivalent circuit model shown in Figure 23.

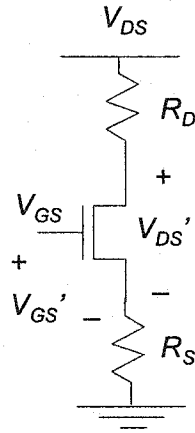


Figure 23. Circuit representation of TFT with series source and drain resistances.

First, the linear mode of TFT operation is examined using a simple drain current (I_{DS}) model with the non-ideal series source (R_S) and drain (R_D) resistances included. This model is appropriate for TFT behavior in the linear mode when $V_{DS} \ll V_{GS} - V_T$. The corresponding I_{DS} equation is given by,

$$I_{DS} = \mu_{EFF} C_G \frac{W}{2L} \left(2(V'_{GS} - V_T) V'_{DS} - (V'_{DS})^2 \right) \quad (1)$$

where,

$$\begin{aligned} V'_{GS} &= V_{GS} - I_{DS} R_S, \\ V'_{DS} &= V_{DS} - I_{DS} (R_S + R_D) \end{aligned} \quad (1A)$$

In eqn. (1), μ_{EFF} is the effective carrier mobility, C_G is the gate capacitance per cm^2 , and W/L is the aspect ratio of the TFT. For the fabricated TFTs, $C_G = 25 \text{ nF/cm}^2$ and $W/L = 60/25$. A value for the effective electron mobility, μ_{EFF} , was extracted by fitting eqn. (1) with $R_D = R_S = 0$ to the ideal TFT (i.e. no series resistance) curve in Figure 22(a).

The extracted parameters for a TFT with no series resistance allow eqn. (1) to be fitted using various series resistance values to the measured linear mode TFT data of Figure 22(a). Here, it was assumed that for the symmetric TFTs, R_S and R_D are equal. The results are summarized in Table 6 below.

Table 6. Extraction of TFT series resistances in linear mode ($V_{DS} = 0.5 \text{ V}$)

	$R_S (M\Omega)$	$R_D (M\Omega)$
Conventional TFT	1.4	1.4
SCTFT	15	15
SCTFT with offset drain	15	37

The high value of series resistance for the conventional TFT and SCTFTs can be attributed to the finite length of the n^+ a-Si ohmic contact layer between the Al source/drain metal contact and the a-Si channel. The difference between the series resistances of the SCTFT and the SCTFT with offset drain is attributed to the extended n^+ a-Si contact layer shown in Figure 21(d). From the various TFT series resistance values in Table 6, the resistivity of the 30 nm thick n^+ a-Si layer can be extracted consistently as $\sim 150 \text{ } \Omega \cdot \text{cm}$. The extremely large drain series resistance of the conventional HVTFT made it difficult to distinguish ON current from leakage current in the above extraction procedure (where $V_{DS} = 0.5 \text{ V}$) and hence, the series resistance value was not extracted for that particular TFT.

Figure 22 (b) shows the I_{DS} - V_{DS} transfer characteristics of different TFTs. At high V_{DS} voltages, the series resistance on the source side determines the saturation current of the

different TFTs. It is seen from Figure 22(b) that the saturation current is approximately the same for the SCTFT and the SCTFT with offset drain. For sake of comparison, the series resistances for all fabricated TFTs were extracted using the I_{DS} saturation data. The extraction procedure requires including the series resistance terms into the saturation mode TFT equation,

$$I_{DS} = \mu_{EFF} C_G \frac{W}{2L} (V_{GS}' - V_T)^\alpha \quad (2)$$

where,

$$V_{GS}' = V_{GS} - I_{DS} R_S \quad (2A)$$

Here, α is a parameter related to the characteristic temperature of the a-Si density of states as described in Appendix A. From previous work, α was extracted for the University of Waterloo 260°C TFT process as 2.38 [46]. Fitting eqn. (2) to the saturation mode TFT data and neglecting channel length modulation, the source series resistances for the various TFTs are extracted. To obtain the drain series resistance from the saturation curves, note that at saturation,

$$V_{DS}' = V_{GS}' - V_T \quad (3)$$

where,

$$\begin{aligned} V_{GS}' &= V_{GS} - I_{DS} R_S, \\ V_{DS}' &= V_{DS} - I_{DS} (R_S + R_D) \end{aligned} \quad (3A)$$

Based on extracted values of the voltage at which I_{DS} saturates ($V_{DS,SAT}$), the drain series resistance is obtained for all of the TFTs in Table 7.

Table 7. Extraction of TFT series resistances in saturation mode ($V_{GS} = 20$ V)

	R_S (M Ω)	R_D (M Ω)	Saturation Voltage ($V_{DS,SAT}$)
Conventional TFT	2.4	0.53	21
SCTFT	9.9	7.5	26
SCTFT with offset drain	9.9	32.5	46

The lumped resistance extraction model [59] of Figure 23 tries to incorporate non-linear space charge limited current contact effects and series resistance into simple TFT drain and

source resistor models. The difference between the extracted linear and saturation mode series resistance values for the conventional TFT and SCTFT are possibly due to the voltage dependent components of contact resistance. The error between linear and saturation mode series resistance values is the least for the case of the SCTFT with offset drain. This is likely because the large resistance of the extended n^+ a-Si contact layer dominates over any other contact resistance mechanism.

The resistivity of the n^+ a-Si layer, extracted from the saturation mode values for the SCTFT with offset drain, is similar to the results for resistivity extracted from the linear region corroborating the reliable resistive performance of the n^+ a-Si TFT contact layer.

Note that the $V_{DS,SAT}$ at which I_{DS} saturates in Figure 22(b) for the SCTFTs is dependent largely on the series resistance at the drain side. Clearly, the conventional HVTFT has the highest value of drain series resistance since the current does not saturate even at the largest measured voltage, $V_{DS} = 110$ V.

It is also interesting to note that due to the high source contact resistance, the channel length modulation effect of the SCTFT and SCTFT with offset drain is significantly suppressed in comparison to that of the conventional TFT.

3.1.5 Discussion

The results in the previous section indicate that a TFT with a conventional design can withstand high voltages and outperforms the ON currents of all other TFT designs shown in Figure 21. The reason for this performance may be speculated upon by comparing the fabrication process of the current TFTs to past efforts [63].

Although there are some differences in the silicon nitride films, it is likely that the main difference between the past and present TFTs lies in the type of contact layer used: an n^+ a-Si film is used presently whereas an n^+ μ c-Si film was used in previous work [63]. The particular μ c-Si film used in the past had a crystalline structure [62] thought to increase the likelihood of the drain/source metal, Al, spiking through the contact to the a-Si layer and causing breakdown at moderate drain voltages (> 40 V reported in [62]). Past experiments also showed supporting evidence that the gate nitride dielectric is disturbed by the top metallization at the edge of the gate metal line where the dielectric is thinned due to slope

coverage limitations [65]. So, by shifting the Al top contact, the SCTFT was developed by Miri [63] to ensure spiking occurred at a further distance from the thinned dielectric, thus permitting the application of larger voltages at the TFT drain.

For the present TFTs however, the amorphous nature of the n^+ a-Si contact film may be reducing the amount of Al spiking, hence allowing higher voltage operation to take place. The main disadvantage of using an n^+ a-Si contact layer is the increased series resistance that serves to reduce the ON-current of the TFT as discussed in the previous section. Comparing and normalizing the n^+ a-Si contact layer TFT results to the n^+ μ c-Si contact TFT fabricated previously, there is a threefold increase in ON-current at similar biases for the n^+ μ c-Si contact TFT. However, this may or may not be of concern depending on the type of application that TFT is used in.

In imaging applications (with a traditional co-planar pixel layout) where the TFT is used as a switch [60], it is preferable to use the smaller conventional TFT layout with an n^+ a-Si contact layer. Since the TFT operates as a switch, the drive current is not as essential as the improvement in fill factor. In contrast, for current driven applications such as OLED displays, it might be beneficial to use the SCTFT architecture since the OLED brightness is largely dependent on the drive current of the TFT, which the n^+ μ c-Si film preserves. In either case, the conventional HVTFT structure of Figure 21(b) is not practical since most of the pixel operation occurs at fairly low voltages (< 40 V) where it is important to have good TFT characteristics such as low V_T and high ON-currents.

In terms of reliability, the SCTFT offers improved reliability at the cost of area, since the offset between drain/source and gate metals reduces the chance of a short circuit. In addition, the chance of a short between drain and source metal on the same level is also decreased due to the increased separation.

For large area applications, it is desirable not only to improve TFT reliability but also that of the surrounding interconnects. This is accomplished by depositing an additional a-Si:N film of an arbitrary thickness after the KOH etching step as shown in Figure 23(a). In addition to serving as an extra isolation layer between the drain/source and gate metal interconnects, it is particularly beneficial in reducing parasitic capacitances in large area applications. The parasitic capacitances ($C_{PARASITIC}$) refer to those occurring due to the gate and data metal line overlaps in each pixel as shown in Figure 24(b).

The additional a-SiN layer comes at little cost: there is no extra masking or photolithographic step required and it reduces parasitic capacitance while the V_T remains a function of the gate nitride thickness only. While there is some evidence pointing to the n^+ a-Si contact film as the reason for the success of the conventionally designed TFT at high voltages, further work (beyond the scope of this thesis) is necessary to verify the exact reason.

The additional a-SiN layer provides the benefits of improved reliability in that the overlapping metal interconnects are insulated by a thicker dielectric. Secondly, the thicker dielectric reduces the parasitic capacitance thus improving performance. Lastly, because of the additional a-SiN insulator, the gate nitride can be made thinner, if desired, to reduce the threshold voltage and hence improve TFT performance. The work presented in this section has been published in [126].

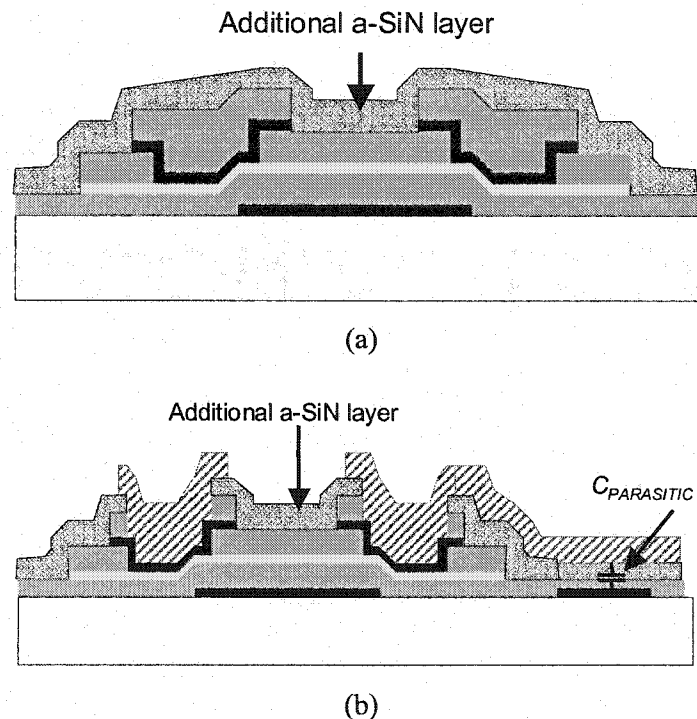


Figure 24. TFT process modification for large area applications. (a) Process step where additional a-SiN is included and, (b) final TFT structure with parasitic capacitance shown between interconnects.

3.2 Continuous layer sensor integration

3.2.1 Non-overlapped electrode process

A traditional co-planar imaging pixel process places the sensor and TFT beside each other on the imaging panel. While this gives process simplicity, it also tends to reduce the pixel fill factor, which is determined by the ratio of the X-ray or light sensitive area of each pixel to the overall pixel pitch. A cross-section for a conventional non-overlapped pixel process using an a-Se photoconductor appears in the figure below. Here, the sensor back electrode and a TFT shield are included on the same metallization. The Al shield is necessary to prevent charge from accumulating at the bottom of the a-Se film over the TFT channel thus giving rise to a parasitic back channel that would degrade TFT leakage characteristics and is discussed more in the next section.

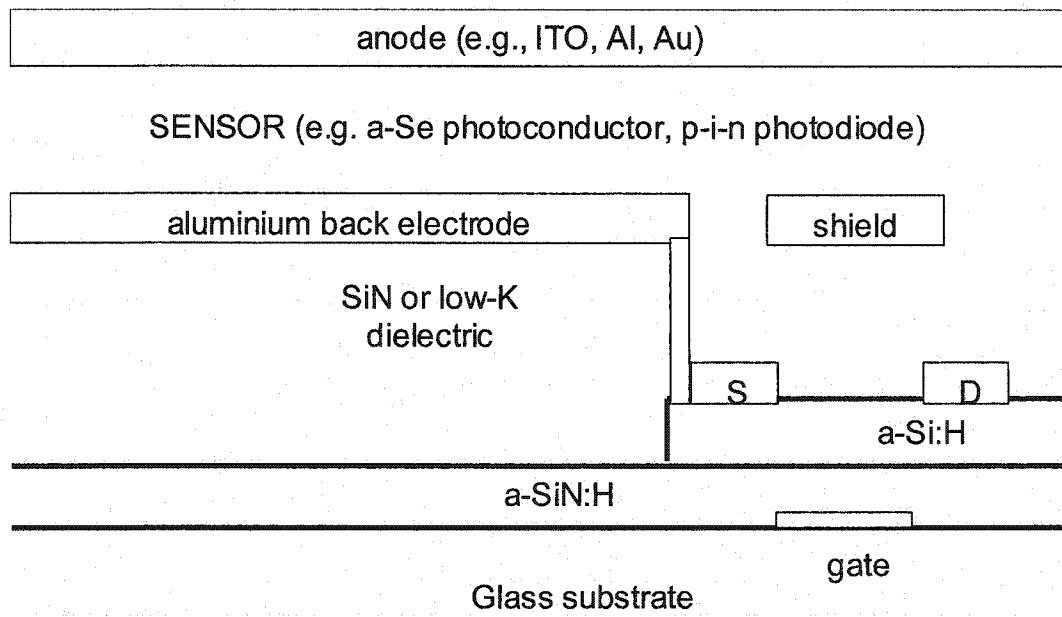


Figure 25. Conventional planar TFT process

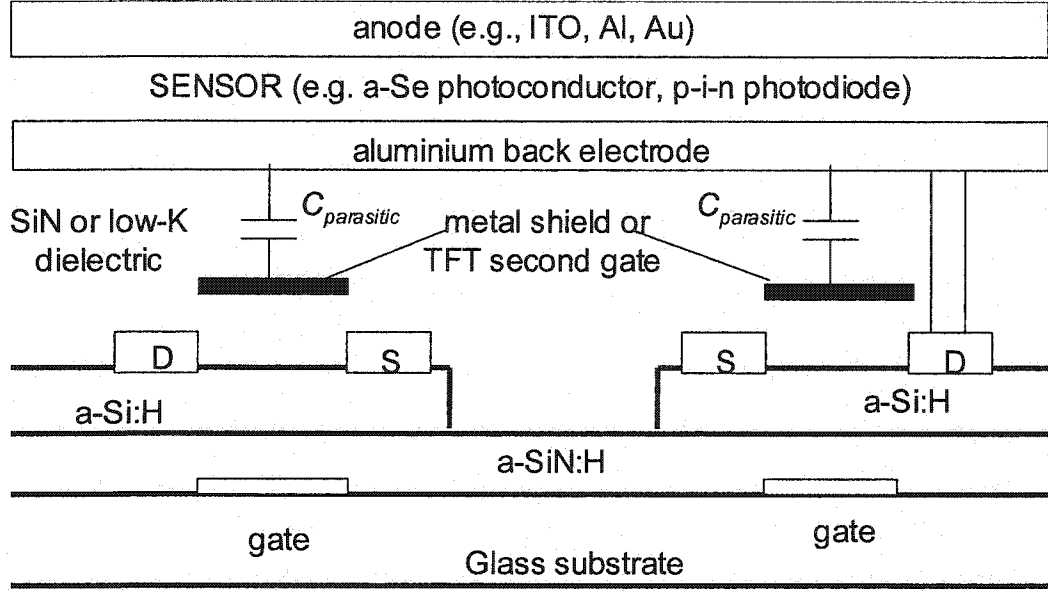
While co-planar pixel architectures may be suitable for imaging pixels where the readout circuit is a simple TFT switch (e.g. PPS), the larger number of TFTs required for on-pixel amplification (e.g. APS) necessitates a move towards vertically stacked pixel architectures.

Also, since a-Si TFTs consume larger areas than their CMOS counterparts, a diagnostic medical imaging modality such as large area mammography that requires small pixel pitch ($50\text{ }\mu\text{m} \times 50\text{ }\mu\text{m}$) can be challenging to implement in a co-planar architecture even if PPS architectures are used.

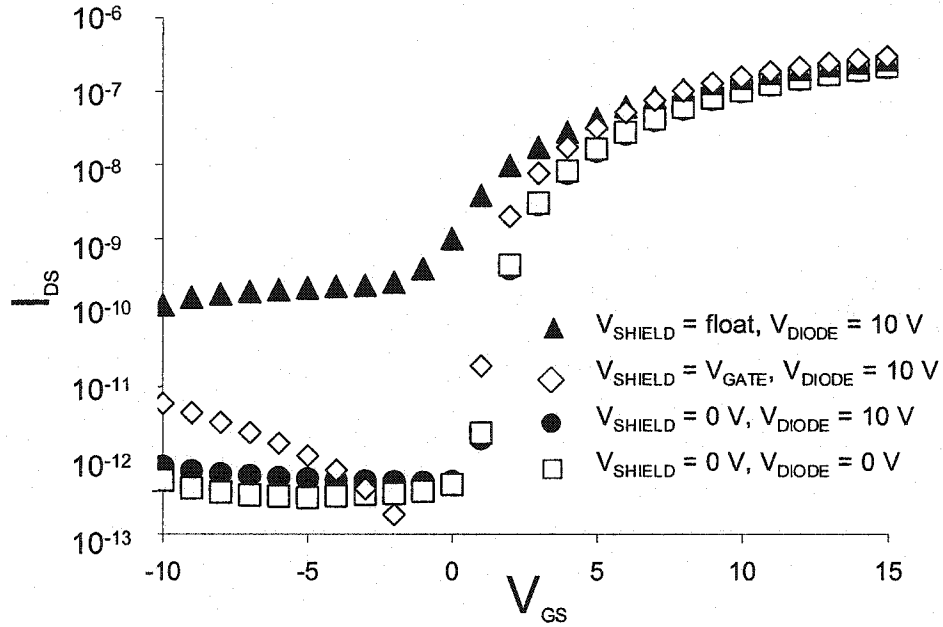
3.2.2 Fully overlapped process

In large area flat panel x-ray imagers, it is important to ensure that the fill factor should be high enough to ensure sufficient charge collection. Conventional imagers are based on a co-planar architecture where the sensor and readout circuitry are placed adjacent to one another. Increasing the on-pixel density of TFTs (such as for an APS readout circuit) or scaling down pixel sizes reduces the fill factor. Using a fully overlapped architecture [42] with a continuous back electrode over the APS pixel can circumvent this. However, the continuous back electrode can give rise to parasitic capacitance, whose effect becomes significant when the electrode runs over the various TFTs in the APS. One possible effect of the back electrode is to induce a parasitic channel in the a-Si layer of an overlapped TFT during its OFF state, giving rise to a larger I_{DS} leakage current [127]. This leakage is particularly severe if the overlapping back electrode is separated from the TFT by a thin insulating layer. To make the I_{DS} leakage independent of insulator thickness, an alternate TFT structure based on a dual gate architecture [128] is employed, in which the voltage on the top gate (metal shield) can be chosen to minimize the charge induced in the (parasitic) top channel of the TFT.

Figure 26(a) illustrates the structure of a dual gate TFT in a fully overlapped sensor architecture where a second gate is inserted between the sensor back plate and the TFT. Figure 26(b) shows static current measurements made on a single dual gate TFT structure ($W/L = 250\text{ }\mu\text{m}/25\text{ }\mu\text{m}$) embedded underneath a continuous back electrode using amorphous silicon nitride as the insulator. Modeling details of the dual-gate TFT structure are outside the scope of this thesis and the reader is referred to [128] for further information.



(a)



(b)

Figure 26. (a) Fully overlapped architecture, (b) TFT transfer characteristics ($V_{DS} = 1$ V)

For the Al back electrode potential, $V_{DIODE} = 10$ V, the lowest values of leakage current are obtained when the TFT second gate bias, V_{SHIELD} , is set to either 0 V or to the TFT bottom gate voltage, V_{GATE} . In the case where V_{SHIELD} is floated, the leakage current is

significantly larger. For a continuous layer sensor APS architecture, it is preferable for V_{SHIELD} to be biased to 0 V. The main reason is that since there are parasitic capacitances ($C_{parasitic}$) between the TFT top gate and the sensor back plate, connecting the top and bottom gates on a TFT gives rise to an additional parasitic capacitance at the TFT's bottom gate. The sensor's pixel capacitance (C_{PIX}) is usually made ten times larger than the parasitics that surround it to mitigate detrimental effects related to parasitic capacitances. Hence, a corresponding increase in C_{PIX} would be required to account for the top gate parasitic capacitance leading to poor APS charge gain and noise performance [53]. In addition, since the RESET and READ TFTs are pulsed, detrimental charge sharing effects (e.g. feedthrough) will be heightened. In contrast, if V_{SHIELD} is biased to a constant 0 V, the parasitic capacitance that results between the back electrode and the TFT top gate can be used to save pixel area by acting as part of the APS pixel capacitance (C_{PIX}). This is particularly useful for thick a-Se photoconductor based pixels where the small intrinsic sensor capacitance requires an additional storage capacitor to be designed in the pixel as discussed in Chapter 2. The work on the fully overlapped architecture process presented in this section has been published in [53][54]. Details on the modeling of dual gate TFTs are provided in [128].

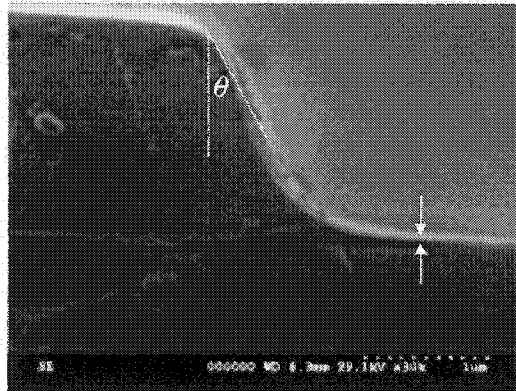
3.3 Low-k interconnect dielectrics

In a-Si TFT active matrix display and imaging arrays, a high aperture ratio or fill factor is essential for improved light transmittance or image quality. One way to achieve a high fill factor is to implement an overlapping pixel architecture where the sensor element is separated from the TFT by an appropriate dielectric [129]. A thick, low dielectric constant (k) material as an inter-level dielectric [130] is necessary to minimize the parasitic capacitances that are a consequence of the vertical stacking. These parasitic capacitances result from overlap of the sensor back electrode and TFT second gate metals as well as overlapping of the back electrode with any other circuit bias lines. Here, the suitability of a photosensitive low-k polymer (PBCB) for integration in a-Si TFT arrays is investigated. Pertinent integration issues to the development of this dielectric such as via opening & descumming, sidewall angle, leakage current, and contact resistance are discussed for different processing conditions.

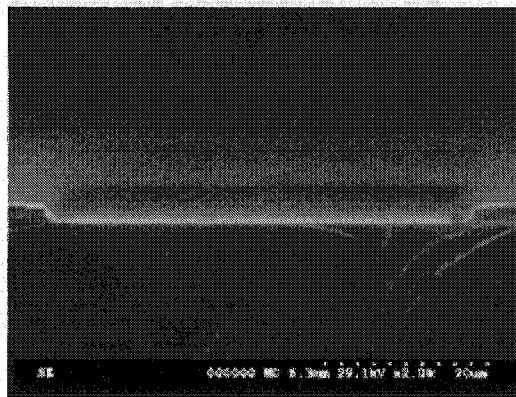
We used either p-type Si or glass (Corning) substrates for the experiments. The PBCB films were spin-coated onto the substrates, UV-illuminated, puddle-developed, and baked. Test structures were fabricated where the PBCB film separates the transistor-level and pixel-level metal pads. Here, glass substrates were first sputtered with 1200Å Mo (or Al) and the metal was patterned using the TFT photomask. PBCB films were then spin coated onto the patterned metal. After a soft bake at $\sim 60^{\circ}\text{C}$ for 2 minutes, the films were subjected to a UV exposure dose of $\sim 10 \text{ mW/cm}^2$ using a via opening photomask. Puddle developing was done after a bake at $\sim 50^{\circ}\text{C}$. The post-develop bake was done at $>70^{\circ}\text{C}$ followed by a hard cure at 260°C in N_2 . For via residue (scum) thickness measurements, PBCB films were spin coated onto Si wafers, UV-exposed for various time durations at $\sim 10 \text{ mW/cm}^2$ using a specially designed array photomask, and then cured at 250°C for 1 hour. To complete via opening, some films were initially wet-etched using an acid-based etchants to remove the residue in the vias. However, in order to develop a better controllable process, a dry-etch process (RIE) is investigated that can overcome the shortcomings of wet etching. For the RIE etching experiments, PBCB films were spin coated onto Si wafers, exposed for 5 s with a UV dose of $\sim 10 \text{ mW/cm}^2$, and then cured at 250°C for 1 hour. Several RIE experiments were performed on a Trion Technology system changing the etch conditions in order to study the etch properties of the polymeric low-k films. An etch gas mix of 20:80 $\text{CF}_4:\text{O}_2$ (10 sccm of CF_4 , 40 sccm of O_2) was used. The top Al metal layer was then e-beam-evaporated, and patterned using the pixel electrode photomask. Finally, electrical measurements were performed.

The via properties of the negative acting PBCB films strongly depend on the exposure time. The sidewall angle in the via increased from 27° to 63° as the exposure time was increased from 5 sec to 180 sec. With longer exposure times, the vias could not be opened. From the experiments shown in Figure 27 and Figure 28 and the results summarized in Table 8, it is observed that an exposure time between 5 and 30 seconds is optimum.

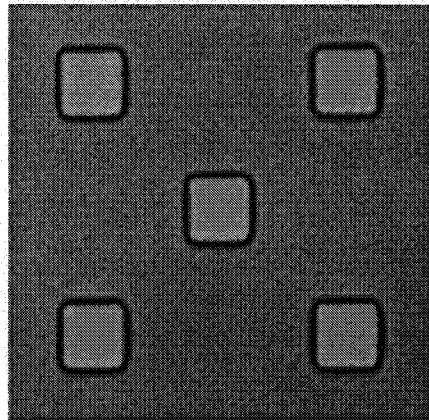
It was necessary to keep the exposure durations short (5 and 30 sec) for acceptable sidewall angles in the via opening. Very large sidewall angles result in opened bottom areas that are very small (see Figure 28(c)). This is probably due to an increased lateral penetration of light. In general however, there is always a residual film left in the vias for all exposure times. Attempts were made to achieve a complete via opening either by an acid-based wet etching, or by dry etching.



(a)



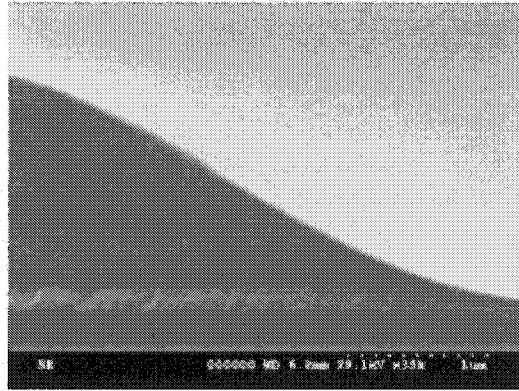
(b)



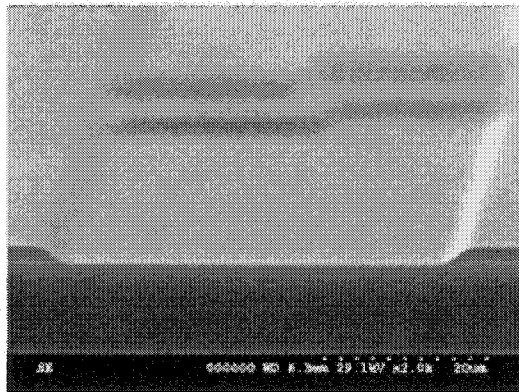
(c)

Figure 27 (a) and (b). SEM pictures of sidewall and complete cross-sectional view. (c)

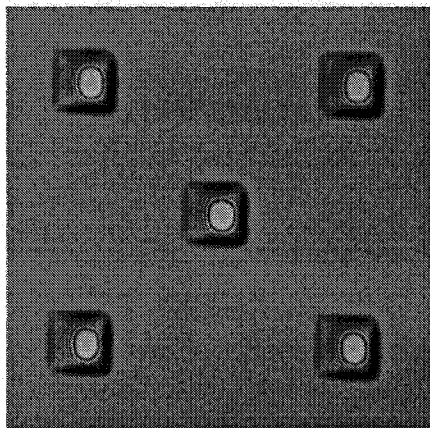
Optical microscope top view of the via. Exposure time 5 sec.



(a)



(b)



(c)

Figure 28 (a) and (b). SEM pictures of sidewall and complete cross-sectional view. (c) Optical microscope top view of the via. Exposure time 3 min.

Table 8. Sidewall angle (deviation from vertical via wall) vs. exposure time (Processing condition: spin at 7000 rpm, develop for 2 min 45s)

Exposure time (s)	Side wall angle (θ)
5s	27°
30s	57°
180s	63°

To determine the depth of the via residue, experiments were carried out on PBCB films coated on Si wafers. The via residue thickness for different UV exposure times is shown in Table 9. It appears that reduced residue thicknesses are obtained for longer exposure times. However, for any prolonged exposure time, it was not possible to completely eliminate the residue. Further, prolonged exposure times result in undesirably shallow sidewalls.

Table 9. Via residue thickness vs. UV exposure time

Exposure time (sec)	Scum thickness (nm)
5	> 150
10	> 150
15	< 50

The removal of the residual film, essential to assure good contact between the top (sensor level) and bottom (transistor level) metallizations, can be achieved by chemically etching it away in a short duration by a wet or a dry etch technique. Though a chemical acid-based wet-etch process can simplify the process [132], there are concerns about protecting the underlying metal (Al or Mo) layer, and therefore process controllability. Less stronger wet etch schemes could not completely eliminate the residual low-k film at the bottom of the vias as shown in Figure 29.

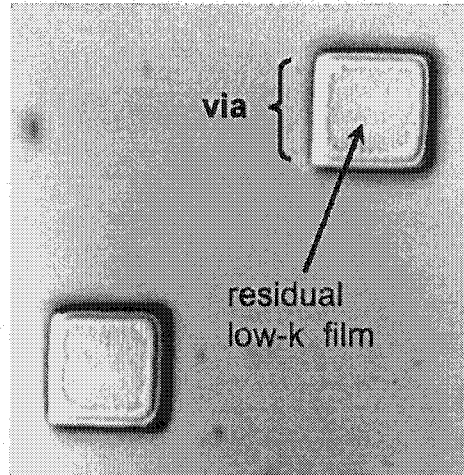


Figure 29. Top view of vias still showing the presence of residual low-k film after an acid-based wet-etch step that followed the UV exposure/development.

In order to avoid the problem of wet-etchants attacking the metal underneath the PBCB layer, dry etching schemes based on RIE were explored. Different process parameters such as RIE power, process pressure and etch duration were looked at in order to study the etching of the low-k film. Figure 30(a) shows the etched thickness of the PBCB film for different etch durations and RIE power at a process pressure of 100 mT. As can be seen from the figure, high power (> 200 W) and long etch duration (> 90 s) are required to etch 150 nm of the PBCB film at 100 mTorr. However, there seems to be a competition between etching and polymerization actions, with the polymerization taking over for prolonged etch durations. For 100 W of RIE power, the etching action is negligible.

When the process pressure is reduced (i.e., to 25 mT) the etching rates are significantly increased as shown in Figure 30(b). As seen here, even a lower power (< 100 W) and small etch duration (< 60 s) resulted in 300 nm of PBCB being etched. This is understandable since the etchant species are expected to be more energetic at lower pressures. It was also observed that for higher pressures, the etching action was negligible and the PBCB film thickness began even to increase at pressures > 200 mTorr and RIE power = 100W. This is most probably due to the polymerization and re-deposition taking over at high pressures and was further confirmed by measuring the resistance across the via-residue in the metal-insulator-metal test devices fabricated after the PBCB layer is exposed to RIE. A resistance started to

show up at high pressures and steadily increased with increasing pressures. After an etching process at 300 mT, a resistance in the 7 M Ω range was measured.

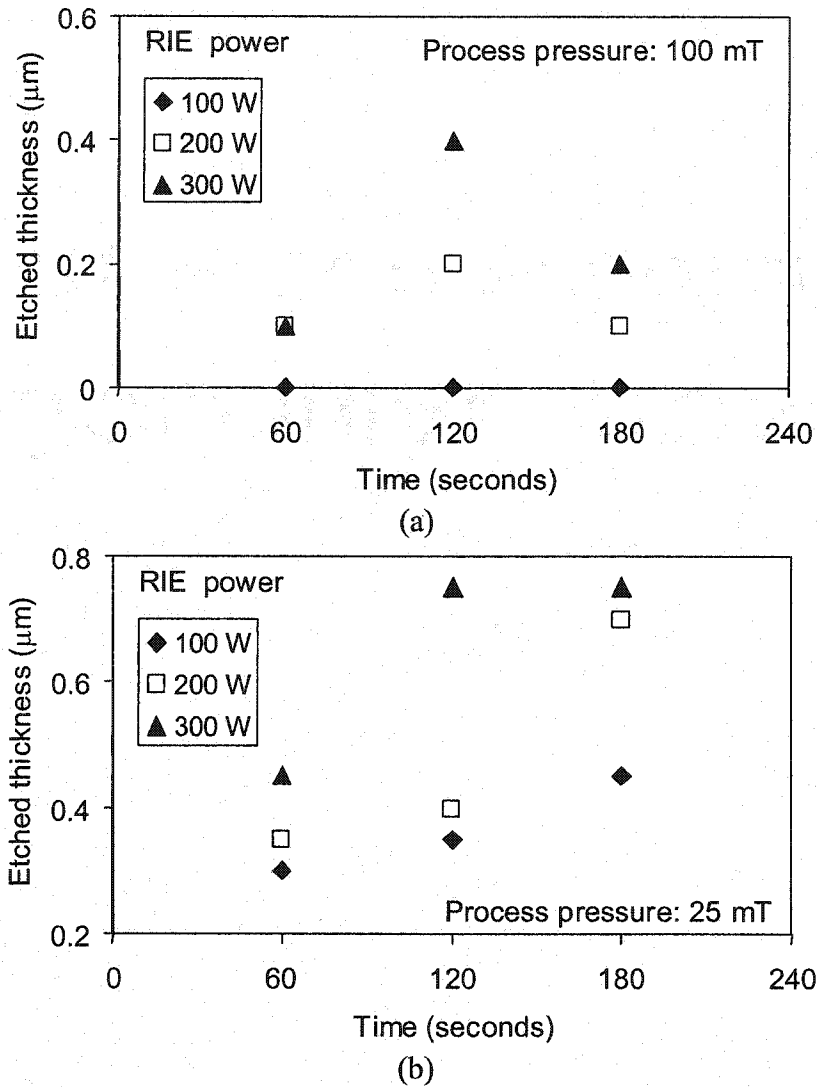


Figure 30. RIE etch-rate of the low-k film for different RIE power and duration: (a) process pressure = 100 mT, (b) process pressure = 25 mT

Figure 31 shows a cross-sectional sketch and a top view die micrograph of array-like test structures. Leakage current between the top and bottom metal levels, as well as the conductivity of the via interconnects was measured on Mo/PBCB/Al and Al/PBCB/Al array-like test structures fabricated on glass substrates. For all films, the leakage current was measured via probes and was less than 10^{-10} A, the measurement limit of the test apparatus. An ohmic I-V was obtained for the via interconnection suggesting good electrical contact.

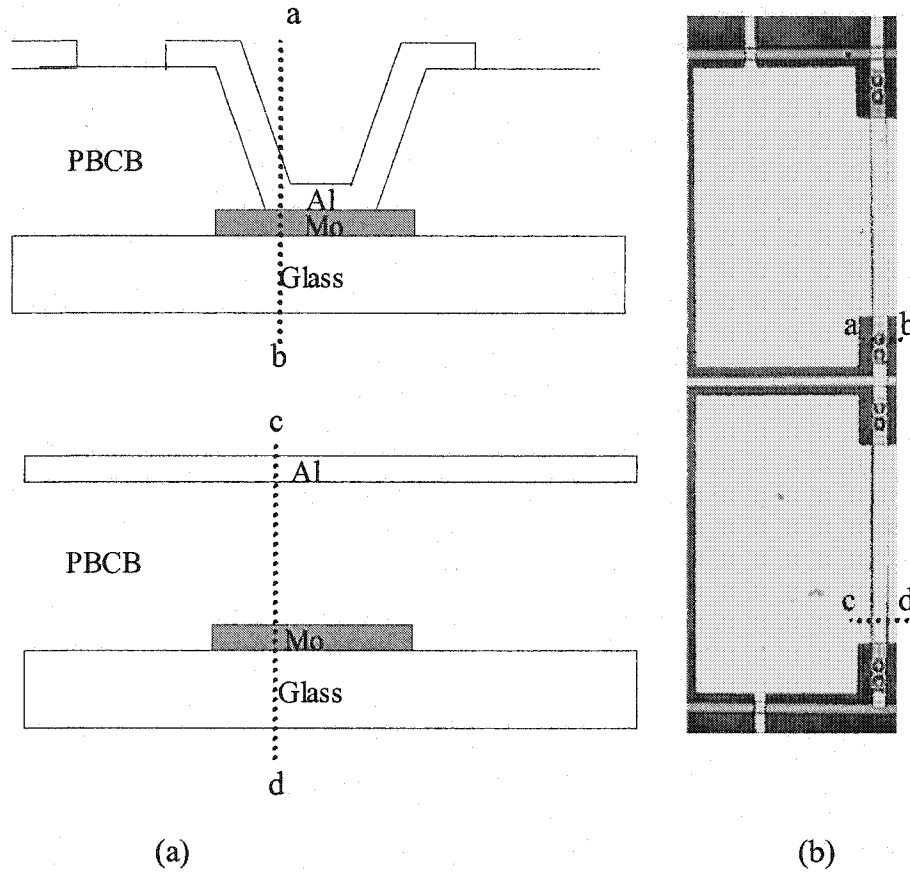


Figure 31. (a) Cross-sectional sketch and (a) Micrographic top view of the array-like test structures

Polymeric PBCB is a promising material for integration as inter-level dielectric in a-Si TFT arrays. Here, k was in the range of 2-3 for processing temperatures between 250°C to 350°C [132]. Since the temperature in a-Si TFT fabrication is generally less than about 300°C, the PBCB films are an excellent choice as a low- k material. A high degree of planarization (>90%) and relatively low film stress suggest that the mechanical integrity of these films is very good. We have designed suitable masks and determined feasible process parameters for PBCB and metal film deposition, via opening, and metal patterning. Conditions have been found to obtain the proper via sidewall angle for good metal contact. Measurements on test structures showed low leakage current ($<10^{-10}$ A) and low resistance for via interconnection. The work presented in this section has been published in [132][133].

3.4 APS array process

3.4.1 Process Conditions

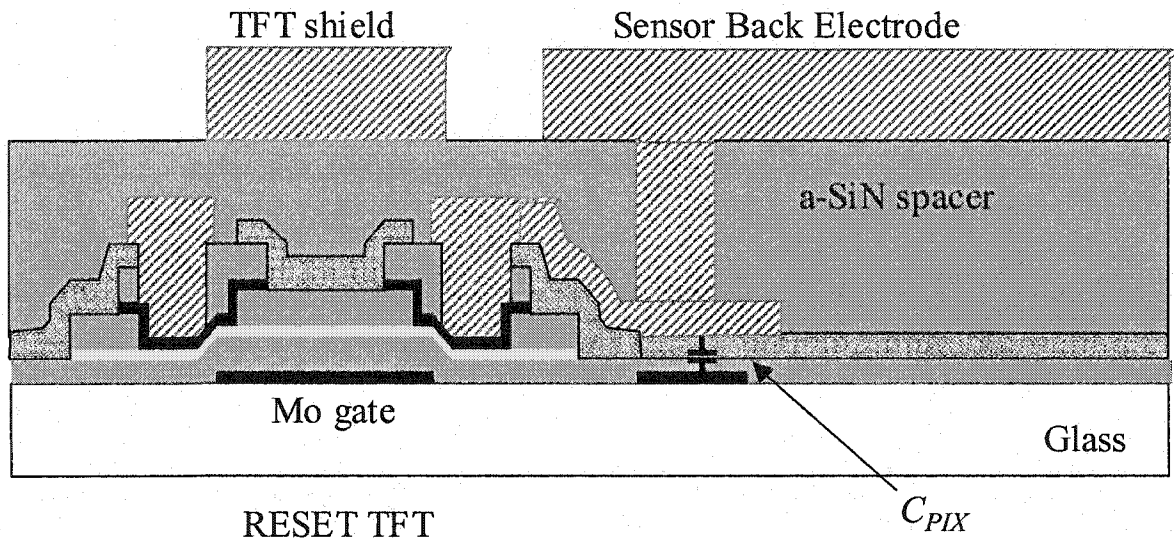
A 2 x 2 a-Si C-APS array was fabricated for integration with an a-Se photoconductor and proof-of-concept. The traditional in-house inverted staggered-electrode TFT structure was used incorporated with SCTFT modifications and the additional a-SiN reliability layer mentioned previously. The SCTFT structure was used partly because of reliability but mainly because the TFTs would undergo further high temperature processing for sensor integration even after the source-drain metallization. It was noticed that temperature annealing of conventional layout TFTs resulted in a substantial increase in their leakage currents (from pA to nA). The reason for increased TFT leakage current at annealing temperatures of 180°C is thought to be due to the Al source/drain metal contact spiking through the thin n^+ a-Si contact layer directly to the a-Si channel above the gate metal. Similar temperature annealing experiments with SCTFT structures where the source-drain metallization is offset from the gate metal and a-Si channel yielded consistent TFT leakage performance (in pA) even after 20 hours of annealing at 180°C.

The complexity of the APS pixel readout circuit (as compared to a traditional PPS pixel) results in an increased number of interconnects at both gate and drain/source metal levels. The extra interconnects increase metal line overlaps and parasitic capacitances and the additional a-Si:N layer (described in section 3.1) was deposited between the gate and source/drain metals to decrease the additional parasitic capacitances.

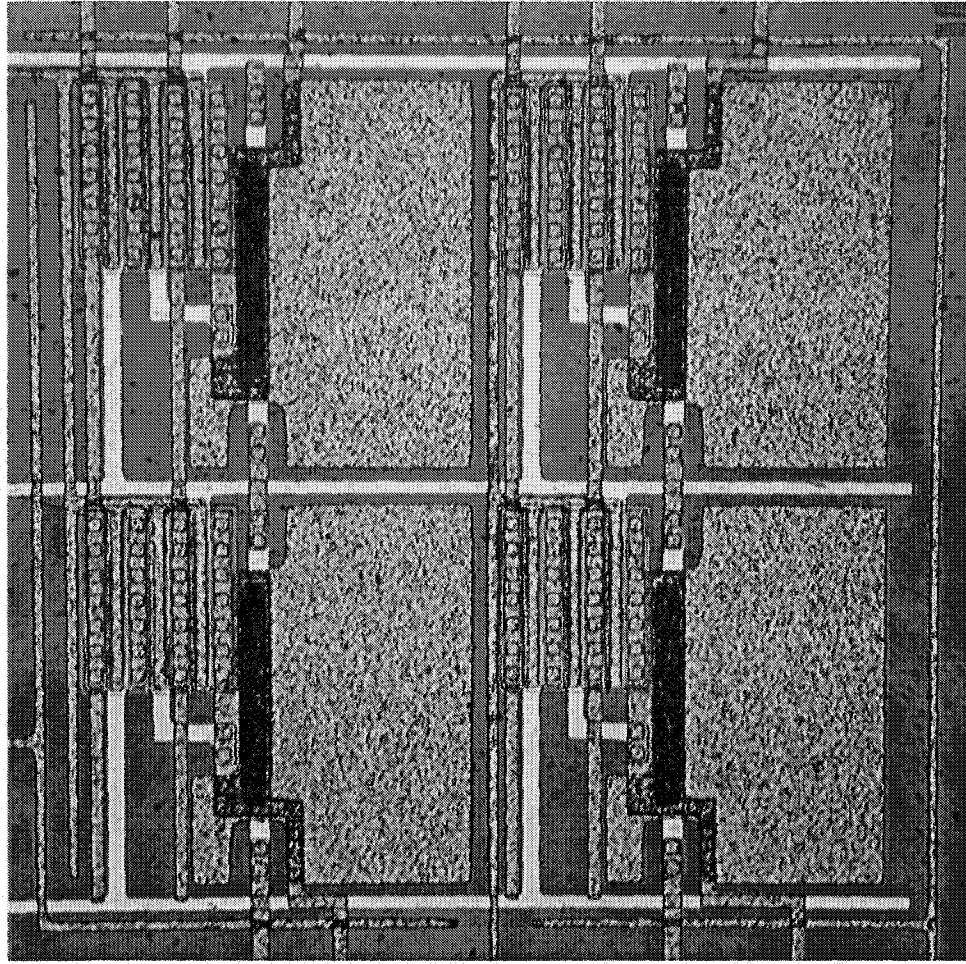
Two additional films (a 260°C a-Si:N spacer and a secondary Al metallization) were deposited in order to get the pixels in a form compatible for integration with an a-Se photoconductor. First, a dielectric film (750 nm of a-Si:N) was deposited between the TFT and the top metallization. Then a via was etched and the TFT array was completed with a final Al metal deposition and patterning. The final Al metal was designed to provide a back electrode to the a-Se photoconductor. In addition, it was patterned to form metal shields over TFT gates to prevent an increase in leakage during array operation due to charge buildup at the bottom of the a-Se layer. The resulting cross-section is shown in Figure 32 (a). The main reason a non-overlapped pixel architecture process was chosen over the fully overlapped one

is because the low-k dielectric process was not fully developed at the time of array fabrication. Hence, to minimize parasitic capacitances that result because of the smaller a-SiN film thickness, the non-overlapped process was chosen to demonstrate proof-of-concept for the a-Si C-APS readout circuit array.

The figure below shows the RESET TFT cross-section in an APS array pixel fabricated using the above process as well as a micrograph of the fabricated array. The following table (where PAN stands for a mixture of (Phosphoric, Acetic and Nitric Acid), BHF is Buffered Hydrofluoric Acid and KOH stands for Potassium Hydroxide) outlines the process flow along with the film thickness and conditions used during fabrication. The array mask set, along with initial V-APS pixel and C-APS pixel mask sets is shown in Appendix D.



(a)



(b)

Figure 32. (a) Pixel Cross-section (b) Fabricated 2 x 2 C-APS array

An alternate method of developing the C-APS pixel TFT array is possible by modifying the layout of a five mask TFT process. Here, the second gate may be patterned on the same layer as the TFT drain/source metal via mask 5 [128]. The five-mask method was not used due to lithographic constraints where the dual gate TFT consumes more area in the five mask process since the top gate is on the same layer as the TFT drain and source metals. Some of the results related to the development of the a-Si TFT based APS imager have been accepted in [58].

Table 10. Process conditions for 260°C a-Si TFTs used in a C-APS array.

Process Sequence	Deposition						Etch	
	System	Temp (°C)	Gases / Target (sccm)	Pressure (mTorr)	Power (W)	~ Thick. (nm)	Mask #	Solution
1) Gate metallization	Sputter	RT	Mo	5	400	110		
2) Gate metal etch							1	PAN*
3) Trilayer deposition:	PECVD							
Gate SiN _x		260	4 SiH ₄ 80 NH ₃ 80 N ₂	400	150	300		
a-Si		260	80 Si H ₄	250	12	50		
Top SiN _x		260	4 SiH ₄ 80 NH ₃ 80 N ₂	400	110	250		
4) Top SiN _x etch							2	BHF**
5) Quick HF dip								BHF**
6) Bilayer deposition:	PECVD							
n ⁺ a-Si		260	1%PH ₃ /SiH ₄	150	12	100		
Passivation SiN _x		260	4 SiH ₄ 80 NH ₃ 80 N ₂	400	110	300		
7) Passivation SiN _x etch							3	BHF**
8) KOH etch								KOH***
9) Passivation SiN _x		260	4 SiH ₄ 80 NH ₃ 80 N ₂	400	110	200		
10) Via SiN _x etch							4	BHF**
11) TFT Drain/Source metallization	Sputter	RT	Al	5	400	500		
12) Metal etch							5	PAN*
13) Passivation SiN _x		260	4 SiH ₄ 80 NH ₃ 80 N ₂	400	110	750		
14) Via SiN _x etch							6	BHF**
15) Pixel electrode metallization	Sputter	RT	Al	5	400	1000		
16) Metal etch							7	PAN*

Since fabrication, particularly using a wet-etch process, is highly dependent on operator skill, the inter-wafer yield was moderate. However, from devices tested on successfully fabricated wafers, the yield was found to be around 90%. Here the TFT ON currents in the linear mode of operation were measured via a probe station for $V_{DS} = 5$ V and $V_{GS} = 30$ V. The results were normalized to the average of 20 samples and are shown in Figure 33 below. Note that edge columns and rows were neglected and the maximum variation in ON currents is about 10% in the lower right hand corner of the wafer.

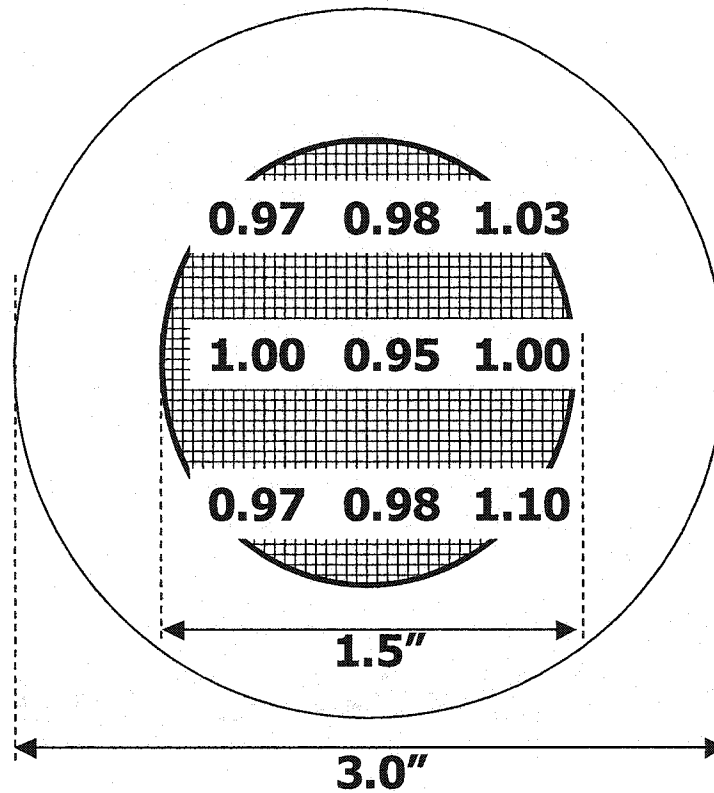


Figure 33. Normalized TFT ON current variation over the wafer.

3.4.2 Design Rules

The device structure used for this work was the inverted staggered-electrode device structure. A fully wet etch 260°C process was used using five photolithographic masks for the TFT definition. Some general design rules for array layout are given below for the wet-etch TFT process used. One of the factors limiting the minimum channel length is the in-

house emulsion mask creation process where the transition between light and dark fields is blurry in contrast to commercial chrome-on-glass masks. Thus, the array design rules take both the lithographic process constraints and emulsion mask limitations into consideration.

The first critical parameter is the gate and source/drain contact overlap (OV_{1-2} in Figure 34), which plays an important role in determining the TFT ON current. Generally, a 2 μm overlap was sufficient for the 2 mm APS array. The second critical step is the gap between the TFT source and drain on the bi-layer nitride (L_{MIN}). In the array process, a minimum gap of 13 μm was used because too small a gap would fail to permit proper TFT source and drain isolation. The last critical parameter is the overlap of the bi-layer step nitride with the top nitride from the tri-layer step (OV_{2-3}). This is particularly important because the overlap protects the a-Si channel from getting destroyed by the KOH etchant during the source/drain and TFT isolation step. A 4 μm overlap amply accounted for emulsion mask and mask alignment errors including slight over-etching. For the rest of the array, a minimum dimension of 15 μm was used for Mo (120 nm thickness) and 20 μm for Al metal (> 500 nm thickness) interconnect. Lastly, at least 13 μm square vias were used throughout the array for all TFT contacts.

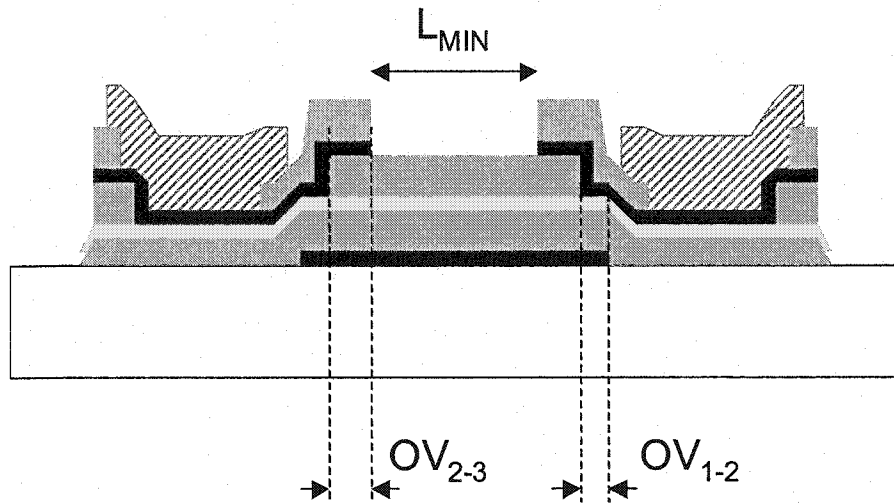


Figure 34. Critical dimensions in the in-house TFT fabrication process

3.5 Considerations for large area APS imaging arrays

3.5.1 Low leakage TFTs

A low leakage current is one of the major requirements for large area imaging arrays. A low leakage RESET TFT minimizes corruption of the signal at the pixel integration node while the low leakage READ TFT minimizes error during readout. Note that during readout, only one READ TFT is ON while the rest of the column READ TFTs are OFF. If their cumulative leakage is high, the output current of the operating READ TFT may be corrupted. Top passivated amorphous silicon TFTs are particularly suited for low leakage applications because currents as low as sub fA have been reported [6] for them.

3.5.2 Process uniformity

The requirement of uniformity stems from the large area application of amorphous silicon arrays. Unlike crystalline or polycrystalline silicon, amorphous silicon TFT deposition is relatively uniform over a large area. For our in-house process, the TFT ON current variation in linear mode was less than 10% over a 4 cm square area. One manner of reducing the effect of process non-uniformities involves designing robust circuits. For example, the C-APS has inherent feedback due to the READ TFT (discussed in Chapter 4) that allows the circuit's g_m to stay relatively constant even for comparatively large variations in V_T .

In addition, using an n^+ a-Si:H contact layer where a larger series resistance (R_S and R_D) exists from the drain and source contacts to the channel, incorporates local feedback in the TFT. As shown in section 3.1, the effect of channel length modulation (that introduces a second order non-linearity in the TFT's saturation current) is almost eliminated for TFTs with large R_S and R_D . However, there is a tradeoff in that the large R_S and R_D also reduce TFT ON current and hence TFT g_m .

3.5.3 TFT reliability

Errors in array fabrication are mostly associated with TFT fabrication since the overlying a-Se photoconductor and associated Al contact do not undergo any form of lithography or etching. For the TFT, as discussed previously, some of the more common faults include

gate/drain, gate/source and source/drain shorts. Using a SCTFT like architecture, the likelihood of all of the above faults is greatly reduced because of the increased separation between the source, gate and drain metallizations. The likelihood of open faults can be reduced by using thick interconnects and proper layout can ensure that a faulty pixel does not affect the entire imaging array column.

3.5.4 Fully overlapped architecture

For the C-APS imaging array with three TFTs per pixel, a high fill factor is essential for high image quality and resolution. The fully overlapping pixel architecture presented in a previous section is capable of accomplishing this task provided the parasitic capacitances that result from the proximity of the top gate to the sensor back electrode are minimized. If the parasitics are not minimized, C_{PIX} must be increased to avoid any adverse feedthrough effects and a larger C_{PIX} implies lower charge gain and higher reset noise (APS noise properties are discussed in Chapter 5). Thus, reducing parasitic capacitances mandates the use of a thick, low dielectric constant (k) material as an inter-level dielectric. The photosensitive low- k polymer (PBCB) presented in this chapter is amenable for integration in a-Si TFT arrays.

3.5.5 Process Scaling

While the fabricated APS pixels demonstrate promising charge and voltage gain results, a larger g_m is even more beneficial for improving SNR. To achieve a charge gain of 30 for a fixed integration time of 33 μ s in real-time fluoroscopy, the TFT process must provide a C_{PIX} of 0.75 pF and a g_m of 0.68 μ S. The goal of $G_i = 30$ is challenging with the current in-house 25 μ m channel length a-Si process since the large features cause a corresponding increase in parasitic capacitance. Also, the 25 μ m TFT channel length in the current in-house process implies a larger pixel area is required which is in conflict with the fluoroscopic pixel pitch requirement of 250 μ m.

In contrast, if a state-of-the-art industry process [6] is used where smaller channel lengths are possible, the goals of $C_{PIX} = 0.75$ pF and a $g_m = 0.68$ μ S are readily achievable. The table below highlights some improvements in the C-APS performance due to process scaling via

in-house TFT simulations. Ideally, an even larger charge gain of 66 (an SNR of 6.6) is possible if the circuit is designed to have a $g_m = 1 \mu\text{S}$ and a $C_{PIX} = 0.5 \text{ pF}$.

Table 11. Scaling effects on C-APS performance

	18 μm a-Si TFT process (implemented)	5 μm state-of-the-art a-Si TFT process (projected)
Parameters	(W/L) _{RESET} = 60/25 (W/L) _{AMP} = 150/25 (W/L) _{READ} = 150/25	(W/L) _{RESET} = 40/5 (W/L) _{AMP} = 100/5 (W/L) _{READ} = 100/5
Supply Voltage	6 V	6 V
Pixel capacitance	1 pF	1 pF
Feedback capacitance	10 pF	10 pF
Reset ($C_{PIX} = 1 \text{ pF}$)	< 30 μs	< 3 μs
Readout	30 μs	30 μs
Charge Gain	> 10	> 30
Voltage Gain	> 1	> 3
Pixel area	250 x 250 μm^2	125 x 125 μm^2

Chapter 4. Circuit

Metastability

Unlike crystalline silicon transistors, a-Si TFTs exhibit bias induced metastability phenomena that have an adverse effect on circuit performance when the circuit is improperly designed or operated. The metastability concerns become particularly important when the TFT is used as an analog device. In contrast to traditional applications (e.g. in LCDs) where the TFT is used as a switch, analog applications can require the device to withstand prolonged voltages on both, drain and gate terminals. This chapter attempts to develop an understanding of circuit performance when both dc and pulse bias voltages are applied at the TFT terminals.

This chapter begins by providing a brief background on the common theories for metastability in a-Si TFTs. Next, experiments for constant and pulse bias stress on in-house fabricated a-Si TFTs are presented and a threshold voltage shift (ΔV_T) model is developed to predict the long-term performance of APS arrays. The stability analysis of a-Si TFTs is necessary to predict the long-term performance of a-Si APS arrays where the TFT metastability affects the C-APS gain by shifting the V_T of various TFTs in the circuit. To this effect, the developed ΔV_T model is used with C-APS circuit equations to model gain degradation and compared to C-APS circuit stability measurements. The gain degradation model is then extended to predict the performance of a typical a-Si C-APS pixel over 10,000 hours where the lifetime variation in gain is found to be less than 5%.

4.1 Background

4.1.1 Metastability mechanisms

Studies of a-Si TFTs have concluded that two mechanisms can explain the electrical instability [67][90]. The first is carrier trapping in the gate insulator which occurs primarily in PECVD a-Si:N gate insulator TFTs where the high density of defects in the insulator can trap charge when the TFT gate undergoes bias stress. Injection of electrons into the insulator layer of a-Si TFTs has long been known to cause ΔV_T . Electrons are first trapped within the localized interfacial states at the a-Si/a-SiN boundary and then thermalize to deeper energy states inside the a-SiN layer either by variable-range hopping [67] or through a multiple-trapping and emission process [70][76][75]. The broad distribution of energies for the trapping levels within the a-SiN layer leads to two kinds of electron trapping behavior [76].

The first is due to interfacial traps with fast re-emission times (or fast states). These traps were found to cause a hysteresis in the I_{DS} - V_{GS} behavior of TFTs [69][70][73]. The density of these fast states decreases when the optical band gap of the nitride layer is increased. Moreover, the optical band gap of the nitride was found to increase when the nitrogen content of the layer was increased [69] [73]. Nitrogen-rich nitrides are generally obtained by using a higher ratio of NH_3/SiH_4 (~ 10) during PECVD deposition.

The second nitride related degradation effect is due to interfacial and bulk traps with slow re-emission times (slow states). These traps cause a metastable increase in the threshold voltage [67][73][74][75][76]. However, the number of these deep traps was found to decrease for wider bandgap, nitrogen rich, a-SiN layers [69]. As such, using nitrogen-rich a-SiN has become prevalent for TFTs since it improves the reliability and reduces degradation associated with both slow and fast states in the gate insulator. The in-house TFT fabrication process uses a ratio of $\text{NH}_3/\text{SiH}_4 \sim 20$ for the a-SiN films to achieve good metastability characteristics.

The second mechanism related to metastability is point defect creation in the a-Si layer or at the a-Si/SiN interface that increases the density of deep-gap states [72]. When a positive gate bias causes electrons to accumulate and form a channel at the a-SiN/a-Si interface, a

large number of these induced electrons reside in conduction band tail states as noted in Appendix A. These tail states have been identified as weak silicon-silicon bonds which, when occupied by electrons, can break to form silicon dangling-bonds (deep state defects) [71][77]. Deep state defect creation forms the basis of the defect pool model [72] which has some similarities to the Staebler-Wronski effect [78] in which photo-generated carriers result in the generation of dangling bonds [79]. In the defect pool model, the rate of creation of dangling bonds is a function of ϕ , the barrier to defect formation, the number of electrons in the tail states and the density of the weak bond sites [72]. The metastable increase in the density of deep defect states is shown in the figure below. The location of these newly created defect states in the gap depends on the polarity of the applied stress bias and in some cases, can cause the V_T of the TFT to shift [72][80].

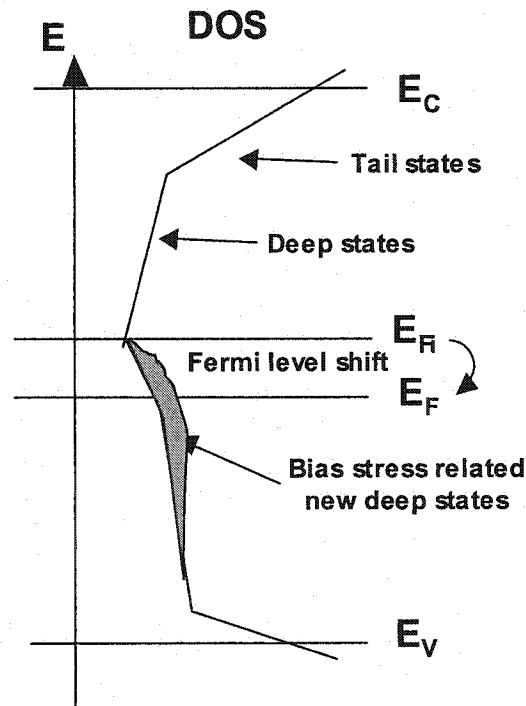


Figure 35. Bias-induced metastable defect states in a-Si TFTs (adapted from [72]). Note that most of the states are below E_F near that valence band.

The charge trapping and defect state creation mechanisms distinguish themselves from each other (for TFTs with an a-Si:N gate insulator) in that charge trapping in the nitride has

been observed to occur at high gate bias voltages and long stress times. Here, the shift in the threshold voltage can be positive or negative depending on the polarity of the trapped charge (electron or hole). In contrast, defect state creation dominates at lower stress voltages and at smaller stress times. At small stress voltages, Powell showed that while state creation in the lower part of the gap dominated at positive biases, state removal from the lower part of the gap occurred for negative bias voltages [72].

Powell distinguished between defect state creation and charge trapping in 1987 by experimenting with ambipolar TFTs [87]. If charge is trapped in the nitride under positive bias stress, the V_T for both electron and hole conduction will shift to more positive values. In contrast, defect state creation in the a-Si layer manifests itself by the V_T becoming more negative for hole conduction and more positive for electron conduction since the Fermi level has to move through the newly created states to establish the channel. Powell showed that for his TFTs, state creation was the dominant mechanism up until 50 V [72] and charge trapping became significant thereafter. The critical voltage at which charge trapping overtakes state creation depends on the bandgap of the a-Si:N gate insulator, which also supports the theory that the charge trapping process is nitride related [68]. The defect creation process appeared to be independent of the nitride characteristics, implying that state creation takes place in the a-Si film [67].

Powell determined that state creation is characterized by a power law time dependence and is strongly affected by temperature. Charge trapping, on the other hand, has a logarithmic time dependence and is weakly dependent on temperature. A logarithmic time dependence and temperature independence is generally observed for charge trapping in an insulator where the injection current depends exponentially on the density of previously injected charge and the charge is trapped near the gate insulator interface [89] [90]. As noted before, the process of state creation observed in a-Si film was reported to have several features in common with observations of state creation through illumination or thermal equilibration. One proposed model is that Si dangling bonds are created by breaking weak Si-Si bonds, which are then stabilized by the dispersive diffusion of hydrogen [11]. The power law time dependence is found to be consistent with a defect creation model [88].

The subthreshold slope in the transfer characteristics of n-channel transistors does not change after positive bias stress confirming the location of the newly created states below the

flat-band Fermi level (see Figure 35). This is consistent with the idea that the created states are Si dangling bonds or deep state defects. The process of creating states below the flat-band Fermi level shifts the Fermi level nearer to midgap, which accounts for the increase in threshold voltage.

For negative biases, there are a few newly created states located above the flat-band Fermi level in addition to state removal in the lower part of the gap. This explains why there is some sub-threshold slope degradation in n-channel TFTs during negative bias stress. For imaging applications using n-channel a-Si TFTs, TFT OFF voltages are chosen primarily by the requirement of low leakage current as explained later on in this chapter. The magnitude of typical TFT OFF voltages ranges from 0 to -5 V implying subthreshold slope degradation will be minimal. Therefore, although a-Si TFT metastability comprises both, ΔV_T and subthreshold slope degradation, the focus in this chapter is on ΔV_T management.

4.1.2 Literature models for ΔV_T

Modeling the two ΔV_T mechanisms is summarized as follows: defect state creation is characterized by a power law dependence of ΔV_T over time, i.e. $\Delta V_T \propto t^\beta$. Both Powell and Jackson [87][90] claimed that their data mapped a relationship,

$$\Delta V_T(t) = A(V_{ST} - V_{Ti})^\alpha t^\beta \quad (1)$$

for the defect state creation mechanism where α takes on a value of unity and V_{Ti} is the V_T before stress is applied. In contrast, charge trapping was associated with a logarithmic time dependence [88], which can be represented as,

$$\Delta V_T(t) = r_d \log(1 + t/t_0) \quad (2)$$

where r_d is a constant and t_0 is some characteristic value for time.

On the other hand, Kanicki [70] reported an empirical stretched-exponential function could describe the stress-time and stress-voltage dependence of V_T in a-Si TFTs irrespective of the ΔV_T mechanism,

$$V_T(t) = (V_{ST} - V_{Ti}) [1 - \exp(-(t/\tau)^\beta)] \quad (3)$$

where τ is some characteristic extractable time constant, and β is the stretched-exponential exponent which is temperature dependent. For a short effective stress time ($t \ll \tau$), the above function can be simplified to a form similar to eqn. (1),

$$\Delta V_T(t) = (V_{ST} - V_{Ti}) \tau^{-\beta} t^\beta = A(V_{ST} - V_{Ti})^\alpha t^\beta. \quad (4)$$

The main difference is that Kanicki extracts non-unity values for α making the function empirical. Our results, as will be seen in the following sections, appear to be in concord with Powell's theory in that we noticed a unity value for α for the range of positive stress voltages applied as well as a power law time dependence for the ΔV_T .

4.1.3 Experimental Setup

The a-Si TFTs used in the experiment are of the bottom gate, inverted staggered variety described in the previous fabrication chapter. The samples were annealed at 180°C for 3 hours and cooled for 3 hours before each bias stress measurement to restore the initial TFT transfer characteristics. Note that the rate at which the annealing oven was heated up and cooled down was kept constant for all experiments in order to preserve measurement consistency.

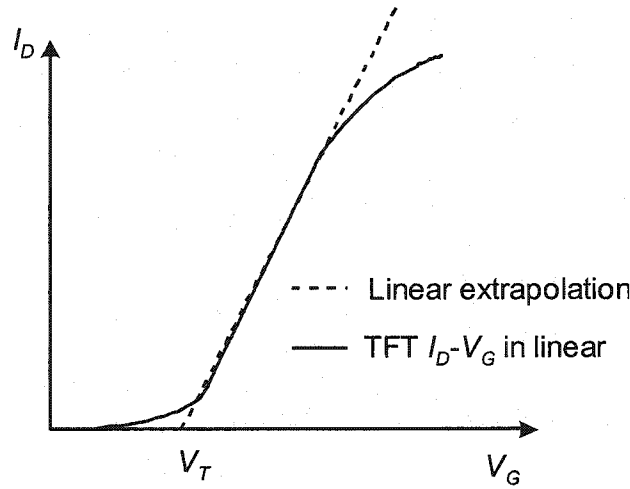
Keithley SMU parameter analyzers were used to extract TFT transfer characteristics every half hour between the applied stress bias. In the case of DC bias stress measurements, the Keithley SMU was also used to apply the stress voltage. For pulse bias stress measurements, an external HP pulse generator was interfaced to the TFT via an Analog Devices AD506 analog multiplexer. Access to the TFT gate was shared between the Keithley parameter analyzer and the HP pulse generator via the multiplexer. The test setup is shown below in Figure 36. To improve confidence in the experiments, all the tests were performed on two TFT devices.

Transfer characteristics ($I_D - V_G$) at V_D at 0.5 V were extracted every 90 minutes for $-4 V < V_G < 6 V$ with a resolution of 0.5 V/step using the fast electrometer setting on the Keithley SMUs. Extracting the transfer characteristics quickly is particularly important for negative bias experiments where the positive bias applied for the $I_D - V_G$ measurement can corrupt the ΔV_T measurement. In order to prevent the $I_D - V_G$ measurement from corrupting the negative

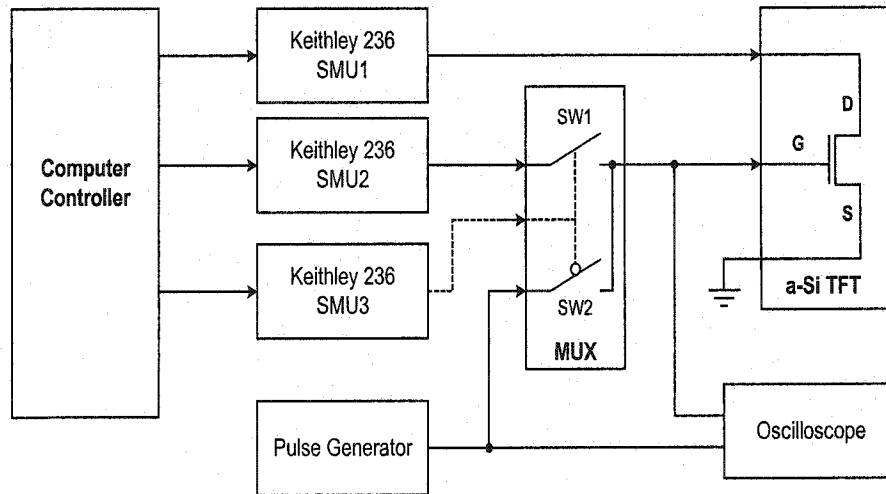
bias related ΔV_T measurement, the TFT's $I_D - V_G$ was measured every 180 minutes for most negative bias experiments at the cost of fewer data points.

The measured TFT transfer characteristics were then used to extract the TFT V_T in the linear region. The V_T extraction procedure in the linear region is reviewed in Appendix C. The primary reason for using the linear method of extraction was that it provided a value for V_T over stress time that was unaffected by stress bias related changes in the α parameter of the I_{DS} saturation equation and hence, measurement and ΔV_T extraction simplicity.

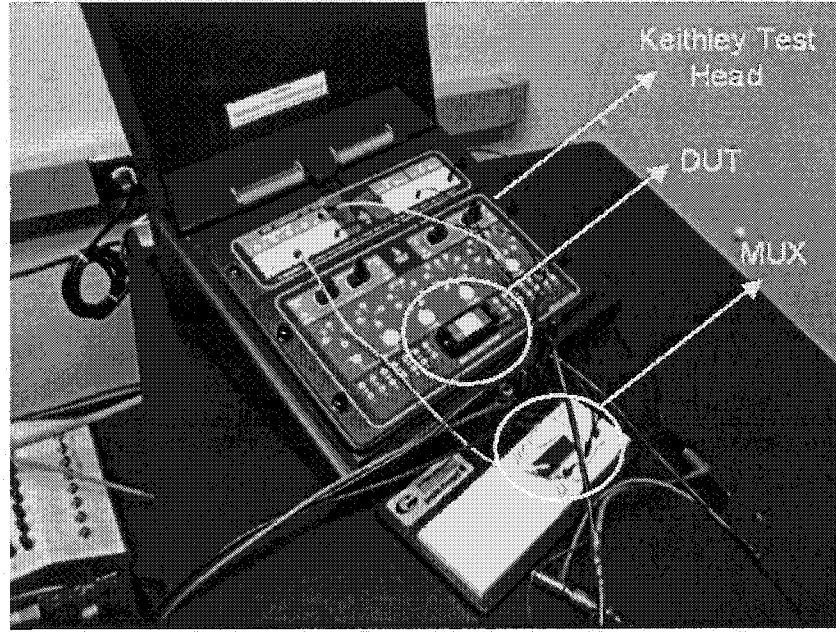
The extraction procedure is shown in the figure below along with the measurement setup used for all of the metastability experiments. A photograph of the measurement setup in the lab is also included in the following figure.



(a)



(b)



(c)

Figure 36. (a) V_T Extraction procedure and, (b) ΔV_T measurement setup for different DC and pulse biases, frequencies, and duty cycles. For DC measurements, the pulse generator and MUX were disconnected.

4.2 TFT Metastability at DC bias values

Figure 37 shows the overall ΔV_T behavior plotted against various gate stress voltages applied during the experiment. Here, the ΔV_T increases for positive stress voltages, and decreases for negative voltages. Note that for identical stress times, an equivalent decrease in the magnitude of ΔV_T appears at much larger negative stress voltages as compared to the increase in ΔV_T at positive gate stress voltages. For positive stress voltages, some authors have claimed ΔV_T is solely due to charge trapping while others have suggested that both, defect state creation and charge trapping co-exist. For the range of negative voltages in Figure 37, Powell [81][82][83] described the small decrease in ΔV_T as a property of the a-SiN/a-Si interface where state creation and reduction mechanisms are occurring simultaneously. The mechanism (reduction or creation) that dominates is a consequence of the type of nitride used as well as the interface.

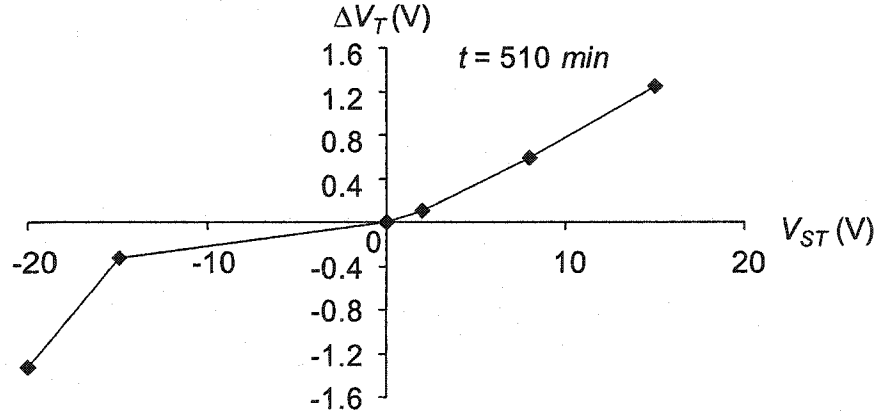


Figure 37. ΔV_T as a function of TFT stress voltage, V_{ST} . V_{ST} was applied to the gate of the TFT for a stress time, T_{ST} , of 510 minutes.

Figure 38 shows the change in TFT I_{DS} - V_G characteristics for positive and negative gate bias stress voltages. Here, although V_T changes significantly for both positive and negative gate bias stress, the subthreshold slopes stay relatively constant. However, there is a slight change in subthreshold slope for the negative stress that is not present in the positive bias stress measurements.

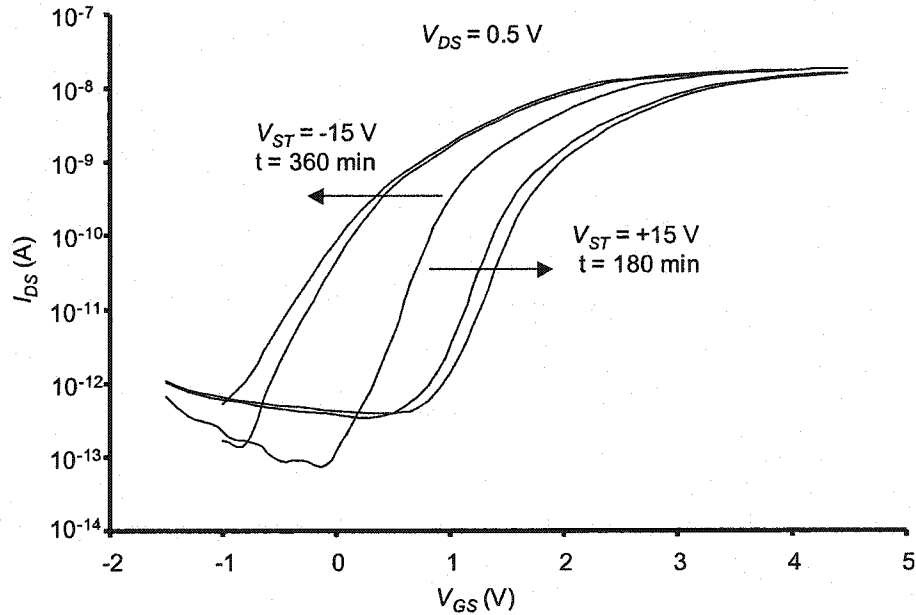


Figure 38. Effect of prolonged gate bias on I_{DS} - V_{GS} characteristics

4.2.1 Positive DC bias stress

As shown in Figure 39(a), if ΔV_T is plotted against $V_{ST} - V_{Ti}$, ΔV_T is proportional to $V_{ST} - V_{Ti}$ for positive voltages. The unity value for α is in concord with the defect creation model. The relationship of the ΔV_T as a function of time for positive stress voltages is shown in Figure 39(b). Here, the value of the time exponent, β_I (shown as β in the figure), is extracted to be around 0.3 for the range of measured stress voltages. To quantify, the $\Delta V_T = A(V_{ST} - V_{Ti})t^{\beta_I}$ relation can be fit to the positive stress data with, $\alpha = 1$, $\beta_I = 0.3$ and $A = 0.0115$ yielding an error of less than 5%.

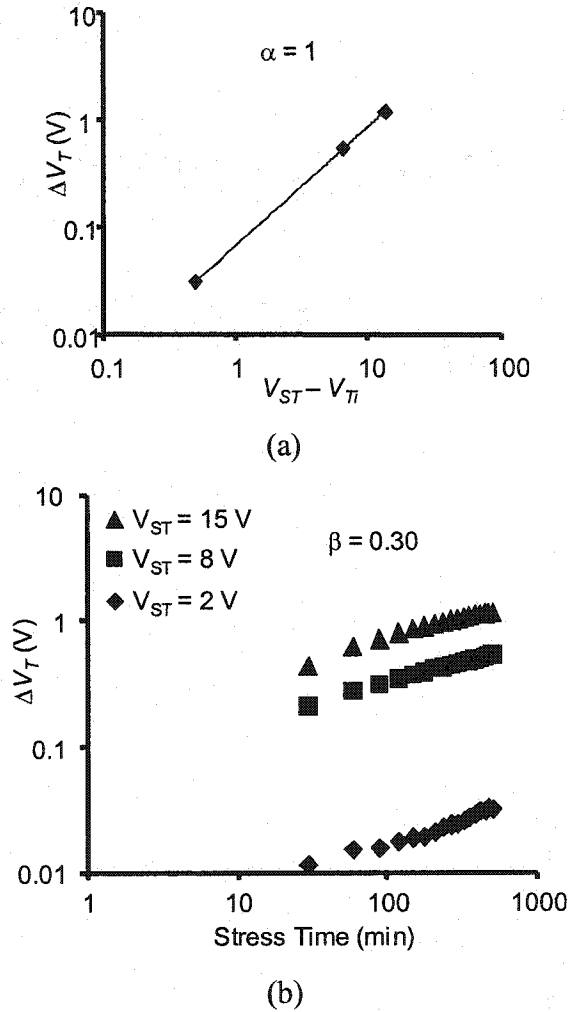


Figure 39. α (measured at $t = 600$ min) and β values for positive DC bias values.

4.2.2 Negative DC bias stress

In contrast to positive stress voltage measurements, the relationship between the measured data and theory is not evident for negative voltages and much of the work done in this area relies on empirical models [86][94]. If the ΔV_T data for negative stress voltages is plotted with respect to gate stress voltage, V_{ST} , we notice a value of around 2.49 for the term α as shown in Figure 40(a). Similarly, plotting against time yields a 0.28 value for the time power dependence, β_2 (shown as β in Figure 40(b)) where ΔV_T is increasing in the negative direction.

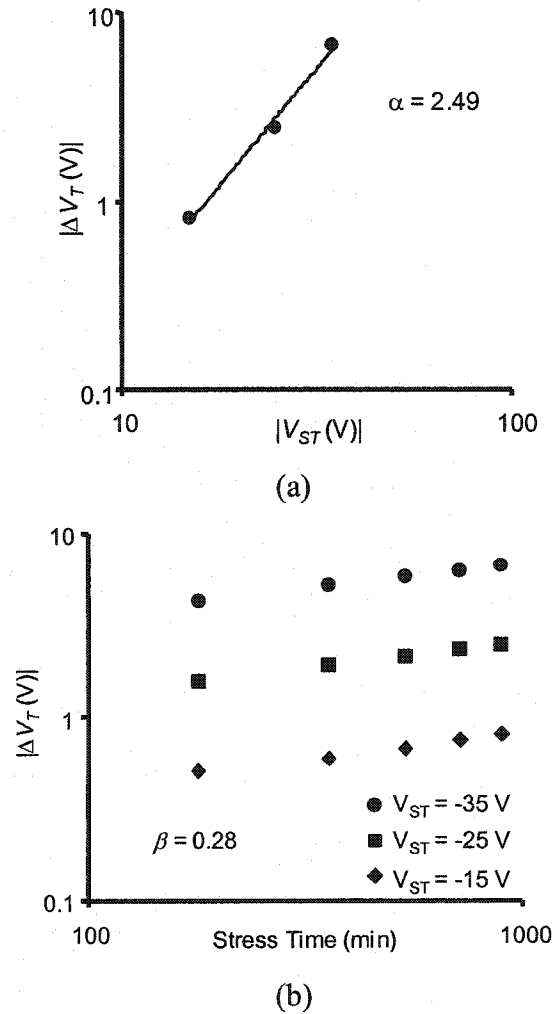


Figure 40. (a) α and (b) β values for negative DC bias stress voltages.

Powell claimed that defect state reduction is responsible for the ΔV_T at low negative voltages but there might be some charge trapping effects as the stress voltage becomes more negative. With respect to the results in Figure 40, it is challenging to confirm the dominant ΔV_T mechanism for negative bias stress on the in-house TFTs. However, ΔV_T appears to have a power law dependence on both gate bias and stress time. To quantify empirically, a $\Delta V_T = -B |V_{ST}|^\alpha t^{\beta_2}$ relation is fit to the negative stress data with $\alpha = 2.49$, $\beta_2 = 0.28$, and $B = 0.12 \times 10^{-3}$ that yields an error of less than 5% for the range of voltages tested. The table below shows values for α and β published by various international researchers for a-Si TFTs over the last decade. Evidently, the values extracted from in-house TFTs for both, positive and negative gate bias stress, are in agreement with some of the previously reported results.

Table 12. α and β values extracted by various researchers for a-Si TFT ΔV_T .

<i>Positive bias stress</i>	α	β
In-house	1	0.30
Powell [88]	1	0.45 (at 40°C)
Libsch [70]	1	0.25
Kanicki [86]	1.9	0.50
<i>Negative bias stress</i>		
In-house	2.5	0.28
Kanicki [86]	2.4	0.32
Tsukada [94]	3.8	0.25

4.2.3 DC bias stress on the TFT drain

4.2.3.1 Positive gate bias

TFTs used in non-switch applications often have a drain bias in addition to a gate bias (i.e. when used as amplifiers or active loads). The presence of a drain bias on the TFT changes the ΔV_T performance by decreasing the carrier concentration and the electric field at

the drain side. Previous studies in literature have incompletely addressed [92][93][94] the issue of drain or source bias stress that occurs in addition to a gate bias.

The TFT is viewed as a symmetric device where the drain is distinguished from the source terminal as being the terminal supplied with a more positive bias. Since the drain-source and source-drain currents in a TFT can be viewed as stemming from a gate-source (V_{GS}) and a gate-drain bias (V_{GD}) as shown in Appendix A, experiments to verify the dependence of ΔV_T on V_{GS} and V_{GD} were carried out. The results are shown in Figure 41 where it is observed that the ΔV_T for a TFT in saturation is smaller than that of a TFT operating in the linear mode at the same V_{GS} . Since the biases studied are of relatively small magnitudes ($0 < V_{GS} < 15$ and $0 < V_{GD} < 15$), it is likely that the ΔV_T stress is dominated by the defect creation mechanism. If the defect pool model is considered (where the ΔV_T is proportional to the number of carriers induced in the conduction band tail states), a TFT in saturation having less carriers at the drain side (due to the pinching off effect) than at the source side would exhibit a smaller ΔV_T . Thus, the decrease in channel charge during saturation may explain the smaller ΔV_T for a TFT operating in saturation mode as compared to linear mode operation.

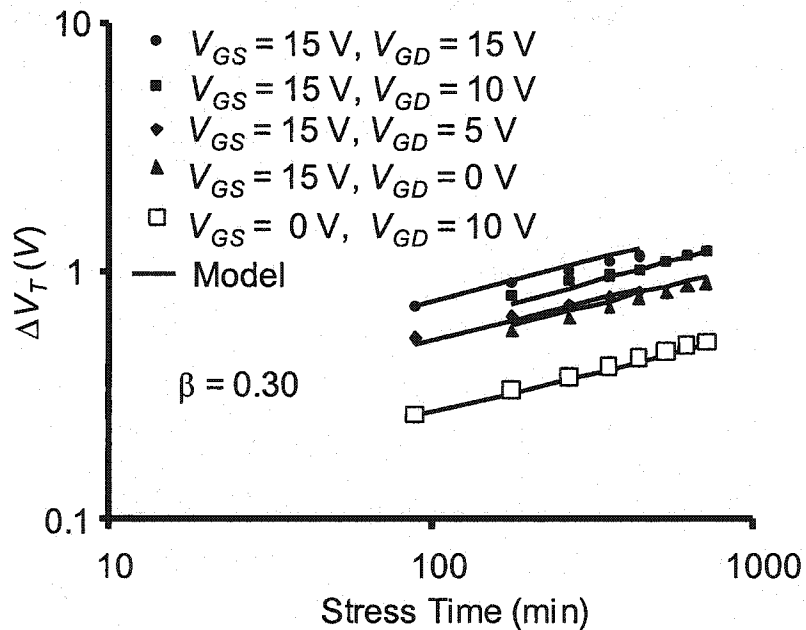


Figure 41. Dependence of ΔV_T on V_{GD} .

To quantify, since defect state creation is proportional to the charge carriers induced in the band tail states, simple MOS equations for induced channel charge are written below to develop a rudimentary ΔV_T model for a TFT operating with both, drain and gate biases.

The maximum number of carriers in the channel occur when the TFT operates in the linear mode implying the ΔV_T should also be at its maximum then. In linear mode ($V_{DS} = 0$) and assuming a uniform channel, the charge can be written as,

$$Q_G(lin) = C_G.W.L(V_{GS} - V_T) \quad (5)$$

where C_G is the TFT gate capacitance per unit area, W is the TFT width, and L is the TFT length.

When a bias exists at the TFT drain, the charge stored on the gate can be calculated by writing it first as a function of the channel length in the y direction (see Appendix A for details on the direction definition),

$$Q_G(y) = C_G.W.(V_{GS} - V_T - V(y)) \quad (6)$$

where $V(y)$ is the surface potential along the channel that varies from 0 to V_{DS} from the source to the drain. The incremental voltage drop along the channel, dV , can be expressed as,

$$dV = [I_{DS}/g(y)] dy \quad (7)$$

where I_{DS} is the transistor drain current, constant over the length of the channel and assumed to flow parallel to the surface and $g(y)$ is the channel conductance expressed as,

$$g(y) = Q(y)W\mu \quad (8)$$

where μ is the effective mobility of the carriers. Then, Q_G can be obtained by integrating eqn. (6) along the length of the channel, L ,

$$Q_G = C_G W \int_{y=0}^L (V_{GS} - V_T - V(y)) dy \quad (9)$$

Making a change of variable using eqn. (7) and eqn. (8), eqn. (9) becomes,

$$Q_G = C_G W \int_0^{V_{DS}} (V_{GS} - V_T - V(y)) \frac{W\mu(-C_G(V_{GS} - V_T - V(y)))}{I_{DS}} dV \quad (10)$$

Substituting the linear mode I_{DS} equation into eqn. (10) above, solving the integral and simplifying yields,

$$Q_G = \frac{2}{3} C_G W L \frac{(V_{GS} - V_T)^3 - (V_{GD} - V_T)^3}{(V_{GS} - V_T)^2 - (V_{GD} - V_T)^2} \quad (11)$$

The limit of eqn. (11) as V_{GD} approaches V_{GS} (i.e. the transistor enters the linear region as $V_{DS} \rightarrow 0$) is given by eqn. (5). In the other direction, as V_{GD} approaches V_T (i.e. the transistor enters the saturation region where $V_{DS} \rightarrow V_{GS} - V_T$), the channel charge on the TFT gate decreases to 2/3 of the channel charge in the linear mode (see eqn. (11) with $V_{GD} = V_T$).

The relationship between normalized channel charge and ΔV_T was verified to be linear in Figure 42 where data from Figure 41 was replotted at various stress times. The implemented model (see eqn. (12) that follows) was compared to experimental data in Figure 41 at the various drain and source bias voltages and appears to be in good agreement with a maximum discrepancy of less than 10%. Since the ΔV_T appears to be proportional to the induced channel charge, the maximum and minimum values for channel charge also set the upper and lower limits for ΔV_T respectively.

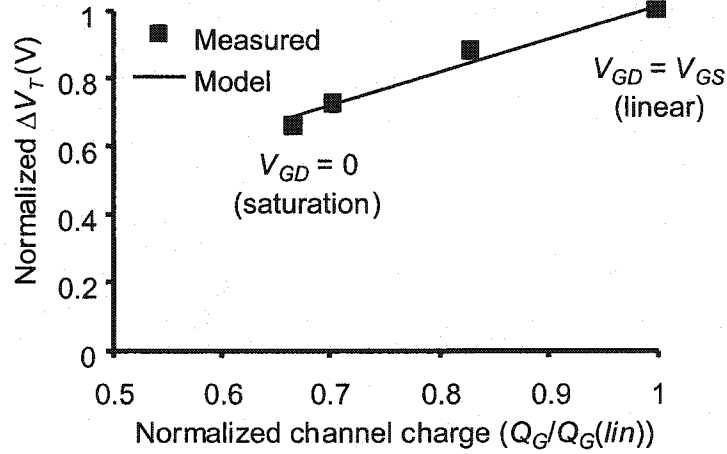


Figure 42. Normalized ΔV_T as a function of normalized channel charge, $Q_G/Q_G(lin)$.

Here, data from Figure 41 for $V_{GS} = 15$ V and $0 < V_{GD} < V_{GS}$ has been used.

Unlike linear and saturation mode, driving the TFT deeper into saturation (i.e. $V_{GD} < V_T$) appears to have little effect on the ΔV_T . In Figure 43, the TFT drain voltage is increased from $V_{DS} = 15$ V to 30 V (i.e. V_{GD} is changed from 0 to -15 V) while V_{GS} is maintained at 15 V. The results indicate that there is very little change in ΔV_T once the TFT enters saturation. Conceptually, the negligible change in ΔV_T appears to agree with the theory that ΔV_T is proportional to the total number of carriers in the a-Si TFT channel. Driving the TFT deeper into saturation modifies the total charge concentration only slightly since the channel is already pinched off and hence, the ΔV_T should not change.

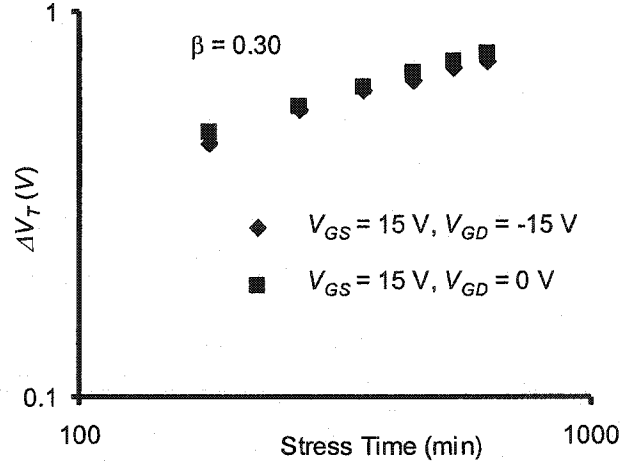


Figure 43. ΔV_T for a TFT in different levels of saturation

The ΔV_T model for positive DC bias stress is updated to include the effect of drain and source bias as,

$$\Delta V_T^+(t) = \left(\frac{Q_G}{Q_G(\text{lin})} \right) A (V_{ST} - V_{Ti}) t^{\beta_1} \quad (12)$$

where $Q_G(\text{lin})$ is defined in eqn. (5), Q_G is defined in eqn. (11), $A = 0.0115$, $V_{ST} = V_{GS}$ and $\beta_1 = 0.30$. Note that the minimum value for Q_G occurs when the TFT enters saturation and driving the TFT deeper into saturation does not change this value.

It is also interesting to note that in Figure 39, Figure 41 and Figure 43, a slight curvature in the ΔV_T versus stress time measurement is sometimes noticeable. This is likely due to the measurement being performed for constant voltage bias stress. Here, as the V_T shifts to a more positive value with increasing stress time, the effective stress voltage ($V_{ST} - V_T$) at the TFT gate decreases since V_{ST} is kept constant. This reduction in V_{ST} implies that the TFT is not being stressed to the same extent as it was at the start of the experiment and consequently, the slope of the stress measurement becomes shallower. In contrast, increasing ($V_{ST} - V_T$) to equal ($V_{ST} - V_{Ti}$) at all times during the stress measurement eliminates the slight curvature as noted by Powell in constant current stress experiments [88].

4.2.3.2 Negative gate bias

Results for small negative biases ($-10 < V_{GS} < 0$ and $-10 < V_{GD} < 0$) were difficult to measure accurately since the positive ΔV_T that occurs during the TFT I_{DS} - V_{GS} monitoring for

V_T extraction between bias stress applications corrupts the small (in mV) negative bias stress related ΔV_T . For larger negative gate and drain voltages ($-25 < V_{GS} < -15$ and $-25 < V_{GD} < -15$), where both defect state creation and charge trapping mechanisms may be active, the channel charge proportionality of V_{GS} and V_{GD} noticed in positive bias stress measurements is not observed.

However, it was noticed that when the $V_{GD} = 0$, the ΔV_T becomes relatively small as shown in Figure 44. The large drop in ΔV_T during the presence of a drain and gate bias is likely due to the non-linear (since α is not unity) relationship of ΔV_T to V_{GS} .

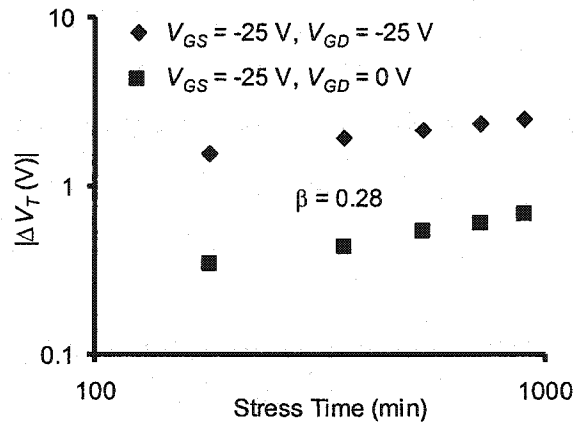


Figure 44. ΔV_T dependence for negative gate, drain and source bias values

Verified only in the ($-25 < V_{GS} < -15$ and $-25 < V_{GD} < -15$) range, the following empirical functions provide an estimate of the measured data with an error of around 15%.

$$\begin{aligned}\Delta V_T^-(t) &= -B|V_{ST}|^\alpha t^{\beta_2}, V_{GS} < 0, V_{GD} = V_{GS} \\ \Delta V_T^-(t) &= -B|(0.66)V_{ST}|^\alpha t^{\beta_2}, V_{GS} < 0, V_{GD} = 0\end{aligned}\quad (13)$$

where $B = 0.12 \times 10^{-3}$, $\alpha = 2.49$, $V_{ST} = V_{GS}$ and $\beta_2 = 0.28$ as before. Effectively, the ΔV_T due to negative bias takes on a maximum value when the drain and source node voltages are zero and the minimum value for ΔV_T at a particular V_{GS} is achieved when $V_{GD} = 0$. Intuitively, the above result is reasonable because the TFT suffers the largest ΔV_T when $V_{GS} = V_{GD}$, i.e. when there is a large field across both the source and drain sides of the TFT and a maximum carrier concentration exists in the channel (so the conditions for both charge trapping and defect creation mechanisms respectively are present). When the TFT drain bias equals that on the

TFT gate ($V_{GD} = 0$), both the field across the drain side and the channel charge are reduced and the ΔV_T consequently decreases.

For imaging applications implementing PPS architectures, the maximum negative bias on the a-Si TFT gate (around -5 V) is chosen primarily to reduce the leakage current. Here, the TFT functions as a simple switch and the drain voltage rarely exceeds 1 V. Thus, $V_{GD} \sim V_{GS}$ and the overall TFT ΔV_T analysis can proceed in a manner as if there is no applied drain bias. In contrast, it will be seen in later sections that some TFTs in the APS readout circuit have a negative drain terminal bias in the OFF state that is equal to or larger than the applied TFT gate OFF voltage. Here, eqn. (13) will be used to provide a worst-case estimate of the negative ΔV_T .

4.2.4 Effect of DC bias stress on leakage current

It is unclear if other authors [67][75][86] have considered the impact of voltage stressing on TFT leakage current. However, commercial radiological x-ray detectors based on a-Si TFT PPS architectures have recently become available [6] implying that the effect of voltage stress on TFT leakage is manageable for imaging applications (where duty cycles are small).

The voltage stress-leakage relationship is also seen for the in-house TFTs in Figure 38. Here, for our in-house fabricated TFTs, the leakage current increases by about five times over a period of 10 hours at a $V_{ST} = 15$ V. In general however, the TFT leakage current stayed in the sub-pA range for all metastability measurements, which is adequate for imaging applications.

4.3 Pulse bias metastability

A pulse can be characterized by its period (related to frequency) and pulse width (related to duty cycle). Varying both of these parameters affects the magnitude of ΔV_T as will be discussed in the following subsections.

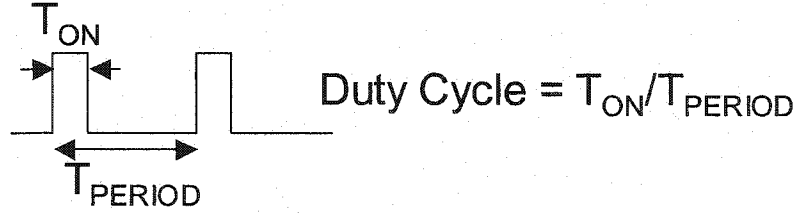


Figure 45. Pulse definitions and duty cycle

4.3.1 Effect of pulse frequency on ΔV_T

The discussion and measurements in the previous sections are valid for constant stress bias voltages (DC). During circuit operation however, the TFTs undergo pulse bias, which can change the metastability performance. The behavior of a-Si TFTs under pulse bias is examined with respect to frequency in this section.

Pulse related ΔV_T has been widely reported to be relatively independent of frequency for positive pulse voltages [86][94][95]. For a unipolar (i.e. +V/0 or -V/0) pulse, a primary effect of frequency is to reduce the total stress time of the TFT. I.e. for a 50 % duty cycle, the pulse is ON only half of the time as compared to DC bias applied for the same time period. In addition, the OFF cycle provides a relaxation time for the TFT, which can further reduce the ΔV_T depending on the relaxation time required by the various trapped charge and/or defects. Note that a bipolar pulse can be viewed as an extension of the unipolar case where during the OFF cycle, a negative voltage is applied to the TFT for the complement of the pulse duty cycle.

In contrast to positive gate bias pulses, the ΔV_T can be reduced significantly for a negative pulse bias in comparison to a constant negative bias for a similar effective application time. A model proposed in [86] attempts to explain this behavior by suggesting that electrons or holes accumulate in the a-Si channel depending on the polarity of the applied pulse bias. This implies that as pulse frequency is increased past some threshold frequency, the ΔV_T should decrease significantly since carriers have not had sufficient time to accumulate. Originally, the model was proposed for only the charge trapping mechanism, which was in line with Kanicki's claim that charge trapping is the major phenomena contributing to ΔV_T in a-Si TFTs. However, since accumulation of carriers in the TFT

channel governs both deep defect creation and the charge trapping mechanisms, the negative pulse bias ΔV_T model does not contradict the defect pool model.

When a gate voltage is applied, carriers accumulate in the channel (some in the conduction band but mostly in tail states) allowing both charge trapping and deep defect creation to proceed. Since hole mobility is almost two orders lower than electron mobility in the a-Si material, the frequency response of the TFT is expected to be much higher for electron accumulation (via positive gate pulses) as opposed to hole accumulation (via negative gate pulses). Of course, carrier mobility is not the only cause of longer accumulation times for holes. For an n-channel transistor, the n-type source and drain regions are a primary source of channel electrons during the ON cycle while thermal generation is the most likely source of holes during the OFF cycle.

So the ΔV_T decreases if the TFT is pulsed at a frequency greater than its 3 dB frequency since carriers do not have sufficient time to accumulate in the channel. For positive bias pulses, pulsing the TFT beyond its 3 dB frequency is a moot point since the TFT is generally operated at a frequency lower than the 3 dB point for proper performance. However, for negative bias pulses, the ΔV_T may decrease at pulse frequencies that are much less than the TFT electron carrier frequency response since the hole accumulation rate is much slower than electron accumulation.

To examine this phenomenon further, a simple RC model [86] can describe a-Si TFT operation under negatively pulsed bias stress as shown below. Here, the gate insulator capacitance, C_i is in series with the a-Si semiconductor capacitance, C_s . An effective resistance, R_s is included in parallel with C_s to account for hole conductance in the a-Si layer. When a negative pulse is applied to the gate (V_{ST}), the total gate voltage is initially distributed across the gate insulator a-SiN and the a-Si layer since the a-Si layer acts as a semi-insulator under negative bias at higher frequencies. Eventually, hole carriers (via thermal generation) begin to accumulate near the a-Si/a-SiN interface and the voltage drop across the insulator, V_i , approaches V_{ST} .

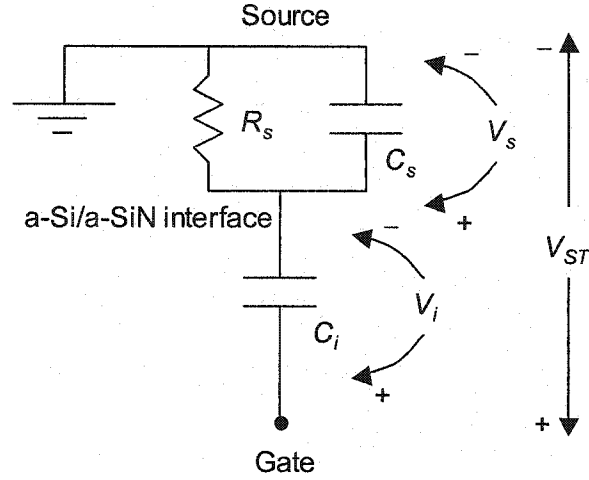


Figure 46. Equivalent circuit of a-Si TFT during negatively pulsed gate bias stress.

Here, $V_i(t)$ can be written as,

$$V_i(t) = V_{ST} \left[1 - \frac{C_i}{C_i + C_s} \exp\left(\frac{-t}{\tau_h}\right) \right] \quad (14)$$

where $\tau_h = R_s C_s$ is the effective hole accumulation time constant. The most likely source of holes is thermal generation near the a-Si/a-SiN interface where the generated electrons are repelled into the bulk semiconductor by the applied negative gate bias. Using the above equation, the initial and final values of V_i are given as,

$$V_i(0) = V_{ST} \frac{C_s}{C_i + C_s}, V_i(\infty) = V_{ST} \quad (15)$$

In order to relate the ΔV_T to the effective carrier concentration at the insulator-semiconductor interface, the accumulated hole concentration can be written as,

$$N_{accum} = -N_i + N_s \quad (16)$$

Where $N_i = C_i V_i / q$, $N_s = C_s V_s / q$ and q is the usual electron charge. Noting the $V_{ST} = V_i(t) + V_s(t)$, $V_s(t)$ can be obtained in terms of eqn. (14) and V_{ST} . Using $V_i(t)$ and $V_s(t)$ in eqn. (16), the accumulated hole concentration can be simplified as,

$$N_{accum}(t) = \frac{C_i V_{ST}}{q} \left[\exp\left(\frac{-t}{\tau_h}\right) - 1 \right] \quad (17)$$

Then, the average accumulated carrier concentration under pulse bias stress, N_{AC} , with a pulse ON time, T_{ON} , can be expressed as,

$$N_{AC} = \frac{1}{T_{ON}} \int_0^{T_{ON}} N_{accum}(t) dt \quad (18)$$

$$N_{AC}(T_{ON}) = \frac{-C_i V_{ST}}{T_{ON}} \left[1 - \frac{\tau_h}{T_{ON}} + \frac{\tau_h}{T_{ON}} \exp\left(-\frac{T_{ON}}{\tau_h}\right) \right], \quad (19)$$

$$N_{AC}(\infty) = \frac{-C_i V_{ST}}{T_{ON}} = N_{DC}. \quad (20)$$

The above equation illustrates that as the negative pulse ON time, T_{ON} , increases and becomes comparable to τ_h , N_{AC} decreases. N_{AC} is at its maximum when T_{ON} is infinity (i.e. at DC).

Following the approach in [86], if the ΔV_T is assumed to be directly proportional to the effective carrier concentration at the a-Si/a-SiN interface (N_{accum}), then the pulse bias ΔV_T reduction factor can be computed as,

$$\frac{N_{AC}(T_{ON})}{N_{DC}} = \frac{\Delta V_T(T_{ON})}{\Delta V_{T_DC}} = 1 - \frac{\tau_h}{T_{ON}} + \frac{\tau_h}{T_{ON}} \exp\left(-\frac{T_{ON}}{\tau_h}\right) \quad (21)$$

The above equation was fit to negative pulse bias metastability data and a value of 32 ms for τ_h was extracted in [86]. In other words, for a negative pulse bias with a T_{ON} of 32 ms, the ΔV_T corresponds to only 36% of the DC bias ΔV_T at the same negative voltage level (where the above equation was used).

4.3.2 Effect of pulse duty cycle on ΔV_T

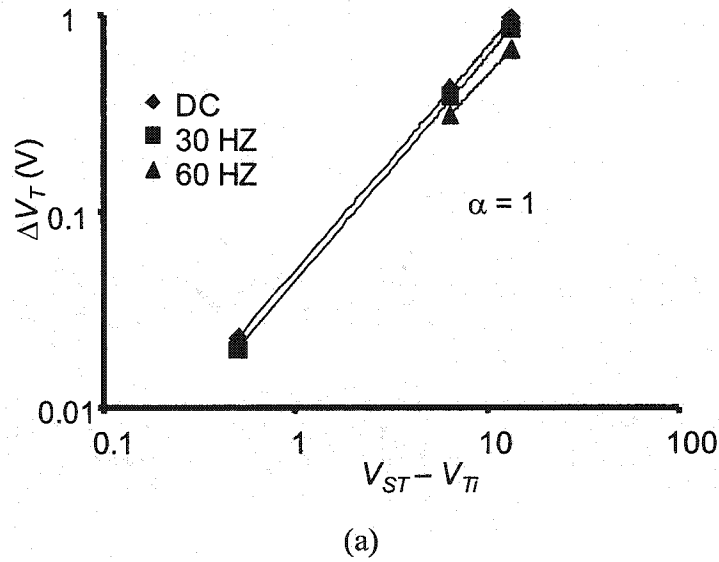
In general, smaller duty cycles induce less ΔV_T for the same pulse frequency since the effective stress time is further reduced. The reduced ΔV_T result holds true for both negative and positive pulse voltages. Due to lower hole mobility and accumulation times, the ΔV_T is also reduced if, in the process of reducing the duty cycle, the negative ON pulse does not provide sufficient time for the holes to accumulate in the channel. i.e. the pulse OFF frequency drops below the hole carrier accumulation time constant, τ_h , as noted in the

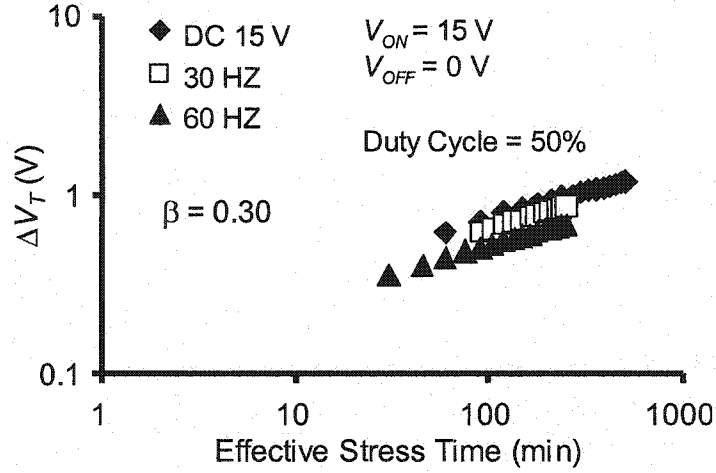
previous section. In addition, detrapping and relaxation of defect states during the longer OFF cycle of small duty cycle ON pulses further reduce the overall TFT ΔV_T .

4.3.3 Positive pulse bias frequency and duty cycle experiments

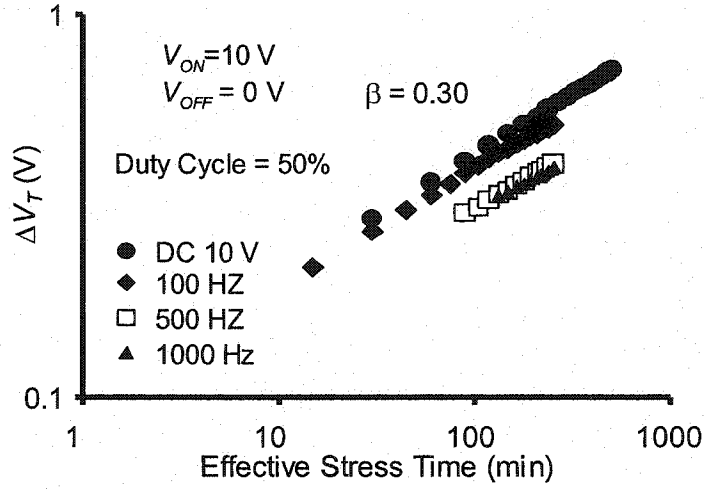
Experiments were carried out to determine the ΔV_T with unipolar positive pulse voltages of varying frequency and duty cycle. For all pulsed gate bias experiments, the ΔV_T is plotted as a function of effective stress time (i.e. time pulse is ON). This is done in order to allow a comparison with the DC stress voltage since an objective of this section is to determine a relationship between the pulsed and DC stress bias voltages.

As shown in the following graphs, applying a pulse bias decreases the ΔV_T slightly during the effective TFT ON time. In both curves plotted below, the β value extracted was the same as that for DC bias stress. In addition, the ΔV_T remained a linear function of $(V_{ST}-V_{Ti})$ at the frequencies of measurement (i.e. $\alpha = 1$). The value of α in the figure below was extracted at an effective stress time, $t = 240$ minutes.





(b)



(c)

Figure 47. Alpha and beta for pulsed positive bias stress voltages.

If the behavior of ΔV_T is plotted against the various stress pulse frequencies, the dependence on frequency appears to level out beyond a certain frequency i.e. slightly less than 500 Hz in the figure below. If the gate pulse frequency is increased further, the ΔV_T rolls off near the corner frequency of the TFT's frequency response as observed in [92].

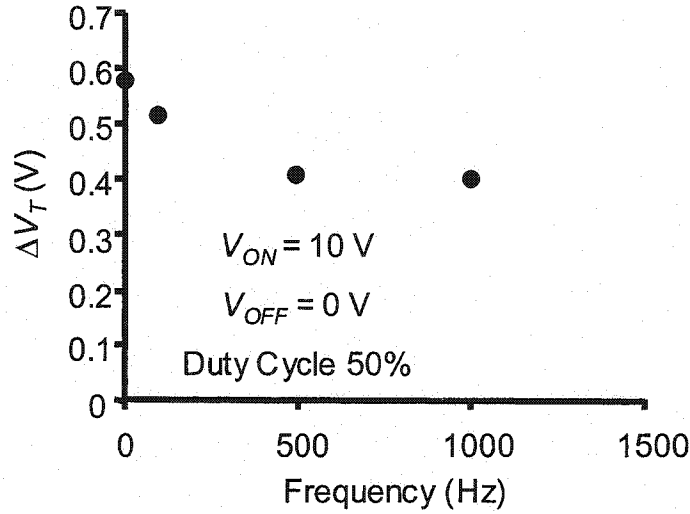


Figure 48. ΔV_T as a function of frequency measured at an effective stress time of 255 minutes

The above figure suggests that there is some frequency dependent ΔV_T mechanism that is dominant at lower frequencies. It is possible that as a pulse is applied to the TFT gate, some deep gap defects relax and/or the fast states in the nitride begin to re-emit. The defect relaxation or re-emission mechanisms can manifest themselves when a constant DC bias is applied at the TFT gate.

A fundamental effect of reducing the duty cycle of a pulse at the gate of a TFT is to reduce the effective TFT stress time. Intuitively, one would expect a smaller ΔV_T as the duty cycle is reduced since the TFT is ON for a smaller time period. Incidentally, reducing the duty cycle is one of the most effective and commonly used methods in industry to obtain reliable long-term performance out of a-Si TFTs. The effect of reducing the duty cycle on a 15 V unipolar pulse is shown in the following figure. Notice that at a 5% duty cycle, the ΔV_T due to the pulse bias is a tiny fraction of the DC ΔV_T . Ideally, the tail end of the 5% duty cycle pulse ΔV_T and the start of the DC bias ΔV_T should line up. The observed discrepancy (a shift in the y-axis) is attributed to the frequency effect discussed above where the extended OFF time of the pulse for the smaller duty cycle allows more deep states defects to relax and/or the fast states in the nitride to emit. In contrast, the β values stay around the DC bias stress value of 0.30 (with an error of less than 10%) for all of the frequency and duty cycle measurements.

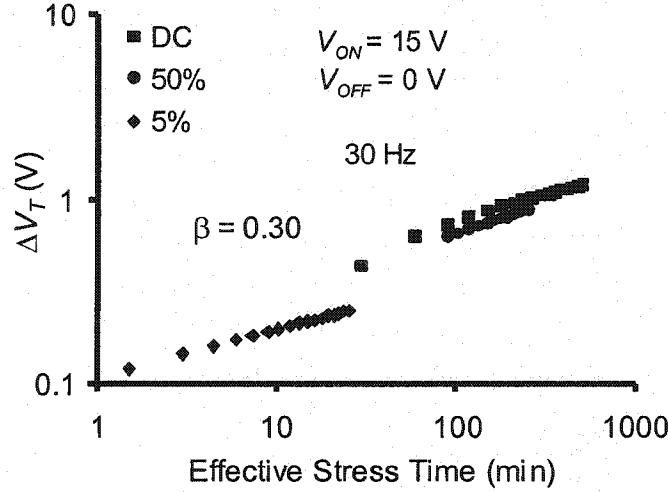


Figure 49. Duty cycle dependence of ΔV_T

In order to model the frequency and duty cycle dependence of ΔV_T on positive pulses, most authors [86][94][95] assume the worst-case scenario,

$$\Delta V_{T_AC}^+(t) = (T_{ON}/T_{PERIOD}) \Delta V_T^+(t) \quad (22)$$

However, the above equation can overestimate the ΔV_T when the duty cycle is very small due to the restoring action of the zero bias during the OFF cycle of a unipolar pulse. The case of a bipolar pulse will be seen later on in this section where the restoring action of the negative part of the gate pulse is fully accounted for.

4.3.4 Negative pulse bias frequency and duty cycle experiments

Unlike positive pulse bias ΔV_T that is relatively frequency independent, slower hole accumulation times make the negative ΔV_T highly dependent on the gate pulse frequency. As an example, consider the graph shown in Figure 50 where a -20 V negative pulse was applied to a TFT gate at 25 Hz. Clearly, there is a large reduction in the ΔV_T and for higher pulse stress frequencies, the ΔV_T dropped to very small values (in mV).

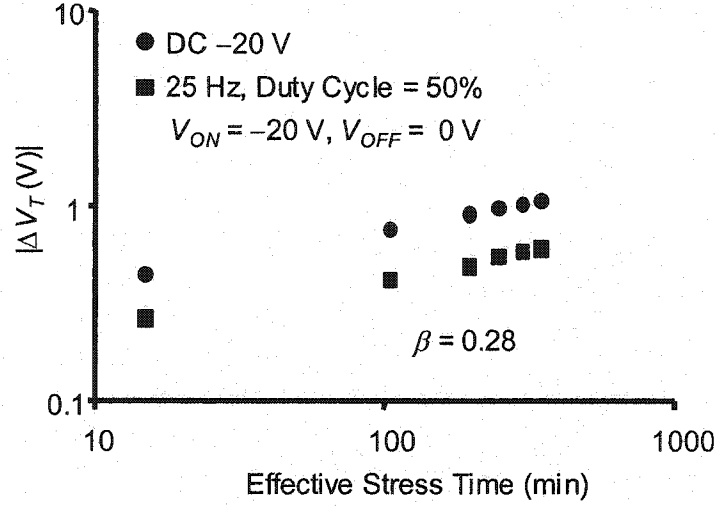


Figure 50. Effect of frequency on negative stress bias ΔV_T

The drop in ΔV_T can be accounted for by applying the hole accumulation theory proposed in [86] and discussed in a previous section. Here, simple measurements of ΔV_T were made for different pulse frequencies (and hence T_{ON}) at a 50% duty cycle and a -20 V ON bias. The pulse bias results along with DC bias values are shown in the following figure where the model derived in the previous section has been fit to the measured results using a value of $\tau_h = 13$ ms. The τ_h value extracted for our in-house TFTs is about three times lower than those reported in [86]. The main reason for this drop is attributed to TFT process differences.

From Figure 51, it is noted that a unipolar negative bias pulse with a T_{ON} of 33 ms has an effective ΔV_T of slightly more than 50% of the corresponding negative DC bias ΔV_T . Since the above graph is a function of the pulse ON time, T_{ON} , both frequency and duty cycle effects can be accounted for by the following equations discussed previously,

$$\Delta V_{T-AC}^-(t) = k_{V_T^-} \Delta V_T^-(t) \quad (23)$$

$$k_{V_T^-} = 1 - \frac{\tau_h}{T_{ON}} + \frac{\tau_h}{T_{ON}} \exp\left(-\frac{T_{ON}}{\tau_h}\right). \quad (24)$$

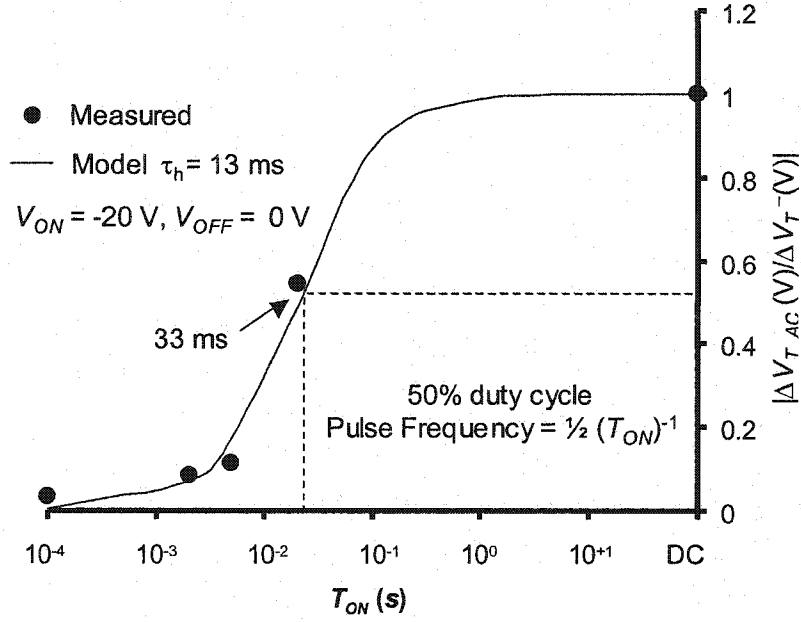


Figure 51. Frequency dependence of negative stress bias ΔV_T

4.3.5 Bipolar pulses

Since positive and negative unipolar gate pulses tend to shift V_T in the positive and negative directions respectively, using bipolar pulses offers an attractive means for reducing the overall ΔV_T . In practice, when TFT ON and OFF periods are comparable, the a-Si TFTs used in the AMLCD industry [86] [94] require bipolar gate pulses for long term ΔV_T management. The effect of these bipolar pulses is discussed in [86] where it was shown that the positive and negative ΔV_T resulting from positive (during the TFT ON cycle) and negative (OFF cycle) pulse bias cancel each other in a linear fashion. Experimental results from in-house TFTs shown below appear to corroborate the findings in [86]. Here, the maximum error of about 15% is attributed to measurement inaccuracy in the unipolar -10 V pulse measurement. As before, measurement interruptions to obtain TFT transfer characteristics for V_T extraction may mitigate the full effect of the negative bias pulse on the TFT's ΔV_T .

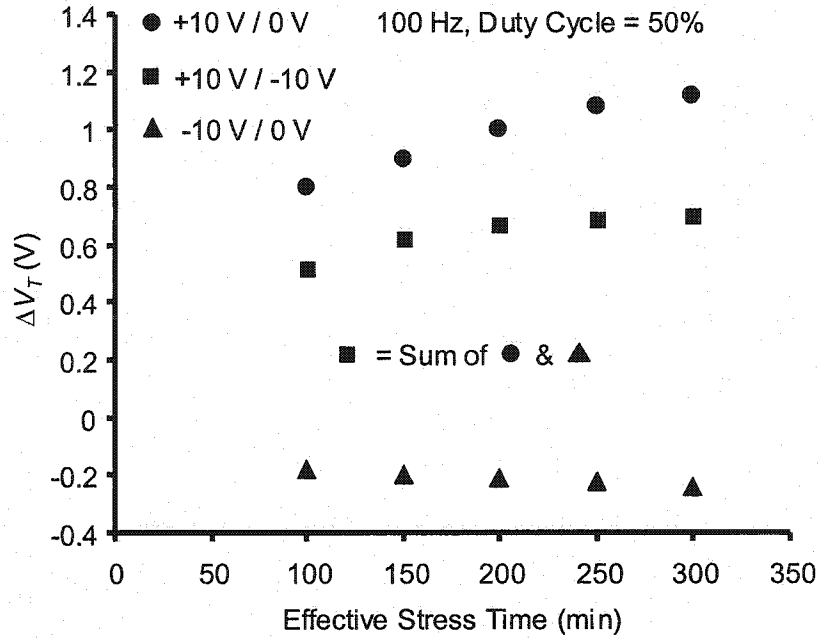


Figure 52. ΔV_T for a bipolar pulse and its two unipolar components.

In contrast to AMLCD applications, imaging applications of a-Si TFTs are governed more by low leakage current requirements on the TFT rather than ΔV_T management. As discussed in previous sections, high leakage current in a C-APS circuit can corrupt the image signal both at the integration node (via the pixel RESET TFT leakage) and during readout (via the combined leakage of the large number of READ TFTs connected to each array column). The following figure plots TFT leakage current and the negative ΔV_T against the negative bias applied at the TFT gate.

Here, a large negative valued pulse gives a large negative ΔV_T , which is useful in negating the effects of the positive ΔV_T that appears during the TFT ON cycle. However, there is a direct tradeoff where the leakage current in an a-Si TFT increases as the negative gate bias on the TFT is made larger. The optimal leakage value for the TFT shown above is somewhere between -5 V and -10 V . However, the negative ΔV_T due to a -5 V gate bias is quite small and unable to fully compensate for the positive ΔV_T during the TFT ON cycle. Fortunately for diagnostic medical imaging applications, the duty cycle of the a-Si TFTs is at most 0.1% for digital fluoroscopy (i.e. one row out of 1000 is being read out at any given time). This will be discussed in the next section where it is shown that although the TFTs in

the APS pixel readout circuit suffer from a ΔV_T in the positive direction, the *gain* of the APS pixel stays relatively constant over a 10000-hour array lifetime due to the circuit's inherent feedback properties and small duty cycles.

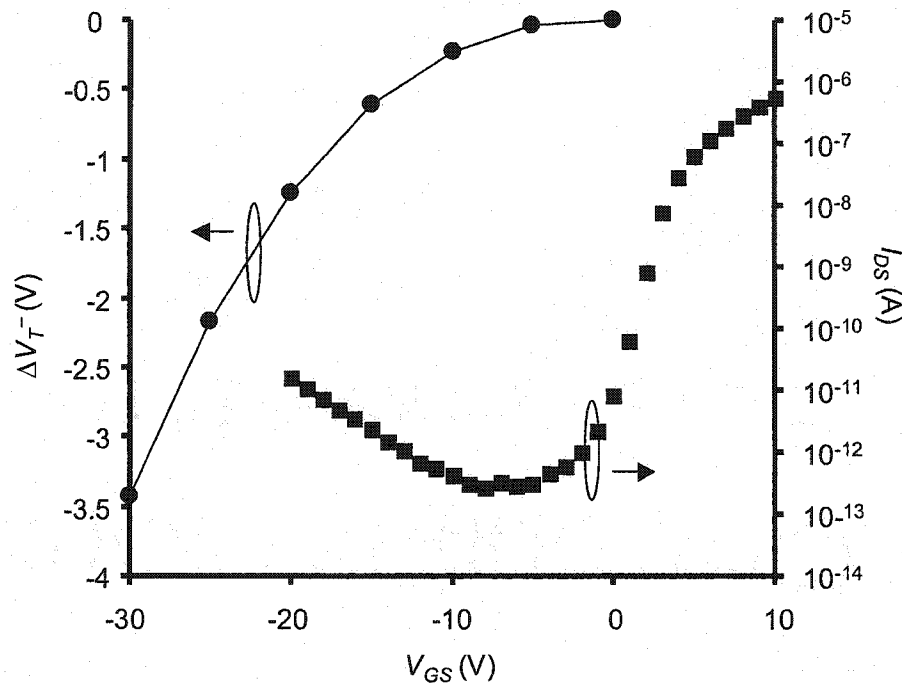


Figure 53. In-house TFT leakage and metastability for negative DC bias gate voltages. Here, the ΔV_T is plotted for a stress time of 600 min. The TFT transfer characteristics are measured for a 150/25 TFT at $V_{DS} = 16$ V.

4.4 Active pixel sensor

Any ΔV_T analysis of the a-Si APS would involve an examination of all TFTs: RESET, AMP and READ. However, since the RESET TFT is decoupled from the APS readout circuit via the AMP TFT, the ΔV_T performance of the C-APS (schematic repeated in Figure 54) can be examined in two stages.

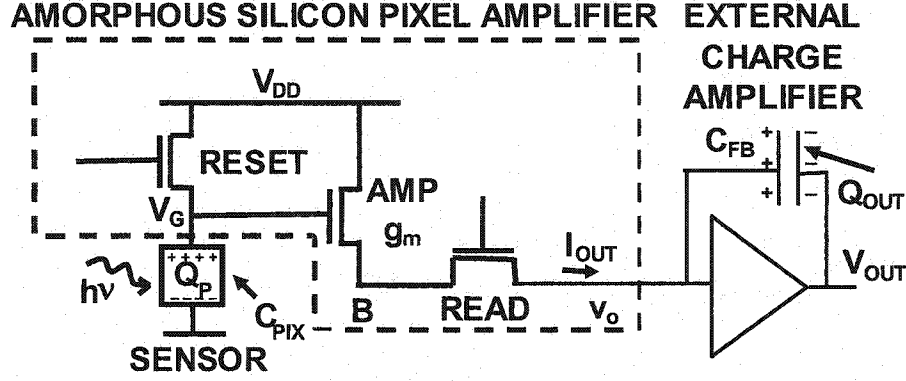


Figure 54. C-APS readout circuit

4.4.1 RESET TFT

The ΔV_T for the RESET TFT affects pixel reset time (T_{RESET}) since the RESET TFT behaves as a switch to reset the integration node every frame. Typical voltages at the gate of the RESET TFT (with respect to the TFT drain and source) would range from $V_{GS} = -5\text{V}$ or -10V in the OFF state to minimize leakage and $V_{GS} = +15\text{V}$ in the ON state to minimize TFT ON resistance (R_{ON}) and hence reset time. A ΔV_T would affect the RESET switch ON-resistance thus affecting the readout time. The small duty cycles used in diagnostic imaging applications appear to be the primary means to manage ΔV_T since it is not feasible to apply large negative voltages that can potentially increase the TFT leakage current and corrupt the signal at the integration node. The RESET TFT's ΔV_T and reset time (T_{RESET}) are shown in the following Figure 55 where it is seen that the V_T changes by a much larger amount than T_{RESET} . Here, the metastability theory developed for positive and negative gate pulses in the previous sections of this chapter is used to calculate the ΔV_T for the RESET TFT.

The main reason for the difference between ΔV_T and ΔT_{RESET} is that T_{RESET} is a function of R_{ON} ($= 1/G_{ON}$) and its sensitivity to V_T depends largely on the applied V_{RESET} bias in the ON state. The normalized sensitivity of TFT on-conductance, G_{ON} with respect to V_T is,

$$\frac{dG_{ON}}{dV_T} \frac{V_T}{G_{ON}} = -\frac{V_T}{(V_{RESET} - V_T)}, \quad (25)$$

where $G_{ON} = dI_{DS}/dV_{DS} = K_{RESET}(V_{GS} - V_T)$ for $V_{DS} \sim 0$ (from the simple Level 1 MOS model discussed in Appendix A). So if a large V_{RESET} (+15 V in the figure below) is chosen, the T_{RESET} becomes relatively insensitive to ΔV_T .

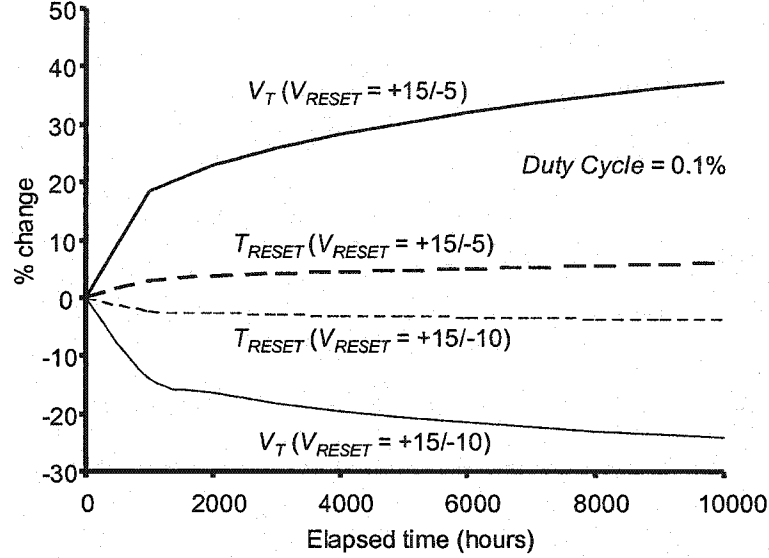


Figure 55. % change in V_T and reset time (T_{RESET}) over a 10,000 hour lifetime for TFTs based on the in-house process. Here, two RESET pulses of magnitude +15/-5 and +15/-10 are applied at a pulse frequency of 30 Hz and a duty cycle of 0.1% ($V_{DS} \sim 0$ V).

4.4.2 AMP and READ TFTs

Since the AMP and READ TFT form part of the readout circuit for the APS and connect to the charge amplifier, the gain is sensitive to any ΔV_T arising from these TFTs. From before, the gain is a direct function of the APS circuit g_m . We recall that the g_m is obtained by equating the current through the AMP TFT in saturation and READ TFT in linear. The TFT currents are equated to derive the V_{DS} across the READ TFT, which then enables the determination of R_{ON} , I_{OUT} , and g_m . Rewriting the previously derived equation for V_{DS} ,

$$V_{DS} = \frac{\left[2K_A(V_{GA} - V_{TA}) + K_{RD}(V_{GRD} - V_{TRD}) - \left[K_{RD} \left(\frac{-4K_A V_{GA}(V_{GRD} - V_{TRD} + V_{TA}) + 2K_{RD} V_{GRD} V_{TRD}}{+2K_A(V_{GA}^2 - V_{TA}^2) - K_{RD}(V_{GRD}^2 + V_{TRD}^2)} + 4K_A V_{TA}(V_{GRD} - V_{TRD}) \right)^{1/2} \right] \right]}{(K_{RD} + 2K_A)} \quad (26)$$

For the AMP TFT, there is a minimal bias across the gate and source terminals (V_{GS_AMP}) during integration (i.e. during the READ TFT OFF state) where the TFT has a gate voltage but is non-conducting since $V_{GS_AMP} < V_T$. Also, since the bias at the gate of the AMP TFT is close to the drain bias (V_{DD}), it can be assumed that little, if any, ΔV_T occurs due to V_{GD_AMP} . Most of the ΔV_T on the AMP TFT occurs during the READ TFT ON state where there is $V_{GS_AMP} = V_{GA} - V_{DS}$ bias and V_{GA} and V_{DS} are defined in the above equation.

For the READ TFT, a pulse with a 15 V bias (V_{ON}) is applied at the TFT gate to turn it ON starting off the readout phase. When readout is complete, a -5 V bias (V_{OFF}) is applied at the gate to minimize leakage current in the TFT OFF state. During the ON state, the TFT operates in switch mode where the V_{DS} across the switch is given by eqn (26) above and is much smaller than the READ TFT gate pulse value, V_{GRD} . During the OFF state, node B (also the drain of the READ TFT during the ON state) reaches a value ($V_{GA} - V_T$) effectively turning the AMP TFT OFF. The value $V_B = (V_{GA} - V_{TA})$ is then “frozen” at that node during the OFF state effectively increasing the reverse bias across the READ TFT (i.e. $V_{GS_READ} = V_{OFF} - (V_{GA} - V_{TA})$). All of these node voltages must be taken into account to estimate the overall Δg_m of the APS circuit over time.

Figure 56 shows the Δg_m by using the equations for ΔV_T developed in the previous sections of this chapter. Here a supply voltage ($V_{DD} = 8$ V) along with a READ TFT gate pulse of +12/-5 V at a duty cycle of 10% is applied (clocked at 30 Hz). Measurements of a-Si C-APS metastability were carried out with the source of the READ TFT connected to ground (thereby mimicking the virtual ground of a charge amplifier). The remainder of the measurement setup was the same as that of the pulse bias metastability. In contrast to extracting the ΔV_T from the TFT I_D - V_{GS} curves, here the g_m was extracted from the I_{OUT} - V_{GS} curve of the C-APS readout circuit at a fixed bias point (i.e. at $V_G = 8$ V).

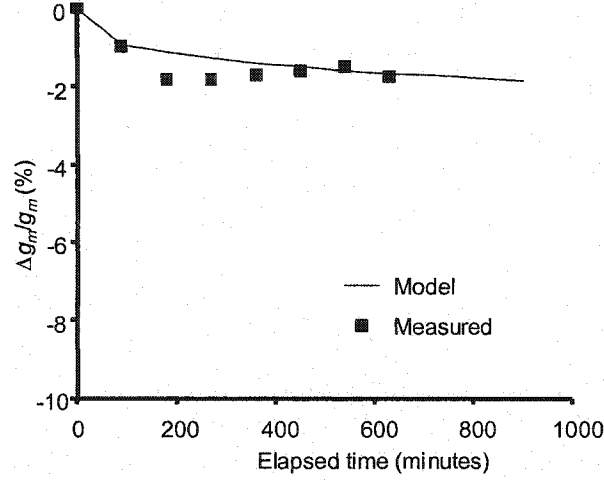


Figure 56. % change in g_m for $V_{DD} = 8V$, $V_{RD} = +12/-5$. The frequency of the applied pulse was 30 Hz at a duty cycle of 10 %. The model was obtained by substituting the ΔV_T equations for positive and negative pulse bias stress developed in this chapter into eqn. (26).

From the above figure, there is a small error in the model prediction compared to the measured data with the least error occurring at the extremities. Since there are no other bias voltages applied to the TFT circuit, it is speculated that the error is possibly due to the presence of large transient voltages at node B in the APS readout circuit.

To examine the effect of transient voltages at node B, simulations using an in-house TFT model and different READ TFT pulse voltages were implemented. The results are shown in the Figure 57 below. Here, three different pulse ON voltages ranging from +12 to +20 V were used. Note that the transient voltage at node B can reach up to +55 V for the rising edge of the +20/0 V pulse in the in-house TFT based APS circuit. At the transient peak where $V_B = 55$ V, $V_{GS} = (12 - 55) = -43$ V for the AMP TFT. In contrast, $V_{GS} = (12 - 38)$ is only -26 V for the +12/-5 V gate pulse. A complementary effect occurs at the falling edge of the READ pulse where the node B spikes to a negative value as seen in Figure 19. As expected, large READ TFT gate pulses cause larger transients at node B. So if the ΔV_T of the APS readout circuit depends on the transient voltage at node B, there would be a larger error between the model and measured results for the +20/0 V pulse since its transient peak is larger than that of the +12/-5 pulse.

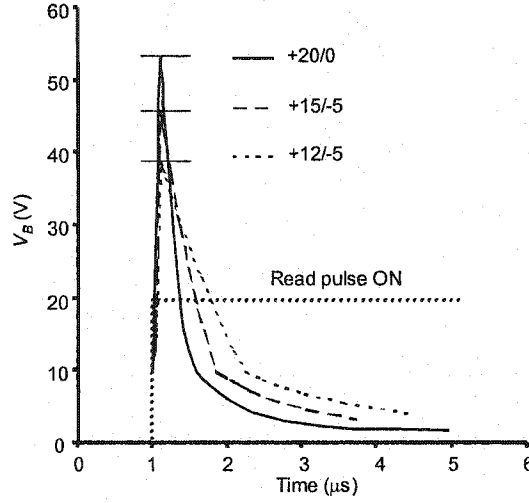


Figure 57. Peaks of the READ TFT pulse transient for different pulse ON values. Note that the transient peak increases and the duration shortens for higher ON voltages. Here, the supply voltage $V_{DD} = V_G = 12$ V.

In Figure 58, measurement results for Δg_m from a +20/0 V READ TFT pulse applied at 30 Hz with a 10% duty cycle and a $V_{DD} = 12$ V are shown. As expected, the error is much larger between the model developed in the previous section and measured data values in Figure 58 than with the data shown in Figure 56.

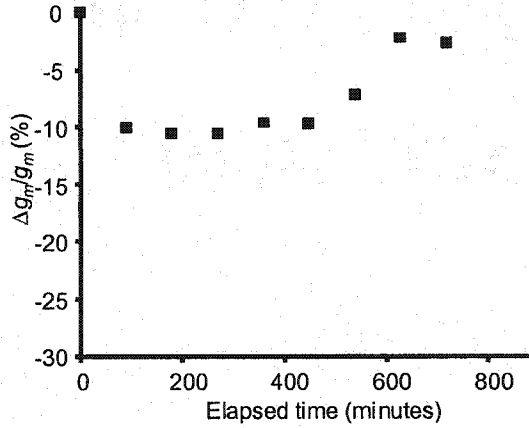


Figure 58. % change in g_m for $V_{DD} = 12$ V, $V_{RD} = +20/0$. The frequency of the applied pulse was 30 Hz at a duty cycle of 10 %.

The above result highlights the possibility that transient node voltages have an effect on the ΔV_T of the AMP and/or READ TFT. It is likely that charge trapping may play a significant role in the ΔV_T calculation due to the large magnitude of the transient voltage. An

explicit comparison of measured data with model equations yields a large discrepancy, particularly at low elapsed times ($t < 500$ min). Hence, the model data is not indicated in Figure 58. The increase in g_m after the first 3 hours of pulse bias stress in Figure 58 indicates that ΔV_T of the AMP and READ TFTs is decreasing. More research (beyond the scope of this work) is required to identify a relationship between ΔV_T and the peaks and duration of the transient voltage at node B.

The matter of transient voltages is simplified considerably for the APS circuit where designing the AMP TFT to be larger than the READ TFT can minimize the V_B peaks as shown in Figure 59. A larger AMP TFT provides a bigger capacitance at node B at the cost of increasing the transient voltage spike's duration and hence, delaying the readout. As mentioned previously, while the transient voltage due to the READ TFT gate pulse turning ON serves to raise the node voltage at V_B , the transient voltage due to the pulse turning OFF pulls the node B voltage below 0 V. When V_B is larger than V_{GA} (AMP TFT gate voltage), there is an additional negative ΔV_T . Similarly, V_B being less than V_{GA} or V_{GRD} (READ TFT gate voltage) accentuates the ΔV_T in the positive direction. Keeping the AMP TFT larger than the READ TFT can decrease the magnitude of both transient voltage spikes by increasing the capacitance at node B but the longer transient voltage duration must be accounted for in the pixel readout time

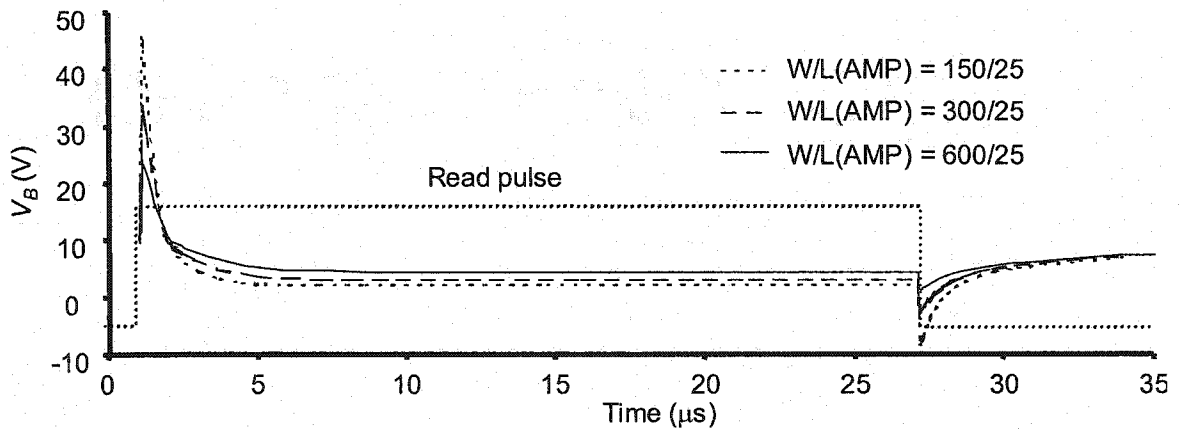


Figure 59. Transient voltage at node B for different AMP TFT aspect ratios. Here, the W/L of the READ TFT was kept constant at 150/25 and $V_{DD} = +12$ V.

The models developed in the previous section for $\Delta V_{T_{AC}}^+$ and $\Delta V_{T_{AC}}^-$ are accurate if the transient voltage at node B is kept to a minimum as shown in measurements presented in

Figure 56. Transients can also be minimized if a small physical capacitor is included in at node B.

The remainder of this section is based on estimating Δg_m for a-Si C-APS circuits on the assumption that transients at node B have been minimized and hence, ΔV_T is a strong function of the steady state voltages at the various terminals of the readout circuit. The TFTs are pulsed with a frequency and duty cycle particular to the application. For real-time diagnostic medical fluoroscopy, the array is operated at 30 Hz with a duty cycle of around 0.001 (0.1 %) or less so the effective ON time for the TFTs is only about 10 hours in the 10,000-hour lifetime of the imager. Fluoroscopy is considered to be the diagnostic medical imaging modality with the most stringent requirements.

The following Figure 60 shows the AMP TFT and READ TFT threshold voltages (V_{T_AMP} and V_{T_READ}) as a function of time for a $V_{DD} = 12$ V and a $V_{READ} = +15/-5$ V pulse at a duty cycle of 0.1 % for 10,000 hours. Note that since the duty cycle is only 0.1%, the READ TFT is OFF 99.9% of the time. For a pulse frequency of 30 Hz, the -5 V bias is in effect for a $T_{ON} \sim 33$ ms (causing about 50% of the equivalent DC negative bias ΔV_T).

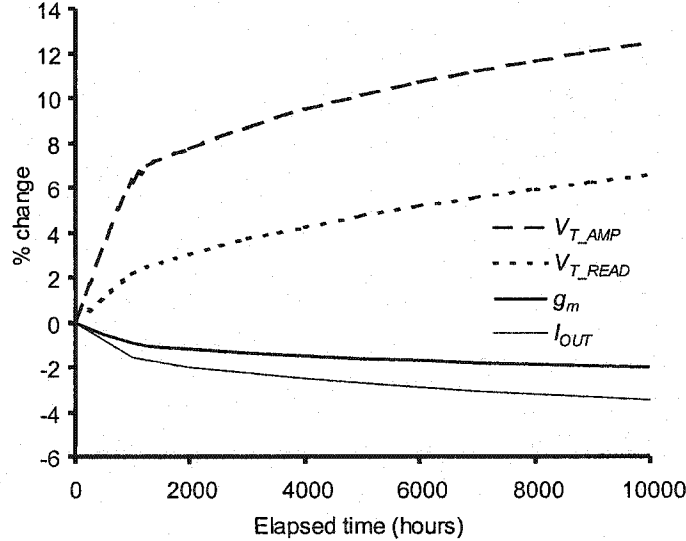


Figure 60. % change in READ and AMP TFT and APS readout circuit g_m . Here $V_{DD} = 12$ V, $V_{READ} = +15/-5$ and the pulse is at 30 Hz with a 0.1% duty cycle.

As shown in the above figure, g_m is expected to decrease by less than 2% over the lifetime of the array. This is primarily due to the reduced duty cycle and to a lesser extent,

due to the negative bias across the READ TFT gate and source in the OFF state ($V_{GRD} = V_{OFF} - (V_{GA} - V_{TA})$), which serves to reduce the READ TFTs ΔV_T . The high stability of g_m is also due to the READ TFT switch, which acts as a compensation resistor. Here, as the AMP TFT V_T increases, the V_{DS} (or V_B) across the READ TFT decreases due to the lowered I_{DS} . The reduction in V_{DS} increases the $(V_{GA} - V_{DS} - V_T)$ drop across the AMP TFT causing the current to increase a little. The net effect is that I_{DS} and g_m change at a lower rate than the AMP or READ TFT V_T .

As mentioned above, a large factor aiding the APS stability in medical imaging applications is the reduced TFT duty cycle. For example, in a 1000 x 1000 pixel real-time fluoroscopic imager, the TFTs are clocked 33 μs every 33 ms giving a duty cycle of 0.1%. The figure below shows the effect of increasing duty cycle on g_m for the same C-APS circuit.

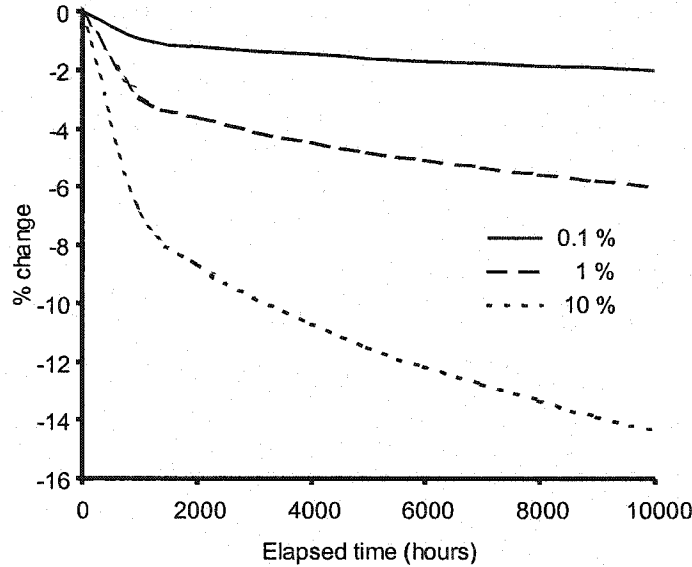


Figure 61. % change in g_m for different duty cycles

As illustrated above, reducing the duty cycle mitigates the ΔV_T . Thus, for the APS READ and RESET switch TFTs, bipolar clocking pulses to provide a small READ TFT ON resistance and low leakage currents in the OFF state can be coupled with small duty cycles to give a relatively small shift in C-APS g_m (and hence gain). Some of the results presented in this chapter related to APS metastability have been published in [52][53][54].

Chapter 5. Noise in TFT circuits

This chapter starts by examining low frequency a-Si TFT thermal and flicker noise sources that contribute to the overall noise performance of the APS. Next, reset noise, a particularly significant source of circuit noise in imaging pixels is considered. In traditional CMOS APS circuits, reset noise is usually the dominant noise source and in this chapter, its nature is examined by theoretical calculations and noise measurements on an a-Si TFT switch. Lastly, the overall noise performance of the C-APS circuit is evaluated and discussed for use in low-noise, real-time fluoroscopic medical imaging, the most challenging diagnostic medical imaging modality from a noise point-of-view.

5.1 Low frequency Noise

5.1.1 Thermal noise

Van der Ziel [98] showed that the spectral intensity of the drain current fluctuation $S_I(f)$, in a long channel MOSFET due to thermal noise is,

$$S_I(f) = \frac{1}{L^2} \int_0^L 4kTg(y)dy \quad (1)$$

where L is the channel length, k is Boltzmann constant, T is the carrier temperature, $g(y)$ is the conductivity of the channel a distance y from the source (in *siemens-cm*) and is directly proportional to the total charge in the channel, and f is the frequency. At no drain bias, the conductivity of the channel is uniform and thus $g(y) = L.g_{ds0}$, where g_{ds0} is the zero drain bias

conductivity $((W/L)C_G\mu(V_{GS} - V_T)$ for $V_{DS} = 0$). Then, at zero drain source voltage, eqn. (1) becomes,

$$S_I(f) = \frac{1}{L^2} \int_0^L 4kT(Lg_{ds0})dy = 4kTg_{ds0} \quad (2)$$

Since g_{ds} is proportional to the total charge in the channel, $S_I(f)$ at larger drain biases can be determined by using the channel conductance $g(y)$ for a drain bias with eqn. (1) as shown below. The total charge in a transistor with a gate and drain bias was estimated previously in eqn. (11) of Chapter 4.

$$S_I(f) = \frac{2}{3} 4kT\mu \frac{W}{L} C_G \left[\frac{(V_{GS} - V_T)^3 - (V_{GS} - V_T - V(y))^3}{(V_{GS} - V_T)^2 - (V_{GS} - V_T - V(y))^2} \right] \quad (3)$$

Eqn. (3) can be solved at saturation ($V_{DS} = V(y) = V_{GS} - V_T$) to give,

$$S_I(f) = \frac{2}{3} 4kT \left[\mu \frac{W}{L} C_G (V_{GS} - V_T) \right] = \frac{2}{3} 4kTg_{ds0} \quad (4)$$

which is the standard equation for MOSFET thermal noise quoted in literature [98]. As the limit $V(y) = V_{DS} \rightarrow 0$, eqn. (3) reduces to the value given by eqn. (2) for zero drain bias. Therefore, eqn (4) may be represented as,

$$S_I(f) = (\gamma)4kT.g_{ds0} \quad (5)$$

where γ is a factor that decreases for a transistor from a value of 1 in the linear mode to 2/3 at saturation.

Measurements performed by Boudry and Antonuk [109] and verified by the author [122] confirmed that TFT thermal noise has some similarities to MOSFET thermal noise and can be modeled using eqn. (5) where g_{ds0} is derived from eqn. (96) from Appendix C,

$$g_{ds0} = \frac{dI_{DS}}{dV_{DS}} = M_0 (V_{GS} - V_T)^n \quad (6)$$

where $n = (\alpha - 1) = 1.38$ for the in-house TFTs. Substituting eqn. (6) into eqn. (5) yields,

$$S_I(f) = (\gamma)4kTM_0(V_{GS} - V_T)^n \quad (7)$$

where M_0 can be represented by the usual product of parameters, $\mu_{EFF}C_G(W/L)$.

5.1.2 Flicker noise

When a constant voltage is applied across the terminals of a resistor, a fluctuation in the dc current is observed. This fluctuating current is in addition to the thermal noise, and exhibits the following general power spectral density (PSD):

$$S_I(f) = K I^2 / f^\Gamma \quad (8)$$

where I is the DC current, Γ lies between 0.8 and 1.4 in general and K is a proportionality constant inversely proportional to the device area. The $1/f$ slope of the characteristic function has been verified over the range of frequencies from 10^{-6} to 10^6 Hz [100]. No experimental evidence as yet has suggested that the spectrum will flatten out in the extreme low frequency range. The first recorded observations of $1/f$ noise were made by Johnson [101] in 1925. Since then, two somewhat different theories of $1/f$ noise have been developed. The first model, commonly known as the numbers fluctuation model, was proposed by McWhorter [102] in mid 1950s. The model attributed the generation of $1/f$ noise to fluctuations in the majority carrier density (number of carriers) near the semiconductor surface, due to a fluctuation in the occupancy of surface interface traps. It has been successfully used to model $1/f$ noise in surface channel devices such as the MOSFET. The numbers fluctuation model does not account for the $1/f$ noise observed in media such as ionic solutions, or wire-wound resistors, which have no interface traps.

An alternative theory in 1960s was proposed by Hooge and Hoppenbrouwers [103] to explain $1/f$ noise. The theory is based upon the mobility fluctuations within a homogenous, conducting medium and is commonly known as the mobility fluctuation model. Hooge proposed the following empirical relation,

$$S_I(f) = \alpha_H I^2 / (N_{tot} f^\Gamma) \quad (9)$$

where I is the drain current as before, N_{tot} is the total number of charge carriers in the medium and α_H is the Hooge dimensionless coefficient. Hooge's coefficient has been experimentally verified to have a value of 2×10^{-3} in several homogeneous mediums. This value does not hold for some mediums and Hooge and Vandamme proposed that α_H should be modified depending on the impurity scattering in a material [104].

For a TFT operating in the linear mode, the Hooge flicker noise spectral density can be approximated as,

$$S_{ID}(f) = \frac{\alpha_H}{f} \frac{q\mu}{L^2} I_D V_{DS} \quad (10)$$

where $N_{tot} = W.L.C_G.(V_{GS} - V_T)$ in the linear mode and I_D from eqn. (96) in Appendix C was used in eqn. (9). Eqn. (10) can now be expressed in terms of the terminal voltages only as,

$$S_{ID}(f) = \frac{\alpha_H}{f} \frac{q\mu}{L^2} (M_0(V_{GS} - V_T)^n V_{DS}) V_{DS} = \frac{\alpha_H}{f} \frac{q\mu}{L^2} (M_0(V_{GS} - V_T)^n V_{DS}^2) \quad (11)$$

In contrast to the Hooge $1/f$ noise theory of mobility fluctuation, the McWhorter theory of number fluctuation is based on trapping and detrapping of carriers. For the trapping theory of carriers [110], the current noise spectral density for a MOSFET is expressed as,

$$S_{ID}(f) = \frac{k^*}{f} \frac{\mu}{C_{OX} L^2} \frac{I_D V_{DS}}{(V_{GS} - V_T)} \quad (12)$$

where k^* takes into account the electron tunneling from insulator traps near the interface to the conducting channel. Eqn. (12) can be rewritten using eqn. (96) from Appendix C to obtain the noise current spectral density for a TFT operating in the linear region,

$$S_{ID}(f) = \frac{k^*}{f} \frac{\mu}{C_{OX} L^2} \frac{(M_0(V_{GS} - V_T)^n V_{DS}) V_{DS}}{(V_{GS} - V_T)} = \frac{k^*}{f} \frac{\mu}{C_{OX} L^2} (M_0(V_{GS} - V_T)^{n-1} V_{DS}^2) \quad (13)$$

Using the above eqn. (13), the noise voltage and noise resistance spectral densities for both mobility and carrier number fluctuation models can be determined [110][111] and are summarized in the table below. Here, the $S_{ID(sat)}(f)$ for saturation mode TFT operation is calculated by substituting $V_{DS} = (V_{GS} - V_T)$ into $S_{ID(lin)}(f)$ shown in eqn. (13).

Table 13. $1/f$ noise spectral densities for McWhorter and Hooge theories in TFTs

	ΔN model	$\Delta \mu$ model
$S_{ID(lin)}(f)$	$\frac{k^*}{f} \frac{\mu}{C_{OX} L^2} (M_0(V_{GS} - V_T)^{n-1} V_{DS}^2)$	$\frac{\alpha_H}{f} \frac{q\mu}{L^2} (M_0(V_{GS} - V_T)^n V_{DS}^2)$
$S_{ID(sat)}(f)$	$\frac{k^*}{f} \frac{\mu}{C_{OX} L^2} (M_0(V_{GS} - V_T)^{n+1})$	$\frac{\alpha_H}{f} \frac{q\mu}{L^2} (M_0(V_{gs} - V_t)^{n+2})$

The importance of the quantities shown in Table 13 appears when the dependence of noise spectral densities on the $(V_{GS} - V_T)$ term is examined. For both the carrier trapping and carrier mobility models, there is a difference in the dependence of S_{ID} upon the $(V_{GS} - V_T)$ term, which provides the means to discriminate between the two theories.

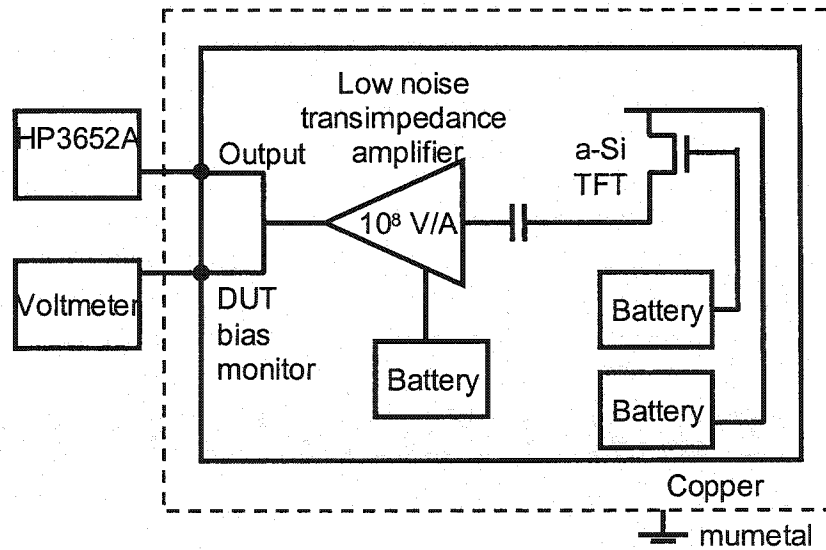
Valenza [112] carried out the various low frequency noise experiments on a-Si TFTs and determined that the Hooge model of fluctuating mobility was responsible for $1/f$ channel noise in TFTs. Rhayem determined an experimental value of 1×10^{-2} for the Hooge parameter α_H for a-Si TFTs, which corroborated earlier studies [113]. This number is about two to three orders of magnitude larger than the classical values observed in crystalline MOSFETS. In contrast, some results have been reported that contradict the Hooge theory of $1/f$ noise in TFTs proposed by Valenza. Specifically, Chen [114] performed experiments similar to Valenza and concluded that $1/f$ noise followed a blend of number fluctuation and Hooge theories. Our experimental results, presented in the next section, appear to corroborate the Hooge theory of $1/f$ noise for our in-house fabricated a-Si TFTs.

5.2 Noise Measurements on TFTs

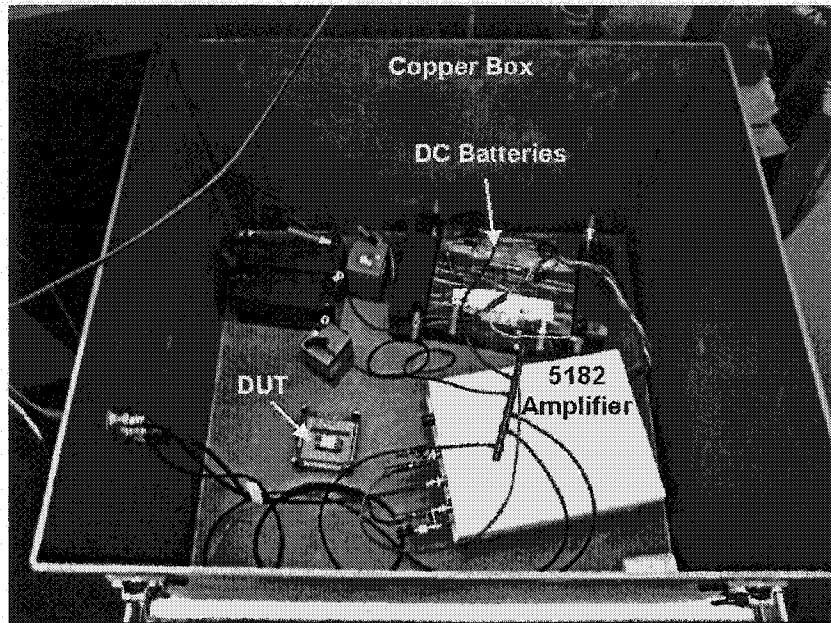
5.2.1 Measurement Setup

Current-noise-power spectrum (S_{ID} in A^2/Hz) measurements were performed on a-Si TFTs fabricated at the University of Waterloo using an in-house fully wet-etch 260°C TFT process (described in Chapter 3) compatible with the process used in developing x-ray imaging arrays. The measurements were carried out for TFTs of two different aspect ratios: 250/25 and 60/25 operating in both linear and saturation regimes (as determined by the TFT gate (V_{GS}) and drain (V_{DS}) voltages). The TFT sizes and design were similar to those used in the current mode APS test pixel introduced in Chapter 2. V_{GS} and V_{DS} were both provided by high amp hour DC batteries while an ac-coupled Perkin-Elmer 5182 transimpedance amplifier was used to amplify the noise signal to levels readable by the HP 3652A spectrum analyzer (Figure 62). The TFT, 5182 amplifier, and batteries were all placed in a shielded enclosure comprising of inner copper and outer mumetal boxes for shielding low frequency

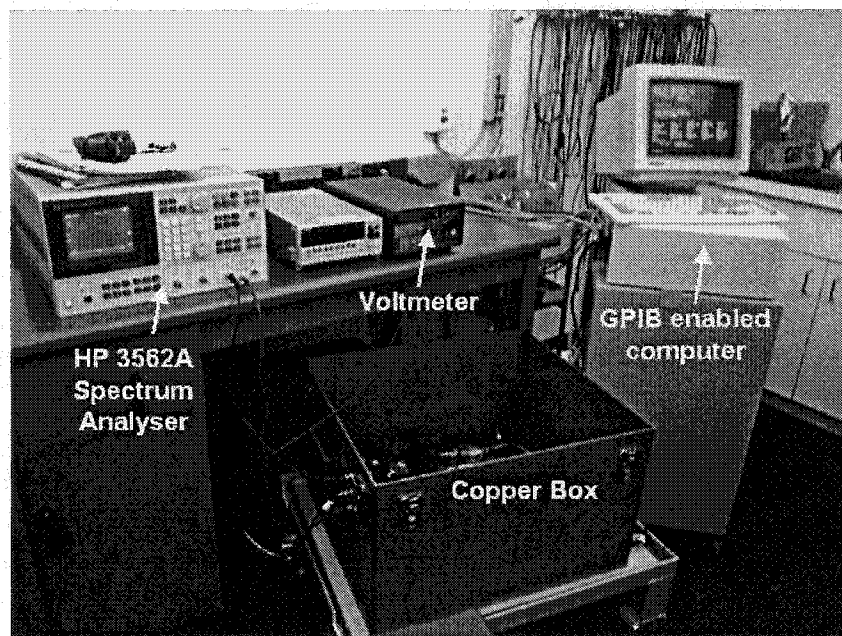
electric and magnetic fields, respectively. The AC gain of the amplifier ranged from 10^5 to 10^8 for bandwidths ranging from 1 MHz to 10 kHz. The TFT gate and drain bias voltages had to be chosen appropriately to avoid amplifier saturation by the TFT DC drain current (I_{DS}) at high gain settings. All current noise power curves (Figure 63) were reconstructed from narrowband measurements averaged at least 25-50 times and higher for low frequencies. The noise measurement system was first verified by measuring the thermal noise of low noise metal film resistors of known values. The measurement system noise was dominated by the input noise of the transimpedance amplifier (shown in Figure 63). The system noise was generally at least 10-15 times lower (at high frequencies) than the TFT drain current noise and was subtracted from each measured power spectrum. For each measured power spectrum, the noise waveform acquisition began a half hour after application of V_{GS} and V_{DS} to allow a-Si TFT drain current (I_{DS}), threshold voltage (V_T) and noise to stabilize. The transimpedance amplifier included a bias current monitor that was used to measure I_{DS} variations (e.g. due to ΔV_T) during each experiment. In general, the I_{DS} bias variation (related to ΔV_T) was less than 5% for most experiments.



(a)



(b)



(c)

Figure 62. Noise measurement test setup, (a) block diagram (b) copper box components and (c) test setup including HP3652A spectrum analyzer and GPIB enabled computer. The computer controlled the Keithley voltmeter and spectrum analyzer via the GPIB bus.

5.2.2 Thermal Noise

Repeating eqn. (7), the expected magnitude of the thermal noise of a Si TFT is:

$$S(f) = (\gamma)4kTM_0(V_{GS} - V_T)^n \quad (14)$$

where M_0 can be represented by the usual product of parameters, $\mu_{EFF}C_G(W/L)$. Here, $C_G = 25 \text{ nF/cm}^2$ for the in-house fabricated a-Si TFTs and γ ranges from 2/3 to 1 depending on the TFT being in saturation or linear mode. μ_{EFF} and V_T are determined from standard TFT parameter extraction methods discussed in Appendix C. The thermal noise measurements were performed at the lowest possible V_{DS} bias of 0.44 V. The thermal noise was visible only for the 60/25 aspect ratio TFTs operating in linear mode since the drain current dependent flicker noise dominated the measurement span of frequencies for higher V_{DS} biases, larger aspect ratio TFTs and in the saturation mode of operation.

Table 14 shows the equivalent thermal noise resistance, $R_{DS} (= (1/g_{ds0}))$ extracted from measured thermal noise data substituted into eqn. (5)) compared to the expected R_{DS} calculated from extracted in-house TFT parameters substituted into eqn. (6). Note that good agreement between the model and measured data is observed when V_{GS} is low. As V_{GS} becomes larger, the error increases and the discrepancy is likely due to additional noise from the TFT series access resistances at the source and drain region. At lower V_{GS} , the channel is highly resistive and there is a possibility that the noise due to the much larger channel resistance masks out any noise due to the series resistances. However, as V_{GS} increases and channel resistances decrease, the series resistances may become comparable to the channel resistance and raise the expected noise floor.

Table 14. Thermal noise resistance (R_{DS}) measurements for a TFT operating in linear.

W/L= 60/25 $V_{DS} = 0.44\text{V}$	Theoretical R_{DS}	Measured R_{DS}
$V_{GS} = 6 \text{ V}$	15.3 M Ω	18.0 M Ω
$V_{GS} = 8 \text{ V}$	10.1 M Ω	14.1 M Ω
$V_{GS} = 12 \text{ V}$	5.1 M Ω	10.2 M Ω

5.2.3 Flicker Noise

Figure 63 shows the power spectra in the linear region for a TFT with $W/L = 10$ and $V_{DS} = 0.44$ V. Over the shown frequency range, both flicker and thermal noise are present. Here, flicker noise ($\propto 1/f^\beta$, β is found to be between 1.0 and 1.1) tends to dominate most of the power spectrum with the $1/f$ corner being around 5 kHz.

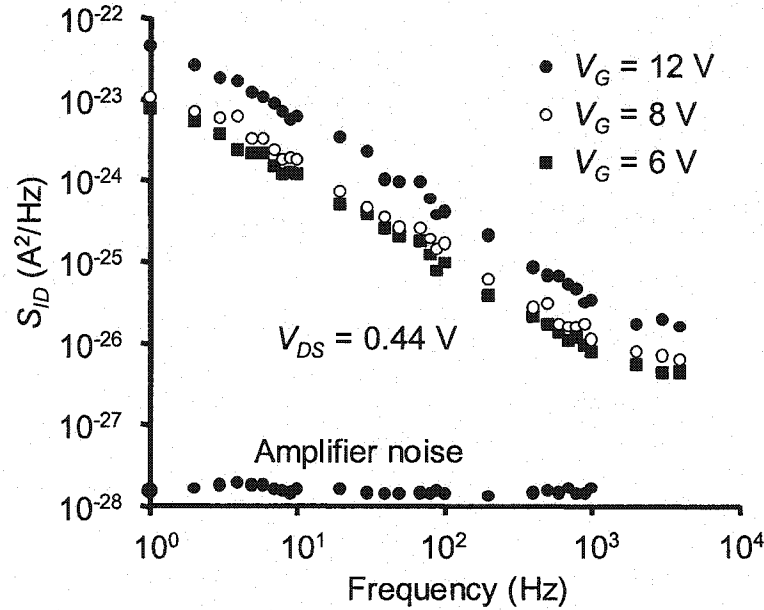


Figure 63. Noise spectra obtained for an a-Si TFT in the linear mode. The flicker noise dominates over most of the spectrum while the amplifier noise is shown at the bottom.

Using Hooge theory data from Table 13, since $S_{ID(lin)}(f) \propto (V_{GS} - V_T)^n$ ($n = 1.34$) and $I_{DS(lin)} \propto (V_{GS} - V_T)^n$, then $S_{ID(lin)}(f) \propto I_{DS(lin)}$ (slope = 1) for the linear region of operation. For the saturation region, since $S_{ID(sat)}(f) \propto (V_{GS} - V_T)^{n+2}$ (slope = 3.34) and $I_{DS(sat)} \propto (V_{GS} - V_T)^{n+1}$ (see eqn. (92) in Appendix C where $\alpha = n + 1$), then $S_{ID(sat)}(f) \propto I_{DS(sat)}^{(n+2)/(n+1)}$ (slope = 1.43) for the usual in-house TFT value of $n = 1.34$.

Figure 64 shows measurements of the noise power spectrum at 100 Hz that appear to be consistent with previous findings [109][110]. The linear and saturation mode experiments were carried out with the TFT being thermally annealed for 3 hours at 180°C between each experiment. The V_T was measured once before the experiment was carried out and once after where each experiment lasted about an hour and a half (the time was needed to acquire many averages for low frequency noise measurement accuracy). Also, due to the convenient

availability of a bias current monitor in the transimpedance amplifier, I_{DS} was obtained during the experiment in between narrowband measurements. Results shown in Figure 64 have a maximum error of less than 20% and indicate that flicker noise in the in-house TFTs appears to concur with the Hooge theory of $1/f$ noise [122].

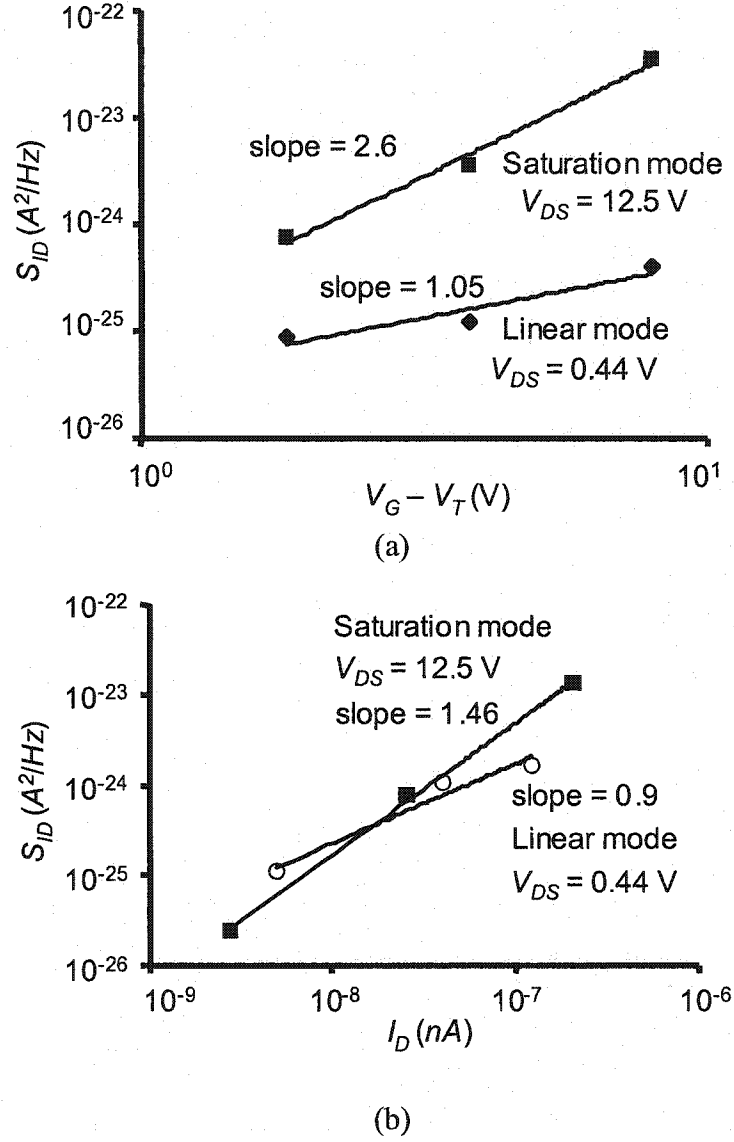


Figure 64. TFT bias current (I_{DS}) power spectral density (S_{ID}) at 100 Hz plotted against (a) $(V_{GS} - V_T)$ and, (b) I_{DS} for a TFT with an aspect ratio of 250/25.

5.3 Reset Noise

5.3.1 Theoretical background

Charge detection circuits used in a number of image sensors (e.g. APS, CCDs) for the conversion of signal charge into a voltage consist of a sensor (e.g. reverse biased diode), a reset transistor and an additional transistor (not shown below) connected as a source follower with its gate at the integration node. The diagram of a typical charge detection circuit is shown in Figure 65 below. This charge detection circuit also forms the first stage of the APS readout circuit.

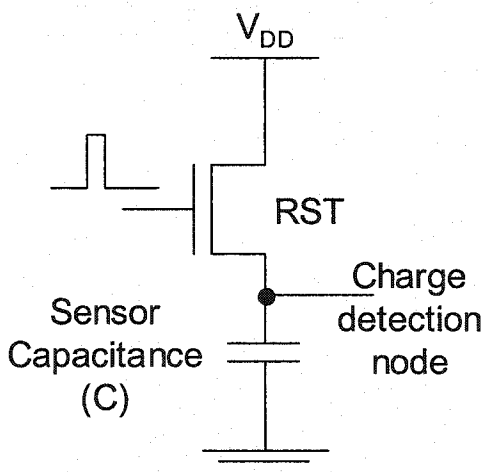


Figure 65. Circuit diagram of a typical charge detection circuit used in APS or CCD imagers

The operation of the circuit above can be divided into two cycles. In the first cycle, the reset transistor (RST) is turned ON and the voltage on the sensor, which functions here essentially as a capacitor, is equalized to that of the reference voltage generator. In the second cycle, the reset transistor is turned OFF and the sensor integration node is allowed to float to make it capable of detecting charge. If charge is collected at the integration node during this cycle, the node potential changes and the source follower transistor transfers this change to the pixel circuit output for signal processing. Turning the reset transistor ON again and transferring the collected charge to the reference generator completes the cycle.

From thermodynamic principles [115], it is well known that the voltage on the pixel capacitance is not the same after every reset, even if there is no charge collected at the detection node. From the equi-partition theorem applied to the case of the above figure [115], it follows that the variance of the voltage fluctuations, usually called reset noise or kTC noise, has the value [116],

$$\frac{1}{2} \langle v_n^2 \rangle C = \frac{1}{2} kT, \quad \langle v_n^2 \rangle = kT/C \quad (15)$$

While useful, the above result does not describe the power spectral density of the reset noise seen by circuits following the detection node. Another problem, usually encountered in the noise analysis of charge detection circuits, is the assumption that there is no correlation between the consecutive voltage levels appearing after the completion of resets [117]. This assumption is flawed because the reset transistor has a non-negligible resistance in the ON state plus any other non-ideal resistances such as those of the reference voltage generation circuitry.

Taking into account the above issues, Hynecek [115] rigorously obtained the power spectral density of reset noise in 1990 as,

$$S_e(\omega) = S_0 |H(\omega_f)|^2 \left[(1 - \xi) + \frac{1}{2} \tau \xi^2 \omega_f \sin^2 \left(\frac{\omega \delta}{2} \right) F_1(\omega_f) + \xi \sin^2 \left(\frac{\omega \delta}{2} \right) F_2(\omega_f) \right] \quad (16)$$

where,

$$S_0 = \frac{1}{\pi} kTR, \quad |H(\omega)|^2 = \frac{\omega_f^2}{\omega_f^2 + \omega^2}, \quad F_1(\omega) = \left(\frac{\omega_f^2 - \omega^2}{\omega_f^2 + \omega^2} \right) \frac{\sinh[\omega_f(\tau - \delta)]}{\cosh[\omega_f(\tau - \delta)] - \cos(\omega\tau)} \quad (17)$$

and,

$$F_2(\omega) = 2 |H(\omega)|^2 \frac{\cos \left(\frac{\omega \delta}{2} \right) \cosh[\omega_f(\tau - \delta)] - \cos \left[\omega \left(\tau - \frac{\delta}{2} \right) \right]}{\cosh[\omega_f(\tau - \delta)] - \cos(\omega\tau)} \quad (18)$$

Here, C is the integration node capacitance, $\xi (= \delta/\tau)$ is the duty cycle of the reset pulse complement, δ is the time during which the reset switch is closed, and τ is the period of the reset pulse. The term ω_f is defined as the inverse of the switch ON resistance, R and the integration node capacitance, C product. To a large extent, the power spectral density is shaped by the second term in eqn. (16) giving it the look of a $\text{sinc}^2(x)$ function. The other terms in eqn. (16) begin to dominate when the switch ON resistance (R) becomes significant.

To illustrate the consequences of an insignificant R on reset noise, the above equations are simplified below for the case where the switch resistance goes to zero. For an ideal resistor, S_0 can be rewritten as,

$$S_0 = \frac{1}{\pi} kTR = \frac{1}{\pi} \left(\frac{kT}{C} \right) \left(\frac{1}{\omega_f} \right) \quad (19)$$

Assuming $(\omega_f) \gg 1$ (i.e. $R \rightarrow 0$), eqn. (16) can be simplified as [115],

$$S_n(\omega) = \left(\frac{1}{\pi} \right) \left(\frac{kT}{C} \right) \left[\frac{(1-\xi)\omega_f}{\omega_f^2 + \omega^2} + \frac{1}{2} \tau \xi^2 \cdot \text{sinc}^2\left(\frac{\omega\delta}{2}\right) \right] \quad (20)$$

For small duty cycles, $S_n(\omega)$ is dominated by the $\text{sinc}^2(x)$ term. Integrating $S_n(\omega)$ from $-\infty$ to $+\infty$, the resulting noise voltage can be written as,

$$\langle v_n^2 \rangle = \left(\frac{kT}{C} \right) \quad (21)$$

Eqn. (21) depicts the ideal value for reset noise reported by many authors and is the same as shown in eqn. (15). It is concluded that to minimize reset noise, the switch should be made as ideal as possible. However, in the case of an a-Si TFT switch, it is challenging to obtain an ideal or close to ideal switch because of the large associated TFT ON resistances. The next part of this section will examine reset noise measurements on in-house a-Si TFTs based on the theory presented in eqn. (16) where the reset switch is non-ideal.

5.3.2 Reset Noise Measurements

One method of measuring reset noise involves fabricating a reset circuit such as the one shown in Figure 65 connected to an integrated source follower transistor capable of driving an off-chip load. This is challenging to accomplish in amorphous silicon circuitry since the flicker noise of the amorphous silicon source follower amplifier is much larger than the reset noise. The elevated noise floor of the resulting integrated circuit makes it difficult to measure just the reset noise component. To circumvent this problem, the following alternate approach was taken.

Amorphous silicon TFT reset noise was measured on a TFT with a $W/L = 60/25$ and a pixel capacitance of 17 pF. The integration node pin on the TFT device package was directly soldered to the positive input pin of an external integrated circuit differential amplifier,

INA116 while the source was connected to the negative input. Part of the pixel capacitance was provided by an external capacitor (10 pF) also soldered to the integration node pin of the TFT package and the rest was due to the input capacitance of the differential amplifier. The first differential amplifier stage, providing a gain of 10, drove an ac-coupled secondary gain stage provided by a wideband FET-input amplifier, LF356 with a fast settling time. The second stage provided a gain of 50 and had a low frequency cutoff of less than 2 Hz. An adjustable voltage divider circuit was connected between the gate and the source to reduce/cancel the feedthrough at the TFT drain in order to prevent the secondary amplifier stage from saturating.

Since flicker noise is directly proportional to current, a smaller TFT was used in order to reduce the flicker noise contribution. In addition, the drain bias of the TFT was kept very close to zero (< 0.1 V) to further reduce any flicker noise contribution by minimizing the drain current. Small TFTs are further beneficial for the reset noise measurement since their parasitic overlap capacitances are smaller and hence contribute less to output amplifier saturation via clock feedthrough. Also, a small reset voltage pulse (< 7 V) and a larger integration node capacitance (18 pF) was used to reduce any additional feedthrough related issues. The goal was to make the reset pulse sample only TFT thermal noise on the pixel capacitance hence replicating the behavior in imaging circuits. The circuit diagram of the test setup is shown in Figure 66.

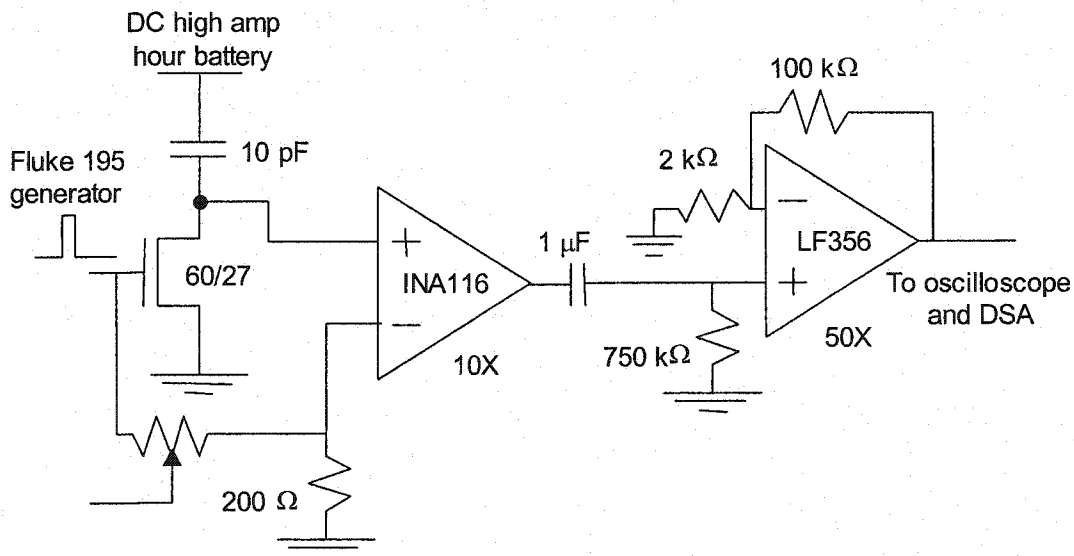


Figure 66. Reset Noise measurement setup

All the measurements were made using gate pulses with frequencies ranging from 50 Hz to 200 Hz for various duty cycles. For pulse frequencies greater than 500 Hz (2 ms period), the reset noise level dropped below the noise floor of the measurement system. The relationship of reset noise to pulse period can be seen in Figure 67 [54] where the data is plotted against a model based on the theory presented in the previous section. The error is less than 5% validating the accuracy of the model. Similar results were obtained when both duty cycle and pulse frequency were varied.

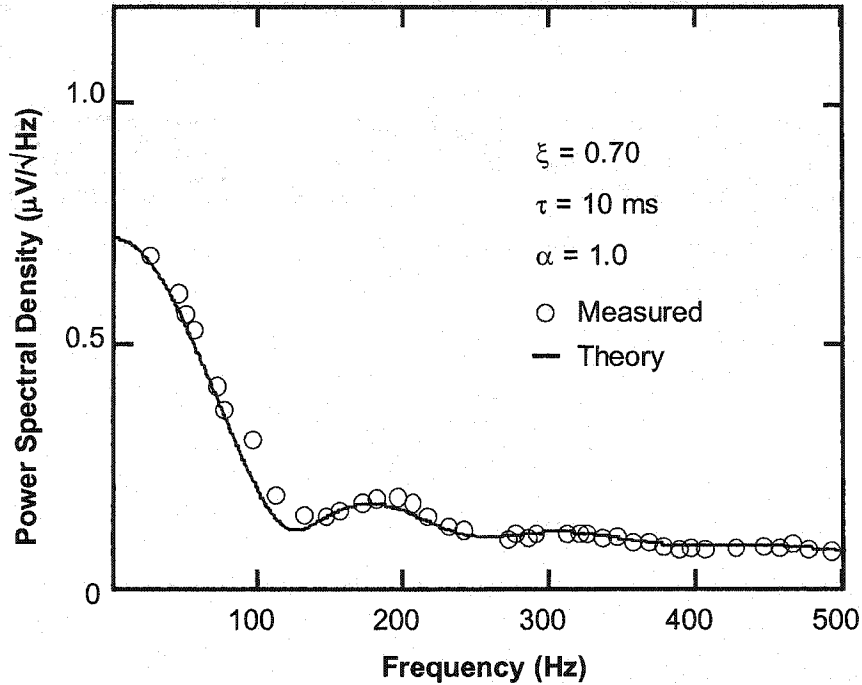


Figure 67. Comparison of theoretical and measured reset noise PSD for an a-Si TFT and a integration node capacitance of 17 pF.

5.3.3 Discussion

To get an idea of how the reset noise spectrum varies with gate pulse frequency, noise PSDs are shown in the next figure for various reset pulse periods of an a-Si TFT switch at a constant duty cycle of 10%. Note that as pulse frequency is increased (i.e. small pulse periods), the spectrum tends to concentrate around zero frequency.

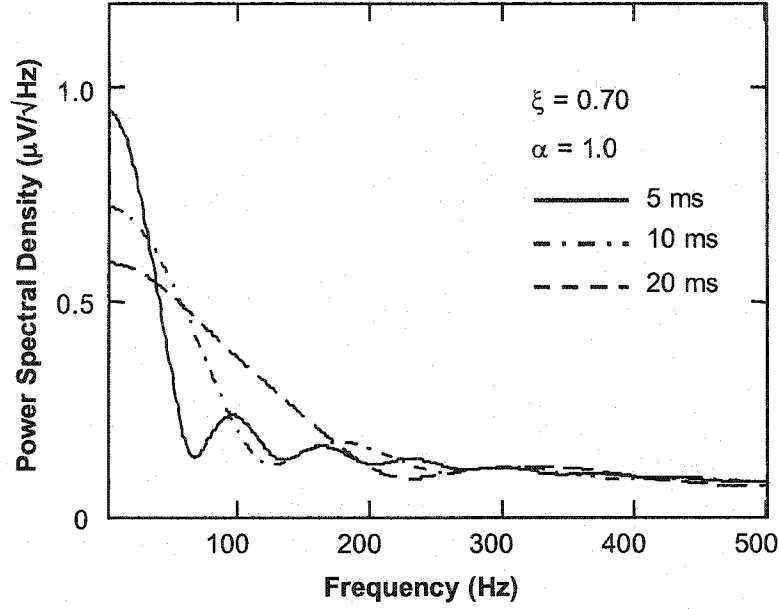
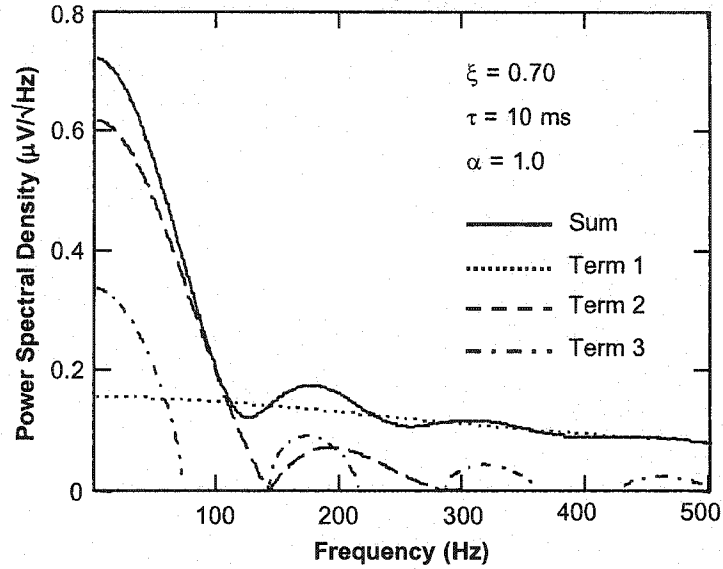


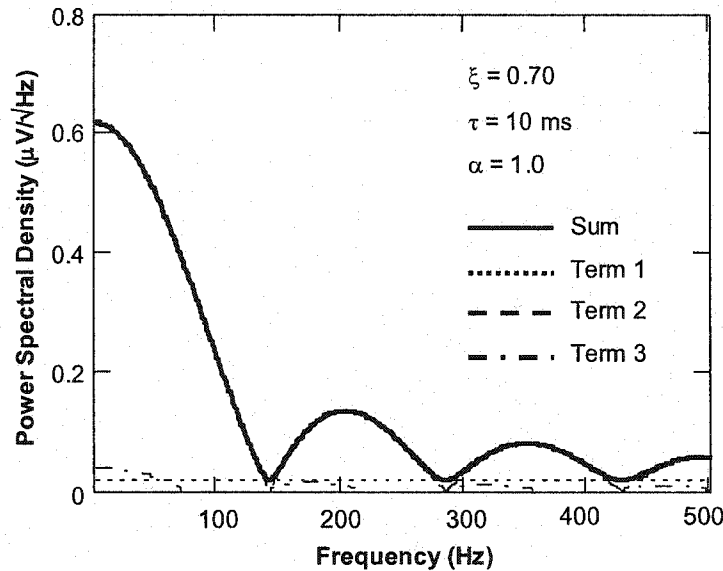
Figure 68. Reset noise PSD for different reset pulse periods.

As TFT ON resistance increases, the reset noise spectrum deviates from the familiar $\text{sinc}^2(x)$ function and this is accounted for by the other two terms in eqn (16). In the next figure, the magnitudes of all three terms are plotted along with the total reset noise PSD for two types of a-Si TFT switches. Figure 69(a) shows the reset noise components for an in-house fabricated TFT ($W/L = 60/25$, $C_G = 25 \text{ nF/cm}^2$) with a 100 Hz gate pulse of +5/0V magnitude at a 30% duty cycle. The second curve in Figure 69(b) depicts the reset noise using a state-of-the-art a-Si TFT switch. The α factor seen in the figures is a correction factor for any additional noise and will be discussed later in the measurement section.

Evidently, for an a-Si TFT switch with a gate bias pulse of 5 V, the magnitude of the first term is comparable to the second term, which changes the noise floor and deviates considerably from the ideal result predicted by eqn. (21). However, when a gate voltage of +15 V/ 0 V is applied to a state-of-the-art TFT as shown in Figure 69(b), the second term dominates and the situation appears much closer to ideal. Thus, if a state-of-the-art a-Si TFT is to be used in a noise-vulnerable medical imaging application, its reset noise performance should be close to ideal although evaluation of the integral in eqn. (16) is the only way to get the exact magnitude.



(a)



(b)

Figure 69. Dependence of the reset noise PSD on different terms in eqn. (16) for (a) in-house fabricated TFT with $V_G = +5$ V, $W/L = 60/25$ and (b) state-of-the-art TFT with $V_G = 15$ V, and $W/L = 50/5$.

Figure 70 depicts the effect of the duty cycle on the shape of the reset noise PSD for a pulse of 100 Hz using an a-Si TFT switch. Note that as the reset pulse duty cycle is reduced, the noise again begins to concentrate in a narrow band around the zero frequency. Also, the first and third terms in eqn. (16) tend to get suppressed and it appears that a small duty cycle pushes the reset noise towards its ideal value reported in eqn. (21). Again, for diagnostic

medical imaging applications, the duty cycle is very small (0.1% for real-time fluoroscopy) and hence the reset noise can be estimated as having its ideal value.

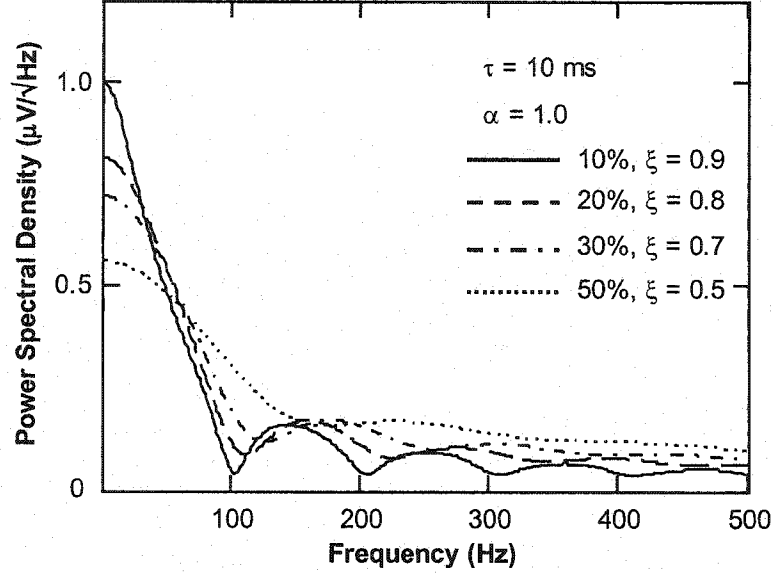


Figure 70. Reset noise PSD for different reset pulse duty cycles

To quantify some results for diagnostic medical imaging applications, assume a state-of-the-art TFT with a $W/L = 50/5$, $\mu_{EFF} = 0.8 \text{ cm}^2/\text{Vs}$, $C_G = 25 \text{ nF/cm}^2$ and a $V_G = +15/0 \text{ V}$ pulse operating at 30 Hz with a 0.1% duty cycle. Also, the integration node capacitance (C_{PIX}) is taken to be a nominal 0.75 pF. Reset noise voltages ($\langle v_n^2 \rangle$) are summarized in the table below for different gate voltages and C_{PIX} values.

Table 15. $\langle v_n^2 \rangle$ due to reset noise for duty cycles of 1 % or less.

$\langle v_n^2 \rangle$	$V_G = +5$	$V_G = +10$	$V_G = +15$
$C_{PIX} = 0.75 \text{ pF}$	6.696	6.696	6.696
$C_{PIX} = 2 \text{ pF}$	2.512	2.511	2.511
$C_{PIX} = 5 \text{ pF}$	0.9998	1.005	1.005

Since the reset noise values calculated in the above table are larger than the ideal value predicted by eqn. (21), it appears that a correction factor of 1.21 must be applied to eqn. (21) to accurately predict the noise for diagnostic medical imaging applications using a-Si TFTs.

The correction factor remained constant for duty cycles less than 1% (which is true for all diagnostic medical imaging modalities) and values of $\omega_f > 100$ kHz. So for a $C_{PIX} = 0.75$ pF, the RESET TFT ON-resistance must be less than 13 M Ω for the correction factor to be valid. For $\omega_f < 100$ kHz, the reset noise correction factor becomes smaller. Note that while increasing the TFT ON-resistance appears to decrease the reset noise, pixel reset time constraints (i.e. $5 \times R_{ON} \times C_{PIX}$ should be less than a few μs) must also be met for proper pixel operation.

5.4 Noise in the current-mediated APS

5.4.1 Thermal and Flicker Noise

During readout, the C-APS circuit of Chapter 2 reduces to a source follower stage with source degeneration as shown in Figure 71 where the READ TFT switch ON resistance provides the degeneration in the AMP TFT's source.

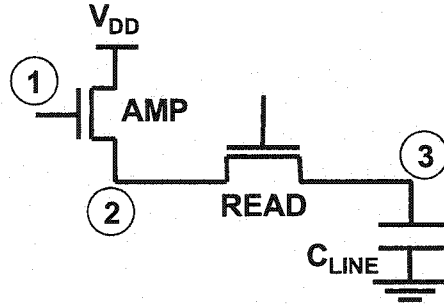


Figure 71. APS readout circuit schematic

The noise analysis is divided into two stages: the first is the noise that appears at the input of the charge amplifier and the second is the noise at the charge amplifier output. Modifying the small signal model to include independent noise sources, the equivalent circuit is shown in Figure 72 where a small signal noise voltage appears on the distributed column capacitance, C_{LINE} . Here, C_{PIX} is the sum of capacitances between the detector node and ground and C_{gs1} is the gate-source parasitic capacitance of the AMP TFT. In steady state, the AMP TFT operates in saturation while the READ TFT operates in the linear mode. Hence, the READ TFT switch is represented by its ON resistance $r_{ds2} = (1/g_{ds2})$. For simplicity, the

TFT switch ON resistance may be approximated as a constant given by $r_{ds2} = dI_{DS(lin)}/dV_{DS} \sim [K(V_G - V_T - V_{DS})]^{-1}$. In Figure 72, i_{n1} represents the noise current from the AMP TFT while i_{n2} represents the noise current from the READ TFT.

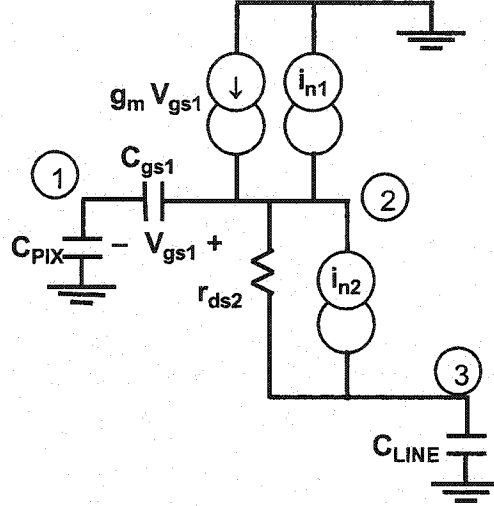


Figure 72. Small signal schematic of the APS readout circuit

A nodal analysis in the frequency domain ($s = j\omega$) of the equivalent circuit of Figure 72 yields the noise voltage at the output, V_3 :

$$V_3 = \frac{g_{ds2} \cdot i_{n1} (C_{PIX} + C_{gs1}) + i_{n2} (g_{m1} \cdot C_{PIX} + s \cdot C_{PIX} \cdot C_{gs1})}{g_{m1} \cdot g_{ds2} \cdot C_{PIX} + s(g_{m1} \cdot C_{PIX} \cdot C_{LINE} + C_{PIX} \cdot C_{gs1} \cdot g_{ds2} + C_{PIX} \cdot g_{ds2} \cdot C_{LINE} + C_{gs1} \cdot g_{ds2} \cdot C_{LINE}) + s^2 (C_{PIX} \cdot C_{gs1} \cdot C_{LINE})} \quad (22)$$

The above expression can be simplified by making some reasonable assumptions: $C_{LINE} \gg C_{PIX} \gg C_{gs1}$, and $s \ll g_{m1}/C_{gs1}$ (i.e. the operating frequency is much less than the pole created by the parasitic C_{gs1}). Thus, the above equation reduces to give the small noise voltage on C_{LINE} at the input of the charge amplifier as,

$$V_3 = \frac{i_{n1} \cdot R_{eq1} + i_{n2} \cdot r_{ds2}}{1 + j(\omega/\omega_{eq})}, \quad R_{eq1} = \left[g_{m1} \cdot \frac{C_{PIX}}{C_{PIX} + C_{gs1}} \right]^{-1}, \quad \omega_{eq} = \left[\frac{1}{C_{LINE}} \cdot \frac{g_{ds2} \cdot g_{m1}}{g_{ds2} + g_{m1}} \right]. \quad (23)$$

From eqn. (23), the voltage spectral density of the noise, S_{v3} , at the output may be expressed as,

$$S_{v3} = \frac{S_{in1} \cdot R_{eq1}^2 + S_{in2} \cdot r_{ds2}^2}{1 + (\omega/\omega_{eq})^2} \quad (24)$$

where $\omega_{eq} = 2\pi f_{eq}$ represents the bandwidth of the APS circuit, R_{eq1} is related to the transconductance of the AMP TFT, r_{ds2} is the ON resistance of the READ TFT switch, and

S_{in1} and S_{in2} are noise current spectral densities. The noise variance at the output, σ_3^2 , can be computed using thermal and flicker noise expressions suitable for a-Si TFTs. For thermal noise,

$$\sigma_3^2(th) = (f_{eq})(\pi/2)(R_{eq1}^2 \cdot a_{th1} + r_{ds2}^2 \cdot a_{th2}), \quad (25)$$

where $a_{th1} = (2/3) \cdot 4kT \cdot g_{m1}$, $a_{th2} = 4kT \cdot g_{ds2}$, f_{eq} is the circuit bandwidth and $(\pi/2)(f_{eq})$ is the classic noise bandwidth of a first order low pass filtering circuit.

For flicker noise,

$$\sigma_3^2(fl) = (R_{eq1}^2 \cdot a_{fl1} + r_{ds2}^2 \cdot a_{fl2}) \int_{f_{OBS}=1/T_{OBS}}^{\infty} \frac{1}{f \left(1 + \frac{f^2}{f_{eq}^2}\right)} df = (R_{eq1}^2 \cdot a_{fl1} + r_{ds2}^2 \cdot a_{fl2}) \left(\frac{1}{2}\right) \ln \left(1 + \frac{f_{eq}^2}{f_{OBS}^2}\right). \quad (26)$$

where a_{fl1} and a_{fl2} are flicker noise coefficients of the saturated AMP and linear READ TFTs respectively and T_{OBS} is the time of observation of the flicker noise [118]. Here, expressions for a-Si TFT flicker noise coefficients are simplified from section 6.1 with $n = 1$ as shown in [112][109]:

$$a_{fl1} = \frac{\alpha_{sat} \cdot q \cdot \mu_{EFF}^2 \cdot C_G \cdot (W/L)^2}{2(W \cdot L)} \cdot (V_G - V_T)^3, \quad a_{fl2} = \frac{\alpha_{lin} \cdot q \cdot \mu_{EFF}^2 \cdot C_G \cdot (W/L)^2}{(W \cdot L)} \cdot (V_G - V_T) \cdot V_{DS}^2. \quad (27)$$

However, when the APS is used in imaging applications, the READ TFT is pulsed causing the flicker noise performance to change. Here, double sampling is essential to perform offset and gain corrections for proper operation of the APS. With double sampling, the effect of V_T non-uniformities as well as any DC components including low frequency flicker noise [119] is mitigated. However, the thermal noise components from the AMP and READ TFTs, the reset noise and the amplifier noise are all increased since they are uncorrelated sources. Using $S_{v,3}$ and noting the thermal white noise sources are uncorrelated here, the output thermal noise with double sampling is:

$$\sigma_3^2(th) = \pi(f_{eq})(R_{eq1}^2 \cdot a_{th1} + r_{ds2}^2 \cdot a_{th2}), \quad (28)$$

Similarly, using previously derived results [119], the output flicker noise with double sampling becomes:

$$\sigma_3^2(fl) = 2I(x_{eq}) (R_{eq1}^2 \cdot a_{fl1} + r_{ds2}^2 \cdot a_{fl2}), \quad (29)$$

where $I(x_{eq})$ is an integral described in [119] that accounts for the band pass filtering effect of double sampling on flicker noise,

$$I(x_{eq}) = \int_0^{\infty} \frac{1 - \cos x}{x(1 + (x^2/x_{eq}^2))} \cdot dx, \quad (30)$$

Here, $x_{eq} = 2 \cdot \pi \cdot f_{eq} \cdot \tau_f$ and τ_f is the time between the pixel output and reset output samples. For small τ_f , the $I(x_{eq})$ function resembles a band pass filter that eliminates low-frequency and DC noise.

In the case where the output is not subject to double sampling, the contributions of the uncorrelated noise sources are that of the unsampled case. The output thermal noise without double sampling is written as in eqn. (25). Similarly, the output flicker noise for a single pulse reduces to eqn. (26). In this case, however, the observation time (T_{OBS}) is defined as the pulse width of the READ TFT sampling signal [118][119].

5.4.2 Reset Noise

The thermal noise of the RESET TFT ON resistance is low pass filtered by the pixel capacitance, C_{PIX} and stored on C_{PIX} during reset. Although it is possible to approximate this noise as, $\sigma_{reset}^2 = kT/C_{PIX}$, it is more accurate to include the effect of the feedback AMP TFT parasitic capacitance, C_{gs1} . Then the effective capacitance at the detection node becomes [119],

$$C_{eff} = C_{PIX} + (1 - A_{V0}) \cdot C_{gs1} \quad (31)$$

where A_{V0} is the DC gain of the AMP TFT buffer. Therefore the reset noise becomes,

$$\sigma_{reset}^2 = kT/C_{eff}. \quad (32)$$

Referring to Figure 72, the DC gain, $A_{V0} = V_2/V_1$, can be accurately estimated by including the AMP TFT ON resistance in saturation as $r_{ds1} = 1/(\lambda I_{DS})$,

$$\frac{V_2}{V_1} = A_{V0} = \frac{1}{\left(1 + \frac{1}{g_{m1} \cdot r_{ds1}}\right)}. \quad (33)$$

In addition, if double sampling is implemented, the reset noise voltage variance doubles to give $\sigma_{reset}^2 = 2kT/C_{eff}$. Note that the correction factor for reset noise discussed in the previous section must also be taken into account.

There has been some evidence [44] indicating that reset noise forms the major noise component in CMOS APS imaging pixels. The key point to note, of course, is that reducing the capacitance will reduce the noise electrons indicating that the APS would exhibit better performance with a small capacitance sensor at the integration node. The change in gain and reset noise for increasing pixel capacitance is illustrated in the figure below where V_{PIX} is the voltage change at the integration node due to input signal and reset noise components. The reset noise was calculated using eqn. (32) above including the correction factor discussed in the previous section. Evidently, a smaller C_{PIX} is desirable from a noise point-of-view.

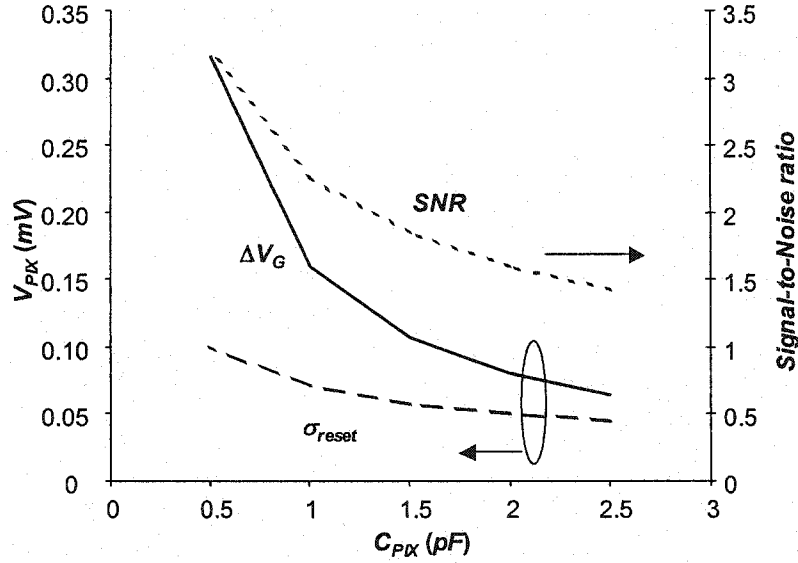


Figure 73. Variation in ΔV_G (for 1000 signal electrons) and reset noise (σ_{reset}) with C_{PIX}

5.4.3 Charge Amplifier Noise and Noise Gain

The amplifier noise at the input can be modeled as having a fixed noise component σ_{amp0} in addition to an input capacitance dependent component [120]:

$$\sigma_{amp} = \sigma_{amp0} + \delta C_d \quad (34)$$

Here δ is a constant determined by the design properties of the charge amplifier (e.g. input FET noise) and C_d is the external capacitance loading the amplifier input node. C_d is the sum of C_{LINE} and the internal amplifier input capacitance, C_{AMP} . A typical value for the amplifier noise (σ_{amp}) is about 1800 electrons [121] where $\sigma_{amp0} \sim 300$ electrons, $\delta = 15$ and $C_d \sim 100$ pF. Again, the presence of double sampling causes this noise to double.

To account for all of the noise at the amplifier input, noise sources from the C-APS readout circuit must also be considered. Then, the noise at the input of the charge amplifier (σ_{in_amp}) appears as shown in the figure below,

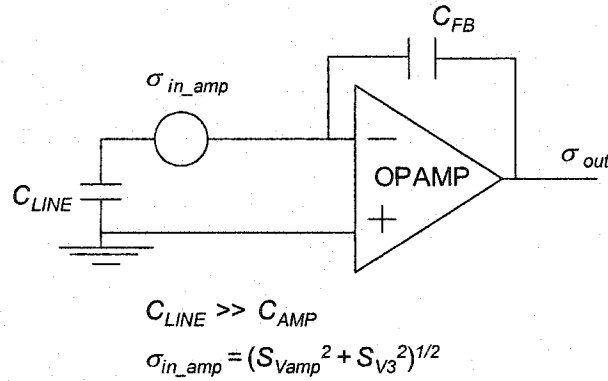


Figure 74. Circuit schematic to extract the noise gain ($1/\beta$) of the charge amplifier

Here, C_{LINE} is the distributed column line capacitance as before, and C_{FB} is the integrator's feedback capacitance. Note the C_{LINE} is assumed to be much larger than the amplifier's input capacitance, C_{AMP} . This is a reasonable assumption for large area arrays where C_{LINE} is typically anywhere from 50 – 200 pF. Assuming that the amplifier is ideal (i.e. open loop gain and input resistance are infinity and output resistance is zero), the noise gain function ($1/\beta$) can be written for the above circuit starting with,

$$\sigma_{in_amp} = \beta \sigma_{out} \quad (35)$$

Using a simple capacitive voltage divider to write σ_{out} in terms of σ_{in_amp} ,

$$\frac{1}{\beta} = \frac{C_{FB} + C_{LINE}}{C_{FB}} = 1 + \frac{C_{LINE}}{C_{FB}}. \quad (36)$$

So the noise gain is directly dependent on the ratio of the line and feedback capacitances. This is an interesting result because it reveals that reducing C_{FB} in order to increase the voltage gain (A_V) also results in a corresponding increase in noise gain ($1/\beta$). In order to get

a better SNR for the C-APS circuit, it is important to improve the *charge gain* (G_i) by reducing C_{PIX} and by maximizing g_m and T_S . Concurrently, the noise gain ($1/\beta$) needs to be minimized by keeping $C_{FB} \geq C_{LINE}$.

5.4.4 Total output noise and input referred noise

Since the various APS noise sources are uncorrelated, the noise on C_{FB} after double sampling becomes (using eqns. (28), (29), (32), (34) and (36)),

$$\sigma_{out}(tot)^2 = (A_V^2 \sigma_{Vreset}^2) + (1/\beta)^2 [\sigma_{v3}^2(th) + \sigma_{v3}^2(fl) + 2\sigma_{amp0}^2] \quad (37)$$

where A_V is the voltage gain of the current mediated APS and charge integrator circuit, determined in the Chapter 2, and restated below as,

$$A_V = g_m T_S / C_{FB} \quad (38)$$

Note that since the reset noise occurs at the same node as the signal, the charge gain increases both the reset noise and the sensor input signal in a similar fashion. $\sigma_{out}(tot)^2$ can be referred back to the input of the APS at the gate of the AMP TFT to give $\sigma_{input}(tot)$.

$$\sigma_{input}(tot) = \frac{\sqrt{\sigma_{out}(tot)^2}}{A_V}, \quad (39)$$

For the purposes of charge gain, it is beneficial to examine the noise from the standpoint of number of electrons. From eqn. (37) and eqn. (39), noise equivalent electrons at the output of the charge amplifier, $NEQ(output)$ and at the APS integration node, $NEQ(input)$ can be determined. Here, q denotes the electron charge,

$$NEQ(output) = \frac{\sqrt{\sigma_{out}(tot)^2} \cdot C_{FB}}{q} \quad (40)$$

$$NEQ(input) = \frac{\sqrt{\sigma_{out}(tot)^2} \cdot C_{PIX}}{A_V \cdot q} = \frac{\sqrt{\sigma_{out}(tot)^2} \cdot C_{FB}}{G_i \cdot q}. \quad (41)$$

5.4.5 Measurements and Discussion

The APS noise measurements were carried out for the fabricated test a-Si APS device of Chapter 2 as shown in Figure 75. V_G , V_{DD} and V_{RD} (the READ TFT bias) were all provided by high amp hour DC batteries while an ac-coupled Perkin-Elmer 5182 transimpedance

amplifier was used to amplify the noise signal to levels readable by the HP 3562A spectrum analyzer. The RESET TFT gate was grounded during this measurement. The AC gain of the amplifier was set at 10^8 for a bandwidth of 20 kHz. The noise measurement setup is shown in Figure 62(a). All noise power curves were reconstructed from narrowband measurements averaged at least 25-50 times and higher for low frequencies. The system noise was at least one order of magnitude lower (at high frequencies) than the APS output noise and was subtracted from each measured power spectrum. For each measurement, acquisition began a half hour after application of the bias voltages to allow the APS bias current, I_{OUT} and the noise to stabilize.

To extract input noise voltage PSD (V^2/Hz), the system (i.e. APS readout circuit plus the transimpedance amplifier) voltage gain had to be measured over all frequencies of interest for each biasing arrangement. Then, the measured gain was used to adjust the output noise voltage PSD to obtain the input noise PSD at the gate of AMP TFT. Figure 75 shows the input noise PSD for a couple of APS biasing arrangements. The measured data appears to be in good agreement with the theory. The values of the Hooge coefficients used here are extracted from single TFT noise data, where $\alpha_{sat} \sim 0.013$ for TFTs in saturation and $\alpha_{lin} \sim 0.008$ for TFTs operating in linear.

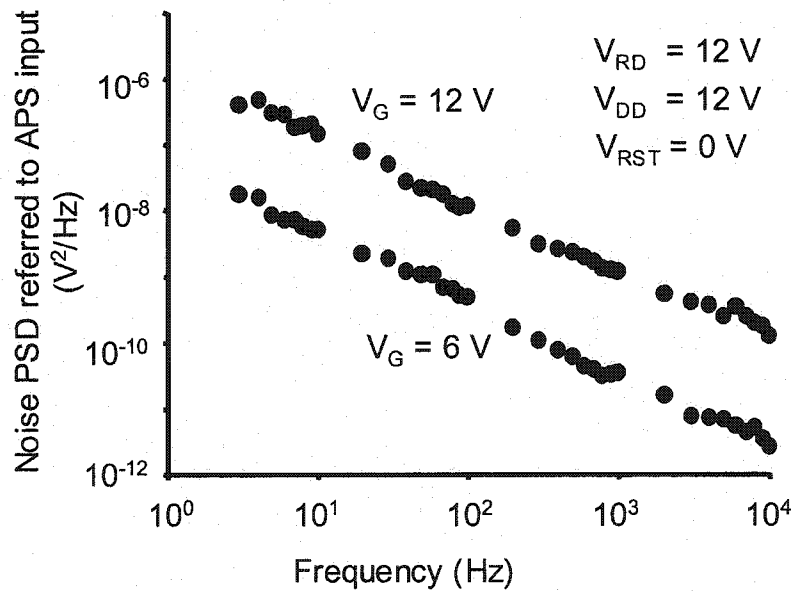


Figure 75. APS Noise PSD for different AMP TFT gate bias values

Integrating the area under the noise curves gives the input referred noise voltage for the APS in a wideband configuration. The lower limit of the integration, in this case, is arbitrarily chosen to be the HP3562A lower bandwidth limit of 64 μHz . Even lower limits could be used but the logarithmic term in the integration significantly reduces the effect and hence, relevance, of this lower limit. The upper limit is chosen as the noise bandwidth, $(\pi/2)f_{eq1}$ defined previously where the APS is directly connected to a charge amplifier. Table 16 contains noise data for each biasing arrangement where the input noise voltage appears to increase with increasing AMP TFT bias (V_G) but decreases with increasing READ TFT bias (V_{RD}). This follows directly from the noise voltage PSD expressions for the Hooge theory of flicker noise where the flicker noise voltage PSD is directly proportional to TFT gate voltage in the saturation region but inversely proportional to the TFT gate voltage in the linear region as shown in Table 13.

Table 16. Input referred noise voltage for different supplies

Biasing ($V_{DD} = 12$ V, $V_{RST} = 0$ V)	Input noise voltage (mV_{rms})	Midband gain
$V_{GS} = 6$ V, $V_{RD} = 12$ V	0.50	6.5
$V_{GS} = 8$ V, $V_{RD} = 12$ V	1.0	7.0
$V_{GS} = 12$ V, $V_{RD} = 12$ V	3.24	6.0
$V_{GS} = 12$ V, $V_{RD} = 18$ V	1.29	12.0

From Figure 75, it is evident that the noise of the APS is dominated by flicker noise of the AMP and READ TFTs. However, when the APS is used in imaging applications, the READ TFT is pulsed causing the flicker noise to reduce somewhat. In addition, for APS circuits used in digital imaging, double sampling, used to perform offset and gain corrections for proper operation of the APS, mitigates the effect of V_T non-uniformities as well as any DC components including low frequency flicker noise. Using the theory presented in this

section, the results of an APS input referred noise analysis with *double sampling* is presented in Table 17 and appears promising for diagnostic medical imaging (particularly for real time fluoroscopy where the minimum signal is only 1000 electrons). The benefits of selecting a small C_{PIX} are evident in that not only does the reset noise decrease but the charge gain also increases. Here, a state-of-the-art a-Si TFT process was assumed with a $\mu_{EFF} = 0.8 \text{ cm}^2/\text{V.s}$, $C_G = 25 \text{ nF/cm}^2$, $V_{DD} = 12 \text{ V}$, $C_{LINE} = C_{FB} = 100 \text{ pF}$, $T_S = 28 \text{ }\mu\text{s}$, and $N_{amp} = 1000$ electrons. The SNR was calculated using the minimum signal of 1000 electrons for fluoroscopy. A T_S of $28 \text{ }\mu\text{s}$ is acceptable for double sampling if the 1000×1000 pixel fluoroscopic array has charge amplifiers on both ends of the column. Two sets of charge amplifiers working concurrently effectively doubles the time available for sampling from $33 \text{ }\mu\text{s}$ to $66 \text{ }\mu\text{s}$. So each reset sample and signal sample is allotted $28 \text{ }\mu\text{s}$ while $10 \text{ }\mu\text{s}$ is allocated to letting any transient currents settle and resetting the pixel.

Table 17. Input referred APS noise in an imaging array with double sampling

Noise at input	NEQ (electrons) ($C_{PIX} = 0.5 \text{ pF}$)	NEQ (electrons) ($C_{PIX} = 1 \text{ pF}$)
Charge Gain (G_i)	61.6	30.8
W/L_{AMP}	150/15	200/20
Thermal	183	357
Flicker	475	654
Reset	434	618
Amplifier	46	92
Total Noise (input)	649	943
SNR (dB)	3.75	0.51

Note that to achieve the low noise performance shown in the previous section, a large AMP TFT is required to reduce the flicker noise contribution. Here, an $\alpha_H = 0.01$ is assumed for the Hooge coefficient. The α_H value of 0.01 for a-Si TFT flicker noise was reported in [109][110] and is slightly lower than the value measured from our in-house TFTs presented in this chapter. As seen in the section for TFT noise, the flicker noise for a TFT in saturation

can be much higher than for a TFT operating as a switch. For the data presented in Table 17, a $W/L = 150/15$ was used for the saturated AMP TFT ($C_{PIX} = 0.5$ pF) to minimize its flicker noise contribution while the READ and RESET TFT switches were kept at a nominal 100/10 and 50/10 for low leakage.

Next, the following figure highlights the importance of choosing an appropriate C_{FB} to minimize the noise gain at the input of the charge amplifier. Note that the large input referred noise for ($C_{LINE}/C_{FB} > 1$) begins to drown out the minimum signal of 1000 electrons in fluoroscopy. Here a $C_{LINE} = 100$ pF and a $C_{PIX} = 0.5$ pF is assumed. All other parameters are the same as for Table 17.

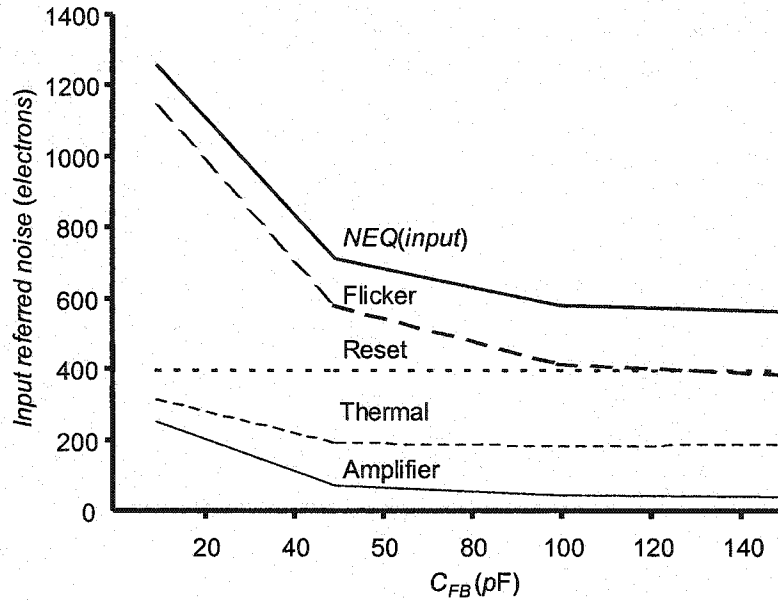


Figure 76. Change in input referred noise components with increasing charge integrator feedback capacitance C_{FB} . Here, C_{LINE} has been set to 100 pF.

The design summary for a low-noise, ΔV_T invariant, high gain, a-Si C-APS for real-time fluoroscopic performance can be summarized as shown in the following Table 18. In order to design a pixel for real-time fluoroscopy, a reset time of $< 2 \mu s$ can be obtained for a $C_{PIX} = 0.5$ pF by choosing a fairly small RESET TFT ($W/L = 50/10$, $\mu_{EFF} = 0.8 \text{ cm}^2/\text{Vs}$) with a gate pulse of +15/−5 V. Here, the need for a small ON resistance for lower reset noise and faster resets is met via the large TFT ON state bias of +15 V. The TFT's long L and small W

coupled with a -5 V OFF state bias can be chosen to minimize leakage currents, I_{OC} and I_{BC} [46].

Table 18. Design summary for C-APS circuit (I_{OC} and I_{BC} are leakage currents due to ohmic conduction and the TFT back channel)

	AMP	READ	RESET
Gain	$(W/L)_{AMP} \uparrow$ – high g_m	$(W/L)_{READ} \uparrow$ – high g_m	$(W \times L)_{RESET} \downarrow$ – small transient voltage spike at node A
Noise	$(W \times L)_{AMP} \uparrow$ – small σ_f $(W/L)_{AMP} \uparrow$ – small σ_{th}	$(W \times L)_{READ} \uparrow$ – small σ_f $(W/L)_{READ} \uparrow$ – small σ_{th}	$(W/L)_{RESET} \uparrow$ – ideal σ_{reset}
ΔV_T	$(W \times L)_{AMP} \gg (W \times L)_{READ}$ – small transient voltage spike at node B	n/a	n/a
Speed	n/a	$(W/L)_{READ} \uparrow$, $L_{READ} \downarrow$ – small transient current duration	$(W/L)_{RESET} \uparrow$ – small τ_{reset}
Leakage	n/a	$(W/L)_{READ} \downarrow$ – small I_{OC} & I_{BC}	$(W/L)_{RESET} \downarrow$ – small I_{OC} & I_{BC}

For high gain, low noise, and immunity to ΔV_T , the AMP TFT must be designed to be as large as possible. Here, the choice of a W/L is dictated mostly by the pitch requirements of $250 \mu\text{m}^2$ pixels for digital fluoroscopy. Since the READ TFT is operated as a switch in the linear mode, its flicker noise is much smaller than the AMP TFT and hence the large size constraints can be relaxed. For low leakage, the READ TFT can be made fairly small and in addition, the requirement for a small ON resistance (lower thermal noise, higher gain, small transient current duration) can be met satisfactorily by using a $+15$ V/ -5 V gate pulse as in the case of the RESET TFT. The circuit performance table shown in Table 17 used a $W/L = 150/15$ for the AMP TFT and a $W/L = 100/10$ for the READ TFT to achieve good results for the C-APS circuit. Here, for a $C_{PIX} = 0.5$ pF and a supply $V_{DD} = +12$ V, a $G_i = 62$ was achieved. The high G_i yielded an $SNR = 3.75$ dB for 1000 signal electrons implying that theoretically, an a-Si C-APS circuit can detect the minimum fluoroscopic input signal. A number of APS noise results presented in this section have been published in [52][53][54].

Chapter 6. Amorphous silicon

APS X-ray detector

This chapter describes the design, implementation and preliminary test results from a 2 x 2 pixel a-Se photoconductor, a-Si C-APS x-ray imager. The a-Si TFT array was fabricated using the in-house process described in Chapter 3 while the sensor material (a-Se) and top contact were deposited at the University of Saskatchewan. The array design is based on the C-APS circuit presented previously in Chapter 2.

6.1 C-APS Array Design

6.1.1 Circuit Performance

Designing the C-APS pixel gain value requires examining with the Burr-Brown IVC102 charge amplifiers that run on a supply voltage of +/-15 V and have a $C_{FB} = 10$ pF. The charge amplifier supply voltage and C_{FB} are particularly important considerations for the C-APS gain since a large output current (I_{OUT}) from the APS readout circuit can saturate the integrator as discussed in Chapter 2. From the IVC102 data sheet, the voltage at the output of the charge amplifier can swing from +13.3 V to -12.4 for a +/- 15 V power supply. In the C-APS case, since I_{OUT} is going from the APS readout circuit into the charge integrator, the output ramps negatively and thus, the largest achievable V_{OUT} before the integrator saturates is -12.4 V. For a constant APS current (I_{OUT}) during readout, the voltage at the output of the charge amplifier is expressed as,

$$V_{OUT} = (I_{OUT}T_S)/C_{FB}, \quad (1)$$

where T_S is the sampling time of the charge integrator. The maximum allowable I_{OUT} can now be calculated for different values of T_S . For example, at a $T_S = 80 \mu\text{s}$, the charge integrator will saturate for $I_{OUT} > 1.55 \mu\text{A}$. Similarly, for a $T_S = 40 \mu\text{s}$, the charge integrator will saturate for an $I_{OUT} > 3.1 \mu\text{A}$.

Keeping the allowable values of I_{OUT} in mind, the C-APS readout circuit is designed for the maximum g_m as a function of supply voltage (V_{DD}) and TFT aspect ratios (W/L). Based on the above constraints, the g_m was designed using the theory presented in Chapter 2 and a-Si circuit simulations. For AMP and READ TFTs with $W/L = 12$, $\mu_{EFF} = 0.3 \text{ cm}^2/\text{V.s}$, $C_G = 25 \text{ nF/cm}^2$, $V_{DD} = 12 \text{ V}$, $V_{RD} = +12$, simulations predicted a $g_m = 0.5 \mu\text{S}$ and $I_{OUT} = 1.3 \mu\text{A}$. Therefore, with an IVC102P $C_{FB} = 10 \text{ pF}$ and a $T_S = 80 \mu\text{s}$, the voltage gain is estimated to be around 4 V/V for a C-APS readout circuit coupled directly to the charge integrator.

The charge gain (G_i) for the designed C-APS circuit can be extracted if the C_{PIX} value is known. C_{PIX} was made particularly large for the fabricated C-APS imager in order to avoid any detrimental charge sharing effects at the integration node. The charge injection error is due to the RESET TFT channel charge and parasitic overlap capacitance ($C_{GS} \sim 150 \text{ fF}$ in the implemented process) when the TFT turns OFF. Even with the precautions of a large C_{PIX} , measurements on a pixel in a sister array yielded a voltage drop of $\sim 2 \text{ V}$ at the integration node (for a $V_{DD} = 12 \text{ V}$ and a $V_{RST} = +16/0 \text{ V}$) when the RESET TFT was switched OFF.

The various components of C_{PIX} are summarized in Table 19. Using a pixel capacitance value of 3.03 pF , G_i is extracted to be 13.3. Measurements on a pixel in a sister C-APS array yielded a value for C_{PIX} that was larger by about 25%. The measurements were carried out by first, inserting a $10 \text{ G}\Omega$ resistor in parallel with the storage capacitor, resetting the pixel once and then intermittently reading out the output until it settled indicating the integration node had discharged completely. The measurement error is attributed largely to any parasitic capacitances added by the external $10 \text{ G}\Omega$ resistor.

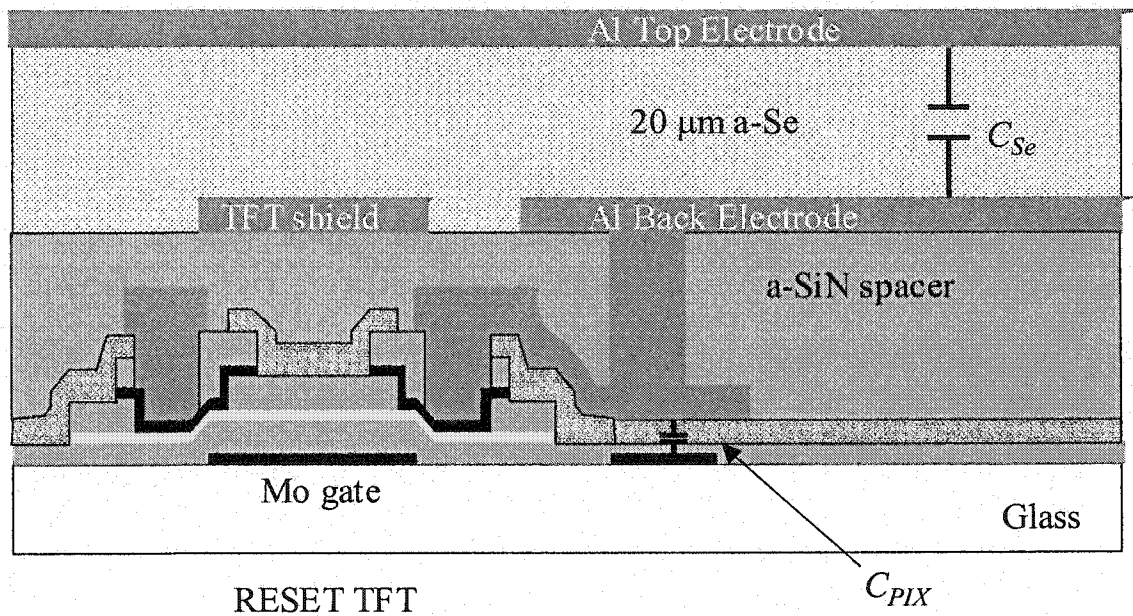
Table 19. Components of C_{PIX}

C_{PIX} components	Capacitance (pF)
a-Se sensor capacitance (500 x 500 μm pixel, 40% geometrical fill factor, 20 μm thick, $\epsilon_{Se} \sim 6.5$)	0.29
AMP TFT gate capacitance ($W = 250 \mu\text{m}$, $L = 25 \mu\text{m}$, $C_G = 25 \text{ nF/cm}^2$, $C_{G \text{ AMP}} = WLC_G$)	1.56
Storage Capacitor (400 x 25 μm area, 450 nm thick, $\epsilon_{SiN} \sim 6$)	1.18

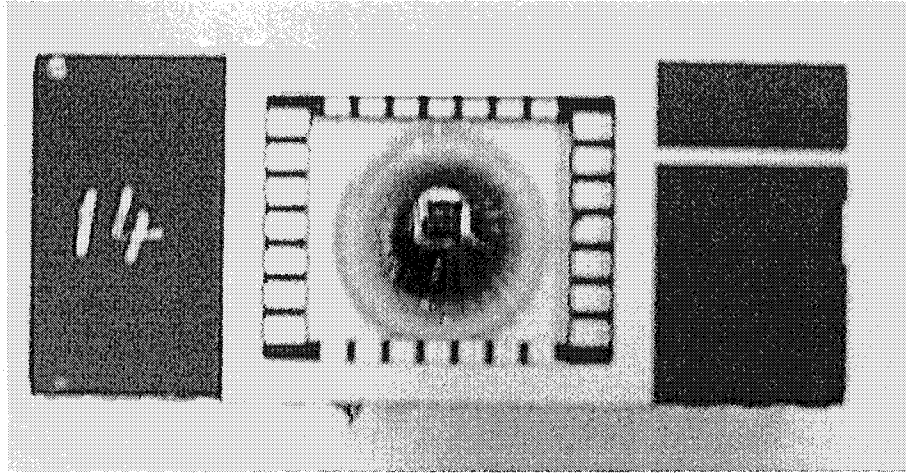
6.1.2 a-Si TFT backplane process

The TFT process has been described in Chapter 3 along with the process modifications required to interface the TFT readout circuit array to an a-Se photoconductor. A cross-section of the TFT process after Se deposition and a picture of the a-Se APS imager chip is shown in Figure 77 below. Since the a-Se photoconductor is a continuous layer sensor, charge accumulating at the bottom of the a-Se photoconductor during x-ray signal integration can cause an increase in the underlying TFT's leakage current. Thus, a grounded TFT shield, as shown below, is placed above the TFT channel to consistently maintain a low value of TFT leakage current.

A die micrograph of the C-APS TFT array for integration with the a-Se photoconductor was shown previously in Chapter 3. Here, a grounded guard ring encircles the test array in order to focus the electric field between the a-Se top contact and TFT array to the C-APS pixel region (approximately a 1 mm x 1 mm square area).



(a)



(b)

Figure 77 (a) Cross-section of a-Se sensor and C-APS array (b) Photograph of complete C-APS chip with a-Se and Al top contact

6.1.3 Selenium photoconductor and Al top contact process

20 μm of selenium were thermally evaporated on a wire-bonded chip (containing an a-Si C-APS array) using a boat temperature of 265°C, a pressure of 1-2 μTorr and a substrate (chip) temperature of 25 °C. After the deposition, the layers were annealed for 1 hour in vacuum. The a-Se layer is visible as the large, dark, circular area surrounding the die in the top view of the chip shown in the Figure 77(b). A shadow mask was designed to permit the evaporation of a-Se as shown in the following Figure 78.

The top contact to the a-Se layer is made up of a thin thermally evaporated Al layer (10-30 nm). Al was picked as the material of choice since it could be evaporated and it gave a relatively low dark current with selenium [123]. Although gold (Au) gives a better dark current than Al [123], sputtering Au (a ballistic process) was not feasible since the chip had many exposed, sensitive bond wires. Tight control was maintained over the deposition area of the Al top contact via a custom designed collimator. The dimensions of the collimator were precisely controlled since it was essential to deposit the Al layer only over the imaging pixels and not over any circuit bondpads on the die (which could cause shorts in the array).

Dark current on both the tested a-Se APS array and a sister sample without any TFT backplane was measured. While the sister sample had a dark current density, $J_{\text{dark}} = 2$

nA/cm² (measured by G. Belev at the University of Saskatchewan), the a-Se on the APS array yielded a much larger $J_{dark} = 83 \text{ nA/cm}^2$ at an applied electric field of $-1.8 \text{ V/}\mu\text{m}$ for a $20 \mu\text{m}$ a-Se thickness. J_{dark} was extracted from I_{dark} , which was measured by inserting a picoammeter in series with the a-Se top electrode contact. I_{dark} found to be 0.5 nA for an approximately 0.6 mm^2 bottom electrode contact area. For a pixel area of $500 \mu\text{m} \times 500 \mu\text{m}$ and a geometrical fill factor of 40%, $I_{dark} = 83 \text{ pA/pixel}$. The large change in J_{dark} between the sister samples is attributed to differences in the back electrode preparation. The Al back electrode on the TFT array was sputtered at the University Of Waterloo under process conditions compatible with the in-house a-Si TFT process. In contrast, the sister sample's back electrode was deposited at the University Of Saskatchewan under conditions compatible with the a-Se process.

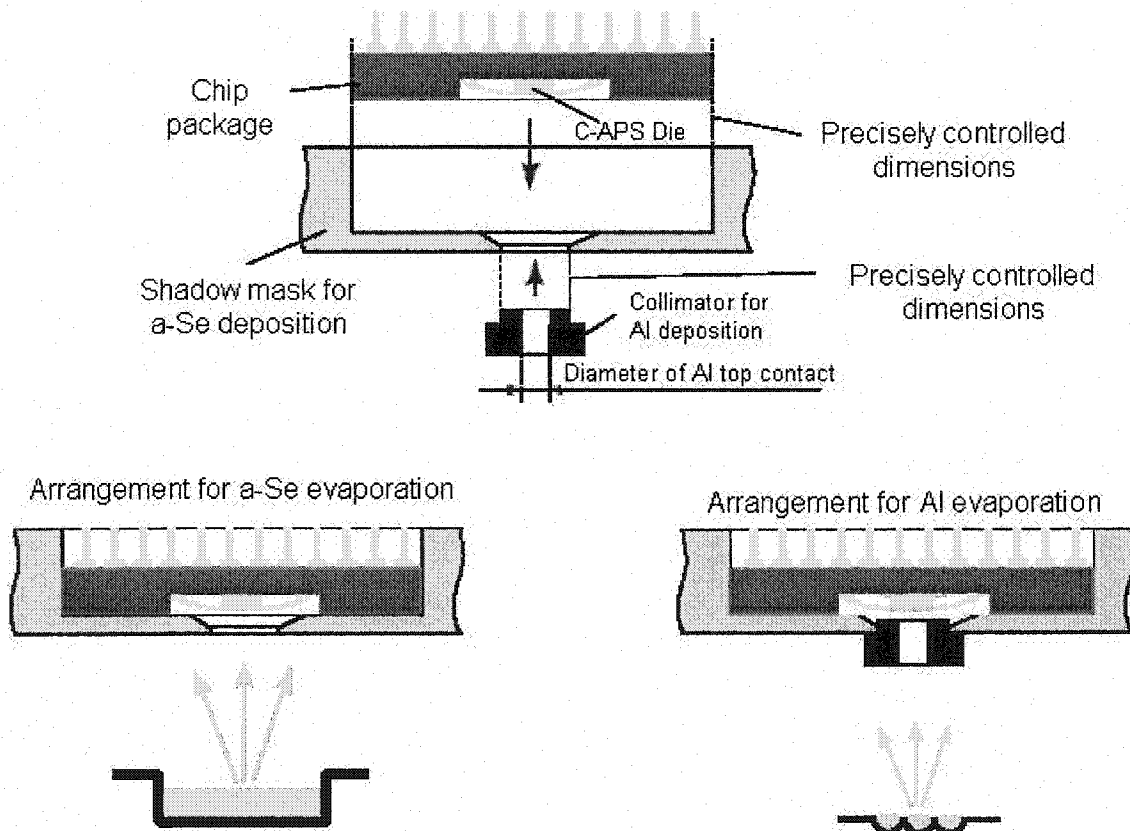


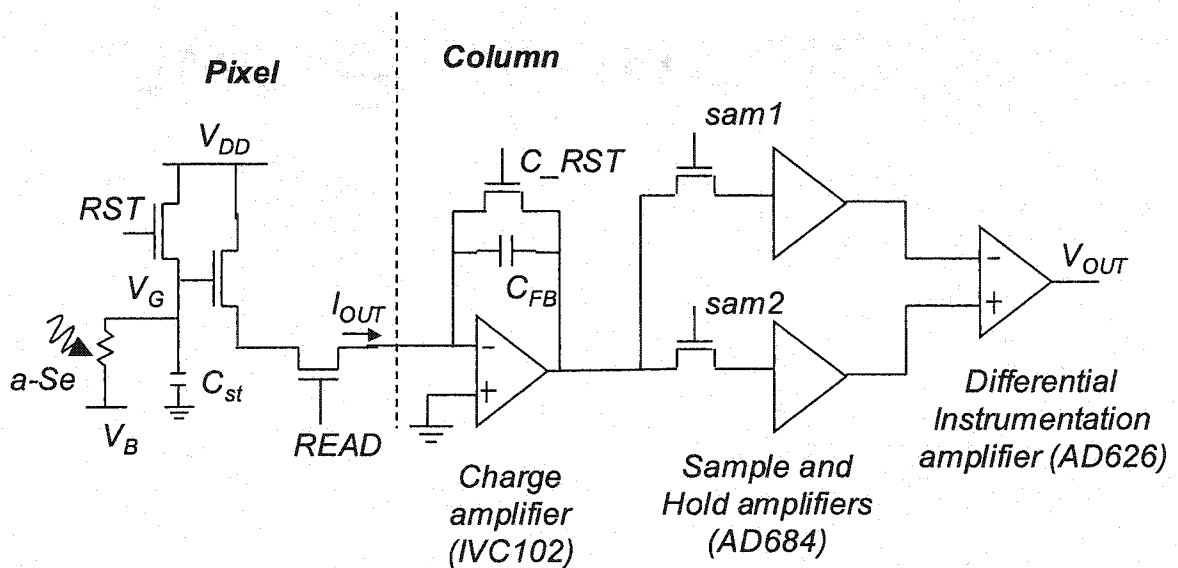
Figure 78. Deposition setup for thermally evaporated a-Se and Al top contact (courtesy of G. Belev and C. Koughia, University of Saskatchewan).

6.2 Test apparatus

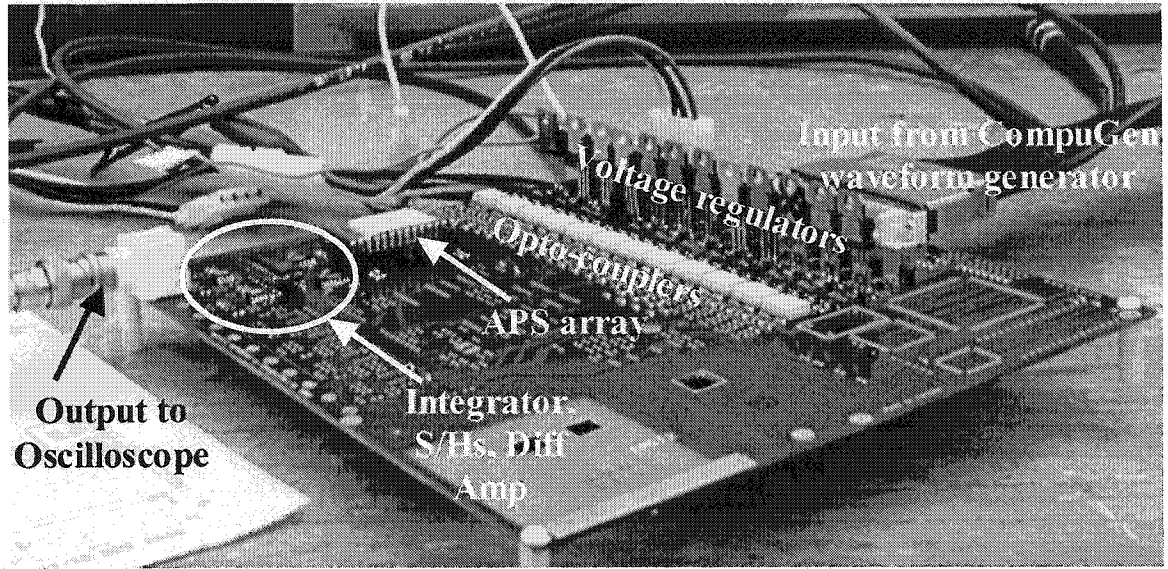
6.2.1 Test board design

The test board was designed using commercial off-the-shelf charge integrators, sample-and-hold circuits and differential amplifiers. Optically isolated pulse voltages form the input to the C-APS array and its associated readout electronics (via HCPL 315J opto-couplers). The power supplies to the board were provided by high amp hour, low noise, DC batteries. On board, positive and negative mode voltage regulators generated the different stable voltage levels required by the imaging array and various readout chips.

A computer controlled Gage electronics digital waveform generator (CompuGen 3250) generated the various digital CMOS/TTL level controlling waveforms to the circuit board. The optocouplers performed the dual function of isolating the imaging array from noise in the externally generated pulse waveforms as well as level shifting to the higher voltages required by the a-Si TFTs. For example, the optocouplers generated a +16/0 pulse voltage for the RST and READ TFTs that triggered upon receiving a CMOS level pulse from the CompuGen card located inside a PC. Figure 79(a) shows a circuit schematic of a C-APS imaging pixel directly coupled to an external charge integrator with on-board double sampling circuitry.



(a)



(b)

Figure 79. (a) C-APS test board schematic and (b) photograph of test board

The fabricated array consisted of 2×2 pixels and thus each column had two pixels connected to it. Figure 79(b) contains a photograph of the printed circuit board during initial testing.

6.2.2 Test waveforms

The array was operated via the CompuGen digital waveform generator where some pertinent waveforms for operating one pixel are shown in Figure 80. Here, *READ* and *RST* refer to the pulses applied to the gates of the READ and RESET TFT respectively. *C_RST* is the pulse that resets the charge integrator while *sam1* and *sam2* lock in the integrator output into two sample and hold circuits.

As evident from the waveforms, the integrator is continuously reset (*C_RST* is high mostly) unless there is a signal to integrate. In the APS readout circuit, when the READ TFT turns ON, there is an output current I_{OUT} . The integrator begins integrating I_{OUT} a bit after the READ TFT is turned ON (delay t_{dl} was chosen to be $20 \mu s$) in order to allow the TFT to fully turn ON and any transients to settle down. T_{INT} is the period of time during which x-rays generate signal charge that accumulate at the integration node (gate of the AMP TFT). T_S is the time over which I_{OUT} is integrated to develop a voltage across C_{FB} .

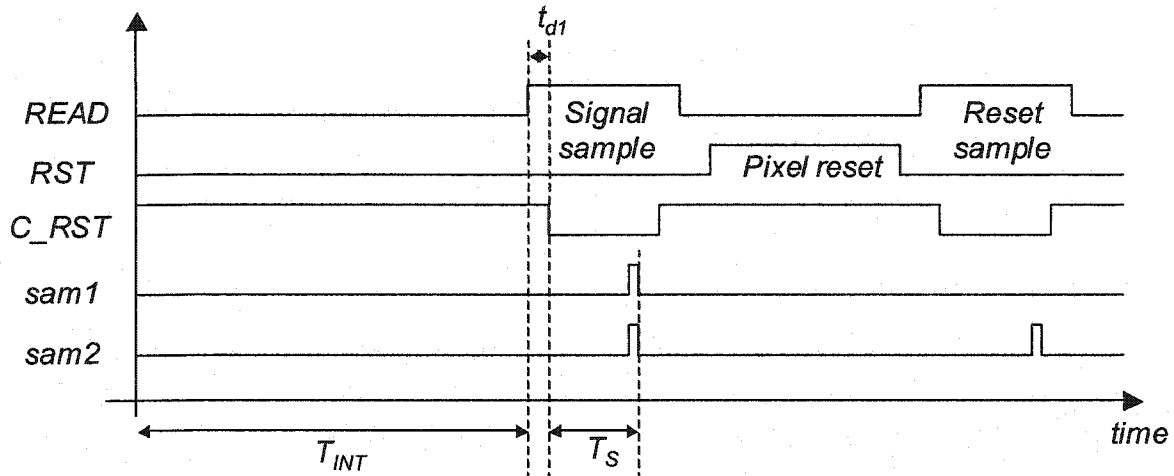


Figure 80. Waveforms used to operate one a-Se C-APS array pixel with double sampling

The waveforms in the Figure 80 above reflect the double sampling nature of the APS array. Initially, both sample-and-hold amplifiers obtain the value across C_{FB} after T_S . The pixel is then reset via the RST pulse and I_{OUT} is integrated once again. The integrated value of I_{OUT} across C_{FB} is sampled by $sam2$ into the second sample and hold circuit. Note that the second sample does not include the effect of x-ray generated signal charge and thus will be slightly different from the first sample. The differential amplifier at the end of the chain in Figure 79(a) subtracts the two samples (signal and reset), thus eliminating the effect of any dc offsets in the APS readout circuit and external readout electronics (including the bias dependent I_{OUT} mentioned in Chapter 2).

Figure 81 below is a screen photograph of a digital oscilloscope capturing the V_{OUT} of one column (i.e. reading out two pixels) of the APS imager. The V_{OUT} signal has been divided into four phases with alternate phases being related to the same pixel. The vertical scale is 20 mV/division while the horizontal scale is 2 ms/division. Here, an input (via on-board charge injection test circuits) was supplied to only one pixel during phase 1. The output is quite evident as being the large jump in voltage shown in phase 1 below. For both pixels when no test charge is injected (i.e. on phases 2, 3, and 4), the output stays relatively close (within 10 mV) to the zero value.

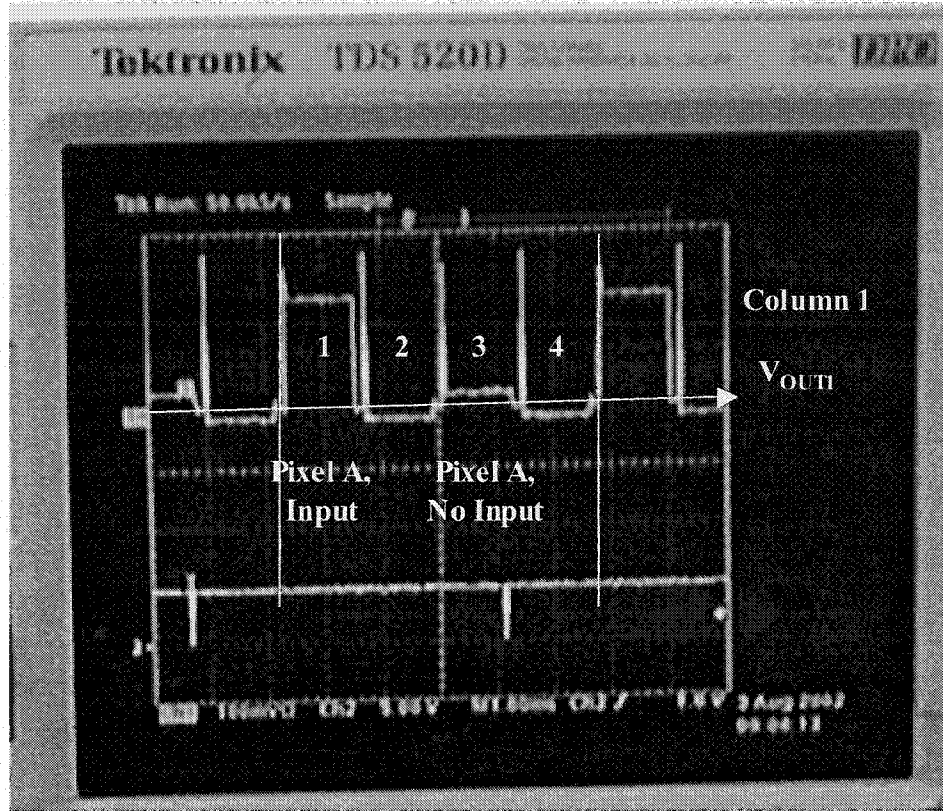


Figure 81. Screen shot of pixel column output with double sampling

6.2.3 X-ray test environment

The a-Se APS imaging array was tested with x-rays using the setup shown in Figure 82 below. Here, a lead shielded test chamber with an x-ray generation unit was used for sensitivity, gain and noise testing. A coiled wire wrap wire gently touching the top Al electrode provided a bias voltage to the a-Se layer. The coiled wire was soldered at the other end to a pin on the chip package, which was connected via the printed circuit board to an off board connector. Bias to the top electrode of the a-Se layer was provided via the off-board connector using high amp hour, low noise batteries to minimize measurement error.

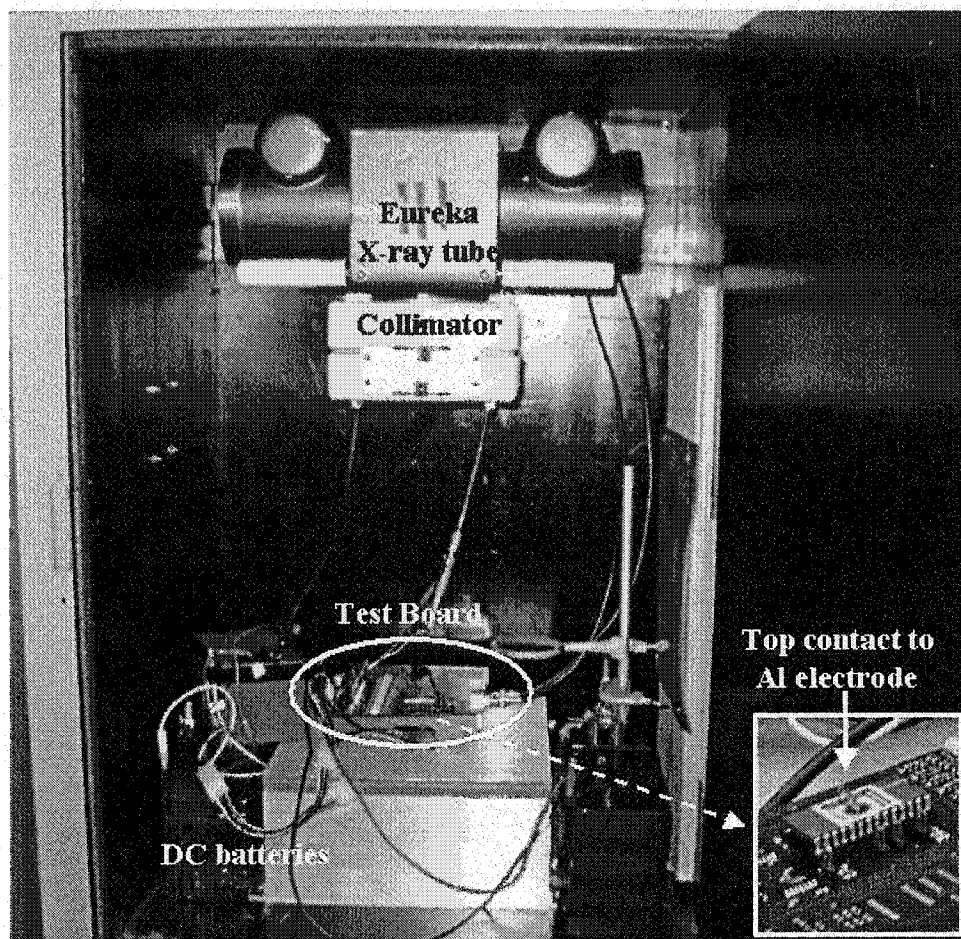


Figure 82. APS test board inside a shielded box for x-ray testing. The inset shows the a-Se APS array with the a-Se top bias electrode contacted via a coiled wire.

6.3 Results and discussion

6.3.1 X-Ray Source

The X-rays were generated by an Eureka RAD-8 rotating tungsten anode target tube located in an Emerald housing. X-ray spectrum simulation software (XRAYLIB) developed at the University of Western Ontario was used to predict and extract the incident photon data used for the calculation of sensitivity. The XRAYLIB software predicts the incident X-ray photon spectrum generated by a tungsten target tube based on an algorithm published in

[134][135]. The software was calibrated for the in-house X-ray generator and takes into account the inherent filtering (~ 1 mm of Al) due to the tube housing and the collimator. The source detector distance was 45 cm while dose was measured via a Solidose dosimeter. An example X-ray spectrum generated using XRAYLIB is shown below in Figure 83.

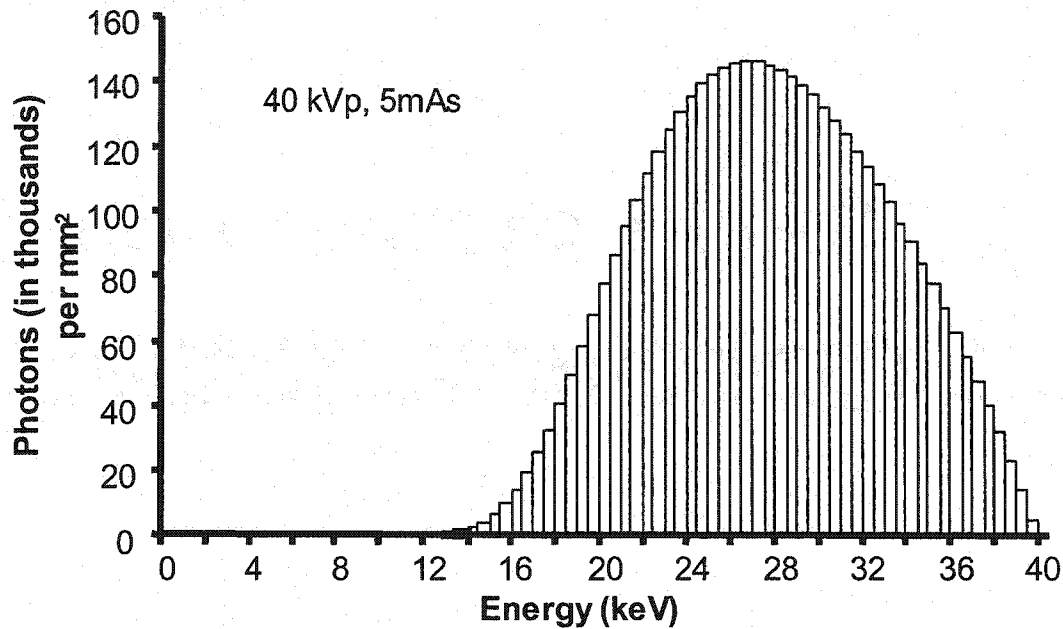


Figure 83. 40 kVp, 5 mAs spectrum generated by XRAYLIB

The error between the dosimeter and software was found to be less than 20% (possibly due to calibration error) for the range of spectra tested between 30 kVp and 70 kVp.

6.3.2 Quantum detection efficiency (A_Q) of the a-Se layer

In order to determine the number of electron-hole pairs generated in the a-Se layer for a given number of incident photons of varying energies, the absorption data of a-Se for a particular sensor thickness must be calculated. Data on the X-ray mass attenuation coefficient (μ/p) for Se from the NIST web site [137] coupled together with a-Se density data from [5] allowed determination of the a-Se attenuation length and absorption for the required range of photon energies. Although the a-Se used in the C-APS imager is alloyed with 0.5% Arsenic (to give stabilized a-Se [5]), the correction factor for the alloy is not significant and there is almost no difference between pure Se and stabilized Se with regard to their x-ray

absorption. The graph below depicts the attenuation length of selenium for photon energies of interest.

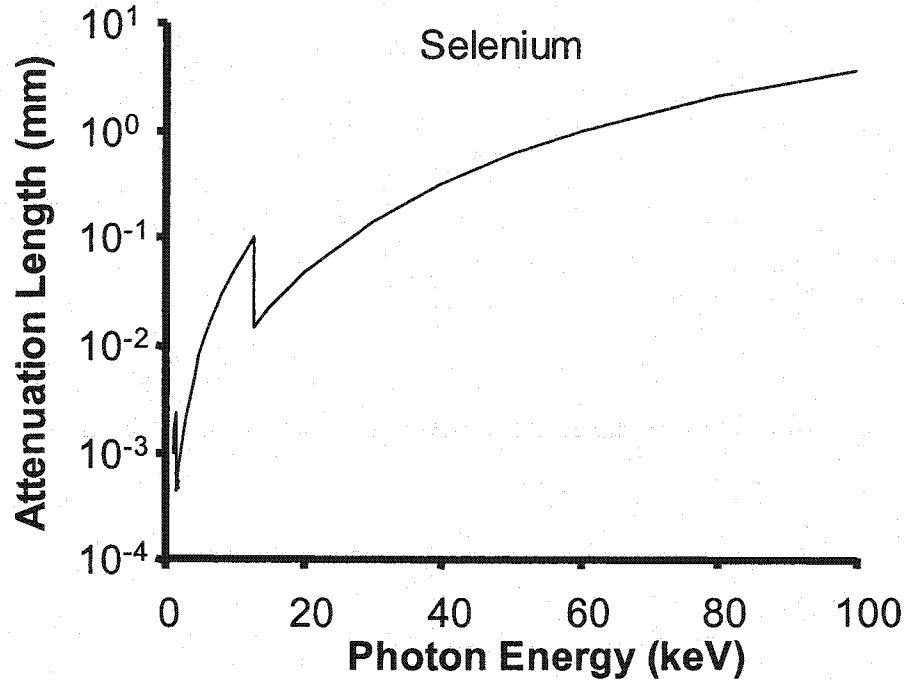


Figure 84. Attenuation length versus photon energy

In order to obtain the probability of interaction for an X-ray of energy E (i.e. the quantum detection efficiency, A_Q),

$$A_Q = 1 - \exp [-\mu(E,Z)T] \quad (2)$$

where $\mu[E,Z]$ is the energy and atomic mass dependent linear attenuation coefficient of a-Se and T is the thickness of the sensor. Since all practical x-ray sources for radiography are poly-energetic and emit x-rays over a spectrum of energies, A_Q must be specified at each energy value. $\mu[E,Z]$ is simply calculated from the Se mass attenuation coefficient data (available from the NIST web site) by multiplication with the density of a-Se [5]. The inverse of $\mu[E,Z]$ is the attenuation length shown in Figure 84. Using $\mu[E,Z]$, A_Q is plotted as a function of various a-Se thickness values in Figure 85 below where, as detector thickness increases, there is a higher likelihood of the x-ray being detected.

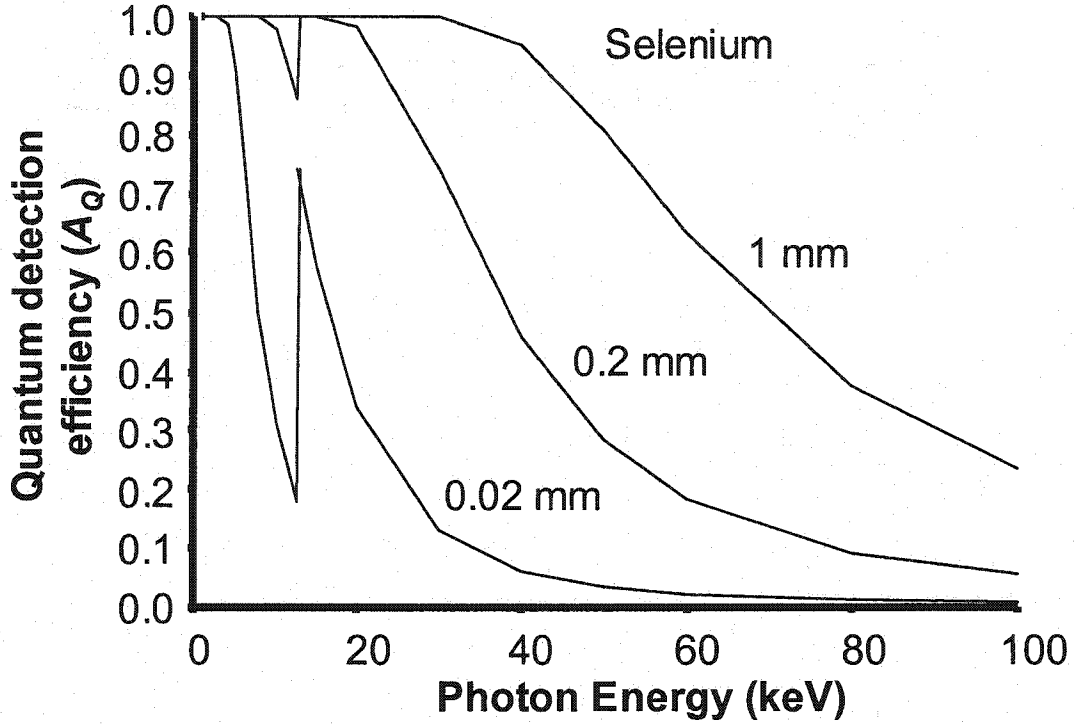


Figure 85. A_Q vs. photon energies for different sensor thickness

6.3.3 X-ray sensitivity

The x-ray sensitivity can be predicted from x-ray absorption and the a-Se conversion gain (i.e. the number of electrons generated per absorbed x-ray photon). The signal charge Q_P generated at each pixel of the detector can be approximated as [60],

$$Q_P = \int_0^{E_{\max}} \frac{\overline{\Phi_0}(E) A_Q A_P F_P}{W_{\pm}} E dE \quad (3)$$

Here, $\overline{\Phi_0}(E)$ is the mean number of x-ray quanta incident per unit area with energy E , A_Q is the quantum detection efficiency defined in eqn (2), A_P is the pixel area, F_P is the pixel fill factor, and $W_{\pm}$ is the electric field dependent energy required to free an electron-hole pair in a-Se. $W_{\pm}$ is given below for a typical a-Se photoconductor as [7],

$$W_{\pm} = 6 + 400/E, \quad (4)$$

where E is the electric field applied across the sensor and $W_{\pm}$ is given in eV.

Note that gain fluctuations [5] are not taken into account by eqn (3) above and in general, eqn. (3) represents an upper bound on the signal electrons generated in the a-Se sensor. Using x-ray spectra generated by XRAYLIB and the A_Q data shown in Figure 85, Figure 86 depicts the signal charge generated in a 20 μm a-Se photoconductor as a function of absorbed photons (a-Se sensitivity) for an $E = 1.8 \text{ V}/\mu\text{m}$, $A_P = (500\mu\text{m} \times 500 \mu\text{m})$, $F_P = 70\%$.

In contrast to the geometrical fill factor of around 40%, an averaged value of 70% is used for the *effective* pixel fill factor to account for the non-vertical electric field extending from the top electrode ($500 \times 500 \mu\text{m}^2$) to the back electrode ($400 \times 250 \mu\text{m}^2$) of the continuous, overlying a-Se x-ray detection layer. Here, the tube current and exposure time is kept constant (5 mAs) while the tube voltage is varied from 30 to 40 kVp. The a-Se conversion gain is around 100 for the range of x-ray tube and a-Se parameters tested. The gain seen in Figure 86 is less than the typical 1000 reported [5] for much thicker a-Se sensor layers (0.2 – 1 mm) and higher kVp (70-80 kVp) values used for fluoroscopic imaging.

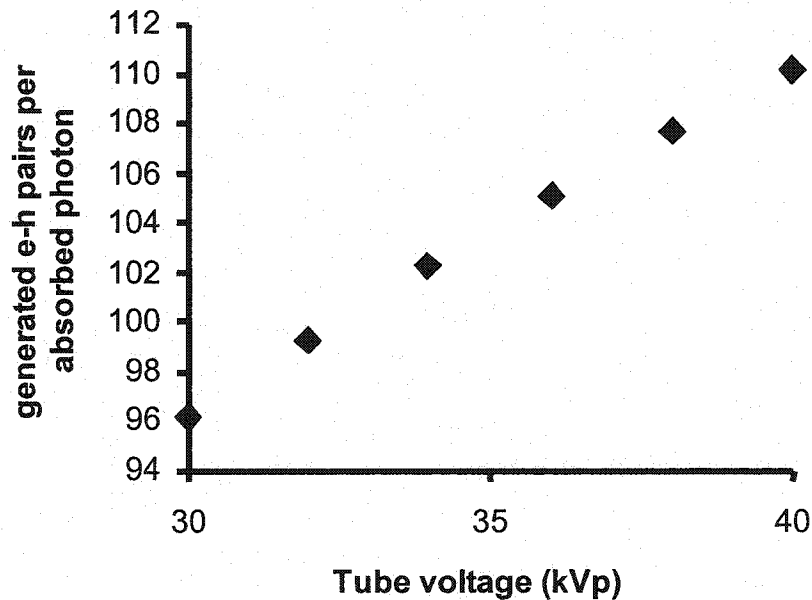


Figure 86. Signal charge generated per absorbed photon in 20 μm a-Se. The tube current was 50 mA while the exposure time was 100 ms.

6.3.4 C-APS output signal and circuit gain

The g_m of the C-APS pixels in the a-Se array was extracted prior to the a-Se deposition where most pixels had g_m values at least 30% smaller than the designed value of $0.5 \mu\text{S}$. In contrast, measurements on some sister samples yielded g_m values as low as $0.1 \mu\text{S}$. These large differences in pixel g_m values are attributed to variations in the in-house TFT fabrication process.

Based on the X-ray spectrum data from XRAYLIB and a-Se absorption curves presented previously, measurements of C-APS pixel output voltage (V_{OUT}) for different x-ray generated (from 30 to 40 kVp, 5 mAs setting) input charge electrons (Q_P) are shown in Figure 87 below. The pixel shown below has a gain of $0.86 \text{ mV}/1000 \text{ electrons}$ appearing at the output of the AD626 differential amplifier.

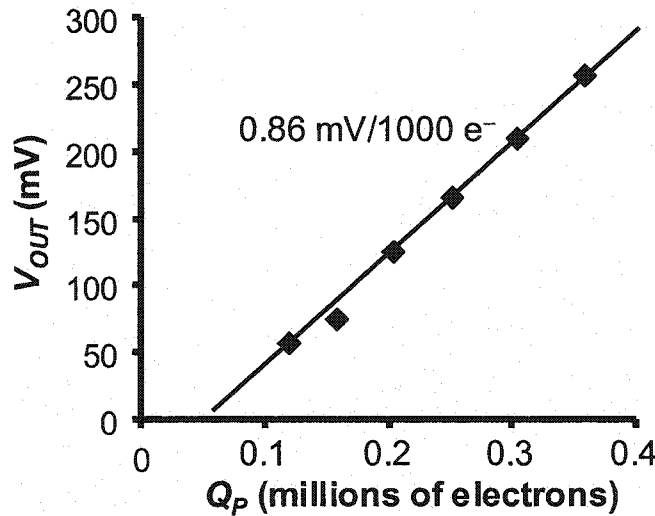


Figure 87. APS imaging pixel output voltage, V_{OUT} per x-ray photon generated electrons, Q_P (Test Chip #5, column 1, row B pixel). Here, $T_S = 80 \mu\text{s}$ and Q_P is calculated from eqn. (3) and XRAYLIB.

If the AD626 amplifier gain of 5 is removed, the C-APS readout circuit directly coupled to the IVC102 charge amplifier provides a gain of $172 \mu\text{V}/1000 \text{ electrons}$ at the IVC102 output. Then, G_i is obtained by converting the voltage at the integrator output into charge stored on C_{FB} . G_i appears to be around 10.5 as given by the slope of the line relating the input signal electrons (Q_P) to output electrons (Q_{OUT}) stored on C_{FB} shown in Figure 88. The

measured G_i value is smaller than the designed value (of 13.3 where $T_S = 80 \mu\text{s}$, $g_m = 0.5 \mu\text{S}$, and $C_{PIX} = 3.03 \text{ pF}$) by about 20% and the difference between the measured and predicted values is attributed to process variations in C_{PIX} and g_m values as well as to errors in the x-ray photon generated charge estimated by XRAYLIB.

Although the test board was shielded from the x-ray source in the preliminary testing, the small size of the C-APS die (2 mm) made it difficult to also completely shield the package while leaving only the active x-ray sensitive pixel area of the die exposed. Thus, there may be additional sources of electrons (e.g. due to generation in the exposed bond wires) and the extracted $G_i = 10.5$ is considered an optimistic result. To verify the a-Se photoconductor was working and that x-ray charge was being generated in the a-Se, the bias across the a-Se sensor was removed which caused a significant drop in the output voltage upon application of x-rays. The bias removal test confirmed that the a-Se photoconductor was the primary source of input charge at the integration node.

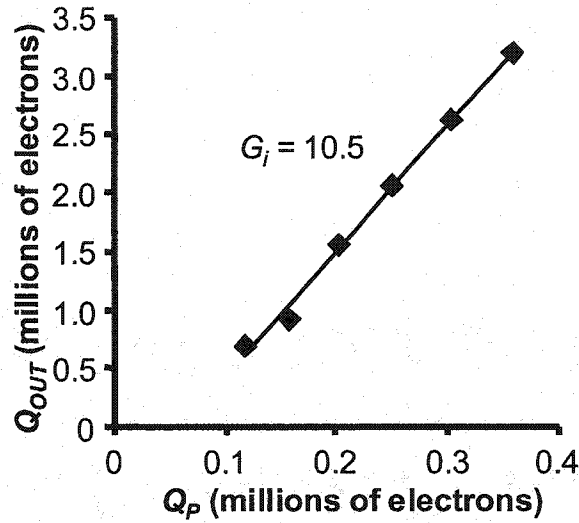


Figure 88. Measured G_i of the C-APS pixel (Test Chip #5, column 1, row B) at the output of the IVC102 integrator where $T_S = 80 \mu\text{s}$.

6.3.5 Dependence on T_S

As demonstrated in Chapter 2, the C-APS is programmable via sampling time, T_S . Figure 89 below depicts the linear behavior of V_{OUT} as T_S is increased from $60 \mu\text{s}$ to $100 \mu\text{s}$ for an x-

ray input signal of 120,000 electrons at the integration node (produced by a 30 kVp, 5 mAs setting on the x-ray generator). The linear relationship between T_S and V_{OUT} was noticed in all working pixels of the test array and illustrates the flexibility of the C-APS circuit in achieving a larger G_i by simply increasing the sampling window.

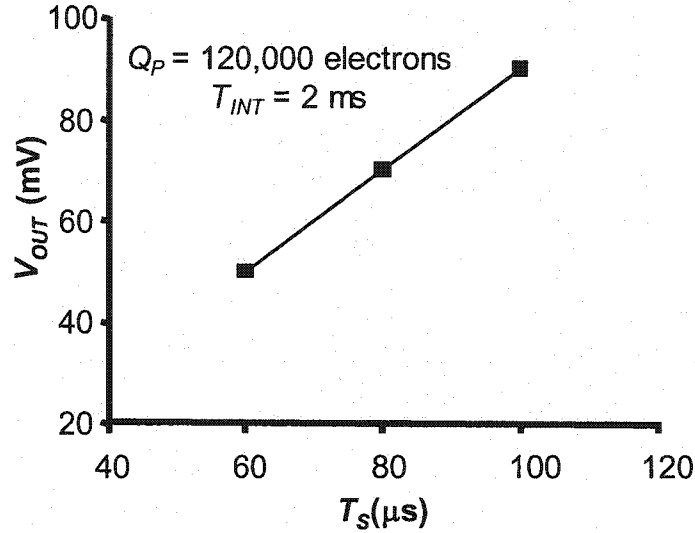


Figure 89. Dependence of array output voltage, V_{OUT} on the sampling time, T_S . Here, data from the column 2, row B pixel on Test Chip #5 is plotted.

It is interesting to note that although each pixel suffers a dark current, $I_{dark} = 83$ pA, the C-APS array is able to function normally (as shown in Figure 87) without the x-ray signal current (I_{signal}) being corrupted by the I_{dark} . An I_{dark} of 83 pA over an integration period of 2 ms will collect 1.04 million dark current electrons on C_{PIX} (around 55 mV of V_{dark}) while the minimum number of signal electrons in Figure 87 was only about 0.12 million.

Here, although $I_{signal} \ll I_{dark}$, the *negative mode* a-Se sensor (since the top contact bias is negative) causes both, I_{signal} and I_{dark} to decrease the bias voltage at the integration node. Since the voltage drop due to I_{signal} and I_{dark} (in mV) is much smaller than the bias voltage (~ 10 V) at the AMP TFT gate, the net effect of I_{signal} and I_{dark} is to simply negatively shift the bias point of the AMP TFT by a few mV. Since I_{dark} is constant from measurement to measurement (because the integration time, T_{INT} remains constant), it becomes part of an offset in the V_{OUT} measurements.

6.3.6 Noise

Noise performance of the a-Se C-APS imager was measured via a digital oscilloscope operating in the phosphor mode. The noise variance was extracted from the noise voltage on the screen after a large number of samples were measured. The noise was taken to be Gaussian in nature (assuming thermal and shot uncorrelated noise sources dominate flicker). Then, the measured noise value was fit to a normal distribution to extract the standard deviation and the noise variance. Noise variance techniques to extract the output rms noise voltage have been successfully used in the past to evaluate the noise performance of CMOS APS imagers [138].

6.3.6.1 Noise with charge integrator reset switch closed

The noise from the charge integrator, S/H circuitry, and differential amplifier was measured by putting the charge integrator into reset mode (C_RST was kept ON all the time). Here, the C-APS pixel was decoupled from the external readout circuitry to remove any effect the pixel circuit may have on the output noise reading. Since the charge integrator output was read out every 2 ms, waiting for five minutes yielded over 100,000 samples on the digital oscilloscope. Assuming Gaussian statistics and that the sample size is large enough to account for 6σ (or 99.7% of values around the mean) of the readings, the standard deviation (σ) was extracted and used to establish the output noise variance (σ^2).

For example, the 6σ value was measured as 9 mV for the external electronics (here, the charge integrator is the primary contributor of noise since it is the first device in the external readout electronics chain), which yielded a variance, $\sigma_{out}^2 = 2.25 \mu V^2$ at the AD626 output. Since double sampling is involved, the measured noise variance was halved and referred back to the charge integrator output. Here, the gain of 5 from the output AD626 amplifier has to be accounted for yielding a noise variance of 45 nV^2 on the charge integrator's feedback capacitor, C_{FB} . The integrator's output noise variance is then converted into an rms noise voltage value of $211 \mu V$, which is about twice of the rms noise value reported for an IVC102 integrator with a $C_{FB} = 10 \text{ pF}$ in the Burr-Brown data sheet. Evidently, there is additional noise due to the S/H circuits, the differential amplifier and perhaps, even the test board. The rms noise at the integrator output is converted into equivalent electrons by using

the C_{FB} value of 10 pF to give 13250 rms noise electrons. The charge integrator's equivalent noise electron value with double sampling (18750 electrons) is used for subsequent C-APS noise performance calculations.

6.3.6.2 Noise from the C-APS Readout Circuit

In order to account only for the noise from the APS readout circuit, the C-APS noise performance is measured without including the effect of the RESET TFT. Thus, the RESET TFT is not pulsed but rather DC biased to 16 V for the duration of the measurement. DC biasing the RESET TFT eliminates reset noise at the APS integration node. Any remaining fluctuations in the integration node voltage are due to the shot noise of the a-Se photoconductor dark current. I_{dark} was extracted to be around 83 pA/pixel at an a-Se bias of -36 V and thus, the shot noise due to the a-Se dark current can be estimated as [136],

$$q_{dark} = \sqrt{\frac{J_{dark} A_P F_P T_{INT}}{q_e}} \quad (5)$$

where J_{dark} is the a-Se dark current density, q_e is the usual electron charge, A_P and F_P define the pixel area and geometrical fill factor respectively and T_{INT} is the time the dark current is integrated at the gate of the AMP TFT (2 ms for the experiment). Using eqn. (5) for the fabricated C-APS 500 x 500 μm pixels (with a fill factor of 40%) yields 1000 noise electrons at the integration node due to the dark current. With double sampling and a charge gain of 10.5, the dark current shot noise electrons are expected to be significant (around 15100 electrons at the integrator output) compared to other noise sources in the circuit. Table 20 below highlights the C-APS noise performance with double sampling at the charge integrator output where the RESET TFT is dc biased in the ON state.

Table 20. Noise performance of a-Se C-APS array without reset noise

$$V_{Se} = -36 \text{ V}, C_{FB} = 10 \text{ pF}, V_{DD} = 12 \text{ V}, V_{RST} = +16 \text{ V}, V_{RD} = +16/0 \text{ V}, G_i = 10.5$$

Noise sources (with double sampling)	Output Noise on C_{FB} (electrons)
Thermal (AMP, READ TFT)	1840
Flicker (AMP, READ TFT)	6400
Shot Noise	15100
Reset (RESET TFT)	0
Measured charge amplifier noise	18750
Output noise	24990
Measured output noise without reset contribution	24580 ($\sigma_{out}^2 = 3.87 \mu V^2$)
Error	< 2 %

6.3.6.3 C-APS noise performance

The complete noise performance of the C-APS circuit is shown in Table 21 below where both the READ and RESET TFT gates are pulsed with +16/0 V biases. Note the large value of reset noise that is mainly due to the in-house developed APS pixel capacitance (C_{PIX}) of 3.03 pF. Based on the C_{PIX} value and the reset noise theory presented in Chapter 5, the reset noise was calculated and is shown in the table below. The noise measurements on the a-Se C-APS imager appear to be in good agreement with the theory presented in Chapter 5. If $G_i = 10.5$ is used, the total input referred noise at the APS integration node is estimated from the total measured output noise to be 2650 electrons.

For the particular C-APS imager fabricated and tested in this experiment, the charge amplifier noise is the major limiting factor followed closely by reset and shot noise. These noise sources can be reduced respectively by incorporating a high performance, low noise, charge integrator into the external readout circuitry, using high quality a-Se with low dark current contacts, and an appropriate choice of C_{PIX} . If the preceding steps to noise reduction are taken, then the flicker noise becomes significant and is mostly due to the AMP TFT operating in saturation. Increasing the AMP TFT size and lowering the supply voltage as discussed in Chapter 5 can reduce flicker noise.

Table 21. Noise performance of a-Se C-APS imager with double sampling

$$V_{Se} = -36 \text{ V}, C_{FB} = 10 \text{ pF}, V_{DD} = +12 \text{ V}, V_{RST} = V_{RD} = +16/0 \text{ V}, G_i = 10.5$$

Noise sources (with double sampling)	Output Noise on C_{FB} (electrons)
Measured noise without reset	24580
Reset noise	11400
Output noise	27110
Measured output noise with reset noise contribution	27900 ($\sigma_{out}^2 = 4.99 \mu\text{V}^2$)
Error	< 3%
<i>Total Input Referred Noise</i>	2650

6.4 Future considerations

A larger charge gain is possible by further reducing C_{PIX} where a reduction in C_{PIX} is possible if the RESET TFT parasitic overlap capacitances and hence, charge injection effects are minimized as described in Chapter 2. Eliminating the storage capacitor can also reduce C_{PIX} . Typically, in diagnostic medical imaging applications, the sensor thickness is at least 10 times that used in the a-Se C-APS imager described in this chapter. Hence, the sensor capacitance would be reduced to fF in a typical application. A lower limit on C_{PIX} arises from the point of view of lower noise performance where the saturated AMP TFT must be kept large enough to minimize its flicker noise contribution. However, experiments and simulations in Chapter 5 show that fluoroscopy level noise performance is achievable with current a-Si technology.

Higher gains are possible by either increasing the TFT size or the supply voltage, V_{DD} to increase the C-APS transconductance (g_m). The current pixel size of $500 \times 500 \mu\text{m}^2$ can be reduced to $250 \times 250 \mu\text{m}^2$ using the vertically stacked pixel process architecture described in Chapter 3. Also, scaling the current TFT process to $L = 6 \mu\text{m}$ industry standard allows smaller TFTs to be fabricated. However, an upper limit to the g_m exists due to C-APS output current saturating the charge amplifier. Here, by designing a custom, low-noise, charge amplifier with a reliable, fixed value, current sink, it may be possible to achieve higher charge gains.

In addition, typical fluoroscopic arrays are expected to have a pixel count of 1000 x 1000. Here, for real-time readout at 30 Hz, a readout time of 33 ms per frame is allowed. However, if charge amplifiers are placed at both ends of the column and operated simultaneously, a readout time of 66 ms per frame can be obtained. Since the charge gain is directly proportional to sampling time, doubling the sampling time doubles G_i .

From the perspective of reset noise, some improvements may also be possible if correlated double sampling is performed off-panel in software. Currently, a reset sample of the C-APS output is taken directly after the signal sample as shown in Figure 80. Here, since the pixel is reset twice (once for each sample), the reset noise variances of the two samples are uncorrelated and thus, add in quadrature increasing the total reset noise rms value. Hence, the technique is more aptly termed double sampling since correlation between samples is not present. In contrast, if the reset sample value was obtained first and stored off-panel in software and the signal sample is taken after the x-ray integration period (i.e. just *one* reset has occurred), it may be possible to reduce the reset noise since the reset noise variances of the two samples are correlated. The above scheme of changing the order in which the signal and reset sample are subtracted requires some form of off-panel frame memory and thus, lower pixel noise performance can be obtained for an increase in the complexity of off-panel readout mechanism.

Chapter 7. Conclusions and Contributions

In this thesis we have developed new pixel readout circuit architectures, fabrication techniques, innovated device designs and developed ΔV_T and noise models for a-Si TFTs. New pixel readout circuit architectures (with particular attention to the C-APS), investigated in Chapter 2, provide on-pixel gain for improving noise performance and can interface to on-panel multiplexers allowing for highly integrated large area imagers. The innovations to the current a-Si TFT process in Chapter 3 improve array reliability and allow for reduced inter-level parasitic capacitances due to the additional a-SiN layer. The TFT process innovations are particularly important for successful integration with a direct x-ray detection scheme employing an a-Se photoconductor. The development of a fully overlapped pixel architecture allows for vertical stacking of the sensor and readout TFTs. The low-k dielectric investigated reduces parasitic capacitance that can arise due to the vertical integration. The progress made in vertically integrating the sensor and TFTs is particularly valuable for fill-factor sensitive applications such as mammography. Pulse and dc bias dependent ΔV_T for a-Si TFTs operating as both switches and active devices was explored in Chapter 4 where models were developed to predict the ΔV_T and hence, gain variations in an a-Si amplified pixel (C-APS) readout circuit for large area, digital medical imaging applications. The developed ΔV_T models can easily be applied to emerging low voltage a-Si technology applications where TFTs are used as both, switches and active devices (e.g. OLED displays). Chapter 5 examined the fundamentals of low frequency noise in a-Si TFTs operating in both linear and saturation regions. In addition, reset noise, commonly the limiting noise source in CMOS imaging pixels, was investigated for a-Si TFT based pixels. The noise performance of the new pixel readout circuit architecture (C-APS) determined its feasibility for low noise

digital fluoroscopy. Lastly, Chapter 6 described the integration and measurement results of an a-Si TFT based amplified pixel (C-APS) array with a direct x-ray detection a-Se photoconductor. The original contributions of the research presented in this thesis to the area of a-Si technology are summarized below.

Circuit Design

- The first a-Si TFT based pixels and arrays with on-pixel amplifiers were invented, fabricated and tested successfully.
- Unlike commonly used a-Si PPS readout circuits, the voltage mediated APS (V-APS) architecture is amenable to having its output multiplexed for highly integrated large area imaging arrays but its readout time makes it suitable for static imaging applications.
- The current mediated APS (C-APS) readout circuit architecture is a unique circuit that provides on-pixel *gain*, real-time readout and can have multiplexed outputs for highly integrated large area imaging arrays. The gain is programmable by varying the supply voltage or sampling time.

Device and Process development

- The first successful a-Si TFT switch based fully overlapped pixel architecture process was developed as a precursor to vertical integration of the sensor and readout circuit TFTs. Devices in the fully overlapped architecture, based on dual-gate a-Si TFTs, maintained low (pA) values for leakage currents even in the presence of a +10 V bias on the overlapping sensor back electrode.
- The first low-k organic dielectric for integration with a-Si imaging and/or display pixels was developed where k values of < 3 were obtained. The dielectric forms the spacer between the sensor and a-Si TFT readout circuit to reduce inter-level parasitic capacitances.
- The existing five mask in-house a-Si TFT process was updated and implemented as a reliable seven mask TFT array process that reduced parasitic capacitances between drain/source and gate metallizations. The fabricated TFTs could withstand terminal voltages of 100 V without breaking down.

TFT ΔV_T and Circuit Metastability

- The ΔV_T relationship for an a-Si TFT used as a passive (i.e. operating as a switch) or active device (i.e. operating in the saturation region) as a function of bias voltage and time was modeled based on measurements. Here, the effect of both positive and negative voltages at the gate terminal for a range of drain/source biases is examined.
- The relationship of ΔV_T to pulsed gate bias voltages as a function of bias voltage (positive and negative) and time was measured and modeled.
- A low voltage (< 30 V) ΔV_T model is developed that accounts for both positive and negative, dc and pulse bias stresses on a-Si TFTs operating in linear or saturation mode.
- ΔV_T performance for the C-APS pixel readout circuit was measured for the first time and found to be in good agreement with the ΔV_T model. The ΔV_T model was then extended to predict the gain variation (found to be less than 5%) in the C-APS pixel over an imager lifetime of 10,000 hours.

TFT and Circuit Noise

- Low frequency noise (thermal and flicker) was measured for in-house a-Si TFTs where the flicker noise was found to follow the Hooge theory of mobility fluctuation.
- Reset noise using an a-Si TFT switch was measured for the first time. Measurements and modeling indicates that the reset noise is about 20% higher than its classical kT/C value for low duty cycle ($< 1\%$) large area, medical imaging applications.
- Noise performance for the C-APS pixel readout circuit was measured for the first time and found to be in good agreement with the developed noise theory. Reset noise was found to be the major component and could be minimized by choosing a smaller pixel capacitance. The circuit noise results were then extended to a state-of-the-art TFT process that indicated digital fluoroscopy is feasible using a-Si TFT C-APS pixels.

Device and Array Integration

- The first a-Si TFT C-APS array integrated with an a-Se photoconductor for X-ray imaging was designed and fabricated and its gain, linearity and noise performance was tested.

Appendix A – Amorphous Silicon TFT

A.1 Amorphous Silicon TFT Technology

The proliferation of a-Si TFTs in the field of large area electronics requires CAD oriented device models to facilitate design of circuits. There are a multitude of a-Si TFT models available in current literature [8][9][10]. Some aim to provide compatibility with existing circuit simulators such as SPICE [10] while others are more physically oriented and attempt to provide analytical predictions of device operation [9].

The operation of a-Si TFTs is primarily affected by the density of localized trap states in the a-Si film as well as by the staggered nature of the TFT structure (see Figure 90).

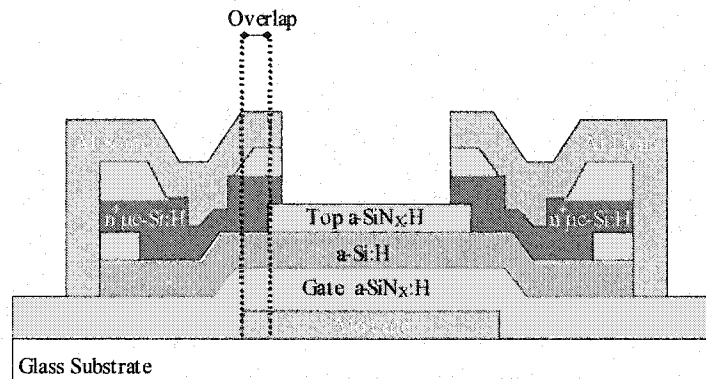


Figure 90. Inverted staggered a-Si TFT

Hence, most analytical TFT models begin by examining the effect of the trap states on device behavior [8][11]. Like MOSFETs, the inverted channel is located at the gate insulator/semiconductor interface. However, the TFT is a three terminal device where the bulk a-Si semiconductor remains floating which introduces additional complexity in the model. Here, the channel properties are determined by the thickness of the various films, material properties and applied gate voltage.

Unlike the MOSFET, the source and drain contacts in a-Si TFTs are situated on opposite sides of the a-Si film and are separated from the gate by an intrinsic semiconductor layer.

This effectively makes the TFT contact behavior significantly different from MOSFETs where the source and drain contacts are modeled via simple parasitic resistances. There are detailed analyses [9][12], which model the effect of contacts on TFT operation.

The main purpose of this appendix is to review the fundamental properties and characteristics of amorphous silicon pertinent to TFT operation. The performance of imaging pixel architectures discussed in this work depends primarily on the forward current (I_D) characteristics of the TFT. Hence, some of the common physical methods of modeling a-Si TFT forward drain current are described in this section. One of the physical TFT models, also forming the foundation for in-house TFT model development at the University of Waterloo, will be discussed in detail to give an insight into TFT behavior. Then, a VHDL-AMS model implementation of the in-house TFT model will be briefly presented and since the circuit analysis in later sections depends on various TFT parameters, extraction procedures for the various TFT parameters are presented.

A.2 Amorphous silicon density of states (DOS)

Unlike crystalline silicon where atoms are distributed periodically in space, the amorphous state is characterized by positional disorder [14]. Although long-range order is lost in amorphous materials, some short-range order is preserved. Subsequently, the DOS concept, $g(E)$, needs to be revisited for amorphous materials [14]. The DOS function for amorphous silicon, in general, is complex and displays a distinct dependence on the material preparation conditions [15]. Hence, the exact DOS is determined through experimental techniques.

The random atomic lattice structure of amorphous materials requires the introduction of new concepts to the energy band theory different from the standard theory for crystalline materials. However, although long-range disorder is present in amorphous silicon, the shape of the density of states is strongly determined by local bonding configurations [16]. Thus, the energy band model of crystalline silicon is applicable to amorphous silicon with few modifications [17] as shown in Figure 91.

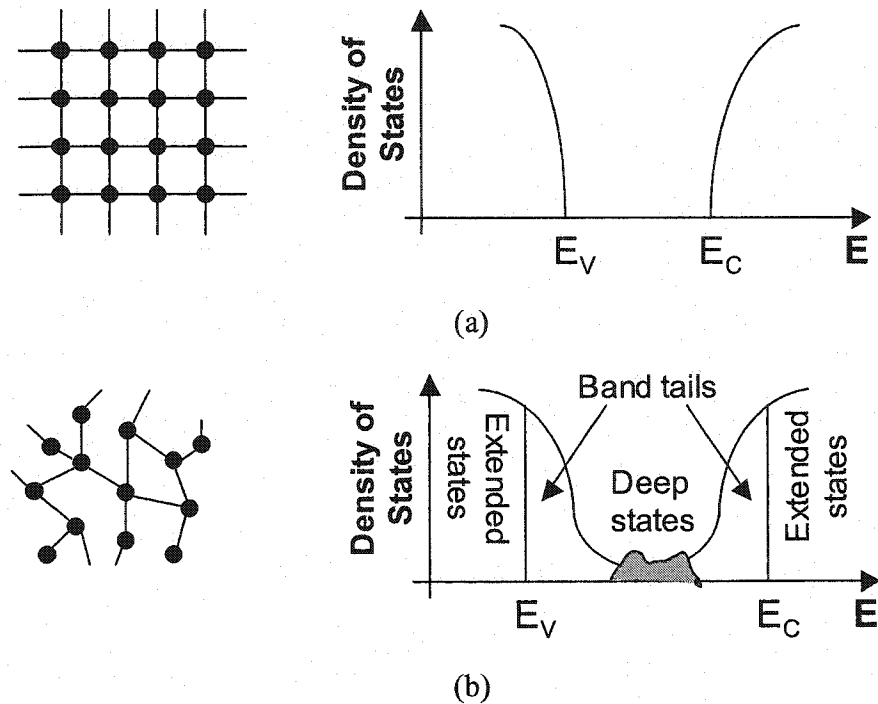


Figure 91. Atomic structure and band model for (a) c-Si and (b) a-Si [4]

Amorphous semiconductors display both conduction and valence bands. The energy band diagram of amorphous silicon consists of two types of states, extended and localized. Carriers in the extended states are not spatially confined and are therefore able to contribute to current conduction. Localized states, also commonly known as tail states, result from the loss of long-range order in the amorphous material. Carriers occupying these states are spatially confined or trapped [14]. The density and distribution of tail states are a function of the amount of disorder in the amorphous silicon film. The trapping behavior of these tail states depends on whether they are associated with the conduction or valence bands. The conduction band tail states are “acceptor-like” in that they are negatively charged when occupied by an electron and neutral when empty. The valence band tail states (“donor-like”) are positively charged when empty and neutral when occupied by a hole. In addition to localized tail states, amorphous silicon also has trap states that are due to dangling bonds and other lattice defects [18]. These traps are commonly known deep localized states or deep states.

It is valuable to note that the localized states (tail and deep) allow carriers to occupy any energy level between E_C and E_V , the conduction and valence band energies. Here, the conventional forbidden gap concept of c-Si is replaced with a mobility gap concept. The

mobility gap is the point in the DOS where the carrier mobility goes from a small value to a large value. Basically, carriers in the localized states can move between states via phonon assisted hopping but the mobility here is very low [14]. On the other hand, carriers in the extended states ($E > E_C$, $E < E_V$), are mobile and free to conduct current taking on values of the band mobility. So to summarize, carriers may occupy energy states within this mobility gap but will not contribute to current conduction unless they are in the extended states.

A.3 Mobility gap models

One of the differences in the a-Si TFT models of various researchers lies in the manner the DOS is represented. The exact distribution of localized states in the mobility gap is controversial. Powell (see Figure 92) of Philips Research Laboratories [11] proposed a linear distribution of the conduction band tail states for about 0.15 eV below E_C . It is followed by a steep exponential distribution with a characteristic temperature, T_C , of 200 K. The deep states take the form of a slow varying exponential or a uniform distribution. The DOS near E_C is expressed as:

$$g(E) = G_{tail} + A_{tail}(E - E_{tail}) \quad \text{for } E > E_{tail} \quad (1)$$

$$g(E) = G_{tail} \exp((E - E_{tail})/kT_{tail}) + G_{deep} \exp((E - E_C)/kT_{deep}) \quad \text{for } E < E_{tail} \quad (2)$$

where T_{tail} and T_{deep} are the characteristic temperatures of the exponentially distributed tail and deep states, respectively. E_{tail} is the energy at which the distribution of tail states changes from a linear to an exponential distribution and G_{tail} ($\text{eV}^{-1}\text{cm}^{-3}$) is the density of localized states at $E = E_{tail}$. The parameters A_{tail} , E_{tail} , G_{tail} , G_{deep} , T_{tail} and T_{deep} are determined by experimentally evaluating $g(E)$.

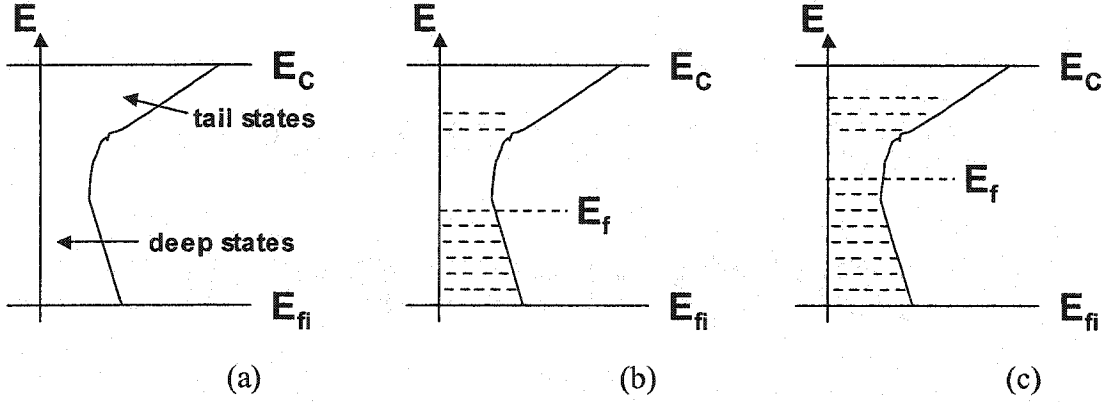


Figure 92. Density of states using the Powell model [11] [20]

(a) Device in equilibrium ($V_{GS} = 0$). The Fermi level is at the intrinsic Fermi level position,

$$E_{fi}.$$

(b) Device in subthreshold ($V_{GS} < V_T$). Deep states trapping control the device behavior.

Few electrons are trapped by the tail states.

(c) Device is in above threshold mode ($V_{GS} > V_T$). The Fermi level is pinned by the tail states.

In comparison to the Powell model, the Shur model [8] assumes that both tail and deep states follow an exponential distribution (see Figure 93) and hence the DOS for the upper portion of the mobility gap is:

$$g(E) = g_D \exp((E - E_C)/kT_{deep}) + g_T \exp((E - E_C)/kT_{tail}) \quad (3)$$

where T_{tail} and T_{deep} are the characteristic temperatures of the tail and deep states, respectively, and g_T and g_D are the respective density of tail and deep states ($\text{eV}^{-1}\text{cm}^{-3}$) at the edge of the conduction band ($E = E_C$). Typical values of T_{tail} and T_{deep} are 300K and 1000K respectively. The high characteristic temperature of the deep defect states results in a slow varying density of states distribution for deep states, which is in agreement with Powell's model. The above equation has been widely used for analytical modeling of TFTs including several CAD TFT models [8][20][21][22]. Later on, Kuo [23] proposed an effective temperature approach that approximates the dual exponentials in the Shur model to a single

exponential which simplifies the analysis considerably by removing the need for numerical methods.

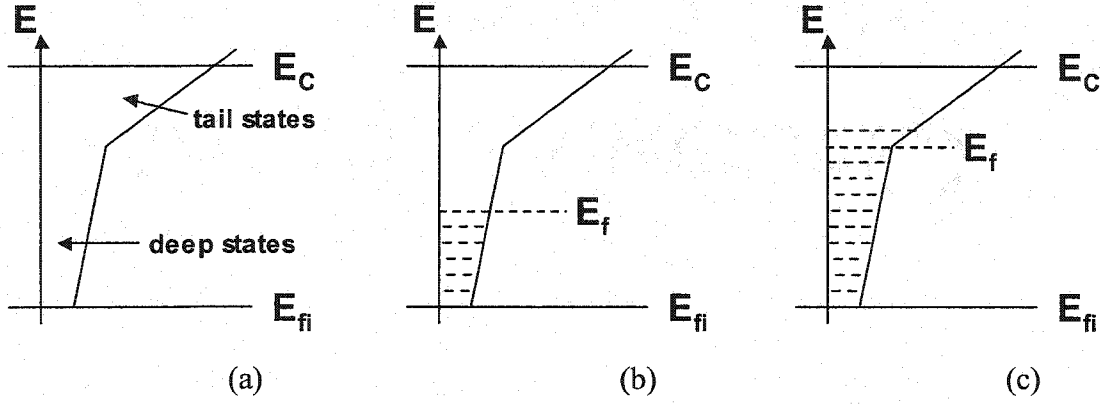


Figure 93. Density of states using the Shur model [20] [24]

(a) Device in equilibrium ($V_{GS} = 0$). The Fermi level is at the intrinsic Fermi-level position, E_{fi} .

(b) Device in subthreshold region ($V_{GS} < V_T$). Deep states trapping control the device behavior.

(c) Device at the threshold voltage ($V_{GS} > V_T$). The Fermi-level is at the intersection point of deep and tail states.

In order to develop an analytical understanding of the TFT device physics, a DOS used by Leroux [21] and proposed in [26] which consists of a single exponential for each band tail (neglecting deep states) will be used in this section. This model, too, is widely used in literature [25][26].

$$N^-(E) = (N_{tc}/kT_c) \exp((E - E_C)/kT_c) \quad (4)$$

$$N^+(E) = (N_{tv}/kT_v) \exp((E_V - E)/kT_v) \quad (5)$$

It is also of interest to note that the analysis developed by Leroux [21], combined with the effective temperature approach of Kuo [23] formed the basis for the in-house University of

Waterloo TFT forward current model [46]. A VHDL-AMS implementation of the in-house model by the author [47] was undertaken in order to facilitate design (via simulation) of a-Si TFT circuits for imaging pixels. Details of the implementation are explained in a later section.

A.4 Amorphous Silicon thin film transistor (TFT)

A.4.1 TFT Device Structure

a-Si TFTs were suggested in 1962 [27] and first demonstrated in 1981 by Spear and LeComber [1][28][29]. Unlike crystalline transistors that are fabricated into a substrate, TFTs are deposited onto a substrate [27]. Modern a-Si TFTs are usually fabricated on inexpensive glass substrates [30]. In contrast to co-planar MOS devices, practical a-Si TFT structures are of the inverted staggered type with the gate metal at the bottom and source/drain contacts at the top of the a-Si film. This structure is the most commonly used TFT structure with a-Si technology because of the relatively low interface state density between the amorphous silicon nitride, a-SiN_x:H, dielectric and a-Si layers as well as its relatively simple fabrication process [11]. This structure has been investigated since the first a-Si TFT was demonstrated and is shown in Figure 90. To deposit the gate insulator (the quality of which determines I-V characteristics, V_T , subthreshold slope), a three-step PECVD process depositing the gate insulator, a-Si active film, and top insulator is used ensuring the gate insulator is never exposed to the environment. The high quality of the gate insulator ensures low surface state trap density at the interface, which is one method to reduce the threshold voltage.

A.4.2 Summary of Device Operation

The difference between the energy band structures of a-Si and c-Si causes significant differences in device operation. In MOSFETs, the charge induced in the semiconductor by the applied gate voltage is primarily made up of free carriers. In the a-Si TFTs, the defective

amorphous silicon traps most of the induced charge in the localized states (tail and deep). The induced free carriers are rarely larger than 10% of the total gate induced charge [8]. In addition, the mobility of the extended states is also quite small due to amorphous nature of the material, which causes an additional decrease in the driving ability of the TFTs.

The TFT characteristics are dependent on the localized DOS and different DOS models in literature predict differing device characteristics. Assuming flat bands, when the gate voltage is increased, band bending occurs at the silicon-insulator interface. Unlike MOS where a depletion layer and then an inversion layer is created in the p-type substrate for an NMOS device, the band bending causes an accumulation of electrons near the surface in TFTs. Some of these electrons are in the conduction band but most of them are in the mid-gap localized acceptor states i.e. deep states. The band bending causes the Fermi level at the gate insulator-semiconductor interface to cycle through the deep states initially making its way up to the tail states. The region dominated by the behavior of the deep states is commonly known as the subthreshold region and here, source-drain current increases exponentially with applied gate bias [8] [11] [21].

As the electron Fermi level rises towards the conduction band, a majority of the gate-induced electrons become trapped in the tail states rather than the deep states give rise to an above threshold region. The drain source current becoming a power law function of the gate voltage accompanies entry of the Fermi level into the tail states. The Powell model defines the TFT threshold voltage as the point where the Fermi level becomes “pinned” in the trap states. As the gate voltage increases, the number of electrons in the tail states increases. Owing to the DOS proposed by Powell and noting that the density of deep states is quite large, the Fermi level need not be located within the tail states to be pinned (see Figure 92). For both Shur and Leroux, since an exponential distribution of tail states is assumed, the tail states are less effective in pinning the Fermi level as shown in Figure 93. Increasing the gate voltage can drive the Fermi level into the tail states and possibly reach the conduction band, E_C although the latter is highly unlikely since such a large gate voltage would cause device breakdown before reaching the conduction band [21].

A.4.3 Introduction to a-Si TFT static forward current analysis

The active region of the TFT (i.e. the a-Si film) in Figure 90 is usually between 30 – 150 nm in thickness. The a-Si film is deposited on a glass substrate and contains defect states that are distributed uniformly through the material. The Fermi level in undoped amorphous silicon is slightly above midgap [4] making the intrinsic material inherently n-type but it can be assumed to be at midgap for simplicity in the initial analysis. The trap states, characterized by their spatial and energy distribution $N_T(x,E)$ in states/(eV.cm³), are also assumed to have a uniform distribution (i.e. N_T is constant in both energy and position) for simplicity. A consequence of a high trap density is an increase in the threshold voltage, i.e. a large portion of the gate voltage is used to induce electrons that fill up the empty trap states. For sufficiently high gate voltages, the traps become filled and the mobile carrier concentration increases.

Doping the a-Si layer does not have any major effect in a-Si TFTs mainly because the extra free carriers provided by the dopant go into the additional traps created by the dopant in the amorphous silicon film [4] leading to a very poor doping efficiency. Practical a-Si TFT structures use an intrinsic film for the conducting channel partly for this reason but more because an intrinsic a-Si film can provide extremely low leakage current (even sub-fA) [4] which is essential for low input imaging applications.

A.5 TFT operation

Considering an a-Si active film with a non-zero density of trap states, N_T (cm⁻³eV⁻¹), the Fermi level is assumed to be around mid-gap for simplicity. In addition, it was reported [31] that the trap states tend to be neutral when the Fermi level is near midgap. Further, the donor-like trap states below the mid-gap are assumed filled while the acceptor-like trap states above mid-gap are empty making the material charge neutral. Figure 94 illustrates the band diagram of a TFT MIS capacitor under different gate biases.

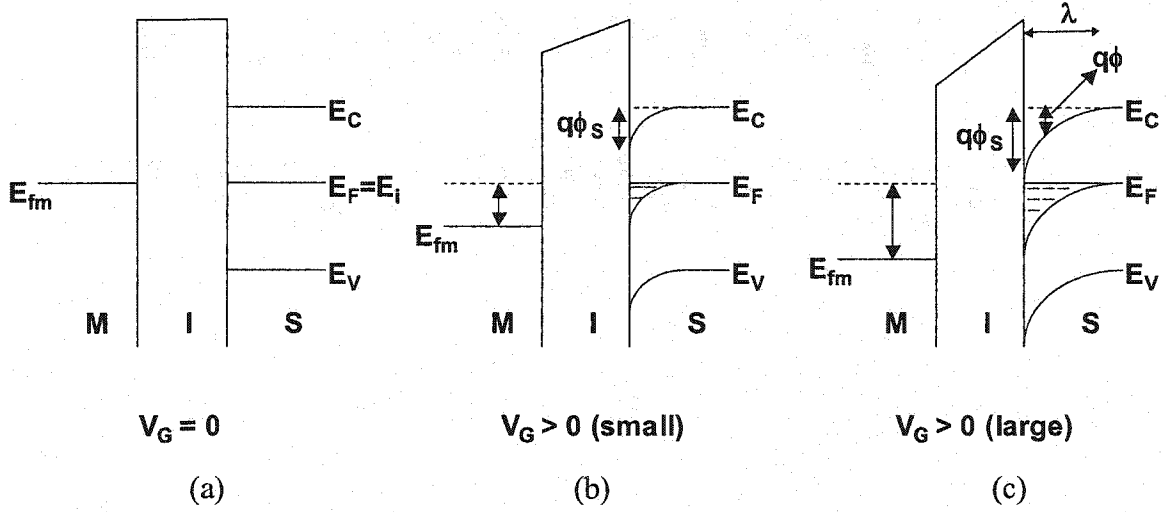


Figure 94. Band diagram for MIS device

Again, assuming flat band at zero gate bias for simplicity, note that the metal Fermi level, E_{fm} moves down with increasing positive gate bias. Since there is no current through the insulator, the bands in the semiconductor bend with applied gate bias. Application of a small positive voltage causes the bands to begin bending at the surface and consequently, some of trap states above E_F , the semiconductor Fermi level, fill with electrons. The states above the Fermi level are acceptor-like traps, and as they fill, the negative charges in these states balances the positive charge on the gate. For small gate voltages, E_C is not very close to E_F after the bending and as a result, the number of electrons in the conduction band is small. For large gate biases, E_F approaches E_C and a significant number of electrons are found in the conduction band.

As illustrated in Figure 94 (c), the distance the bands bend into the semiconductor is described as a “screening length”, λ . λ represents the a-Si semiconductor depth that contains most of the trapped charge and is a screening length over which the bands bend to screen an applied surface field from the bulk of the semiconductor. The screening prevents any further band bending in the semiconductor. The screening length for a semiconductor can be calculated by starting with Poisson’s equation:

$$\frac{d^2\phi}{dx^2} = -\frac{\rho(y)}{\epsilon_s} \quad \text{where} \quad \rho(y) = qp(y) - qn(y) + \rho_T(y) \quad (6)$$

Here,

$$\rho(y) = qn_i \exp[(E_i(y) - E_F)/kT] - qn_i \exp[(E_F - E_i(y))/kT] - qN_T[E_F - E_i(y)] \quad (7)$$

where p_T [coul/cm³] is the trapped charge density and N_T (in cm⁻³eV⁻¹) is constant. Below threshold, the electron and hole charge can be neglected [31] and since $q\phi(y) = E_F - E_i(y)$, Gauss' law then becomes:

$$\frac{d^2\phi}{dx^2} = q^2 \frac{N_T\phi(y)}{\epsilon_s}, \quad (8)$$

which can be solved if a solution of the form $\phi(y) = \phi_s \cdot \exp(-y/\lambda)$, is assumed where ϕ_s is the surface band bending. $\phi'(y)$ and $\phi''(y)$ can then be derived and compared to eqn. (8) to extract,

$$\lambda = \left(\frac{\epsilon_s}{q^2 N_T} \right)^{1/2} \text{ cm}. \quad (9)$$

The screening length is an important parameter in TFT design. To make TFTs where the mobile electron concentration is easily modulated, the number of trap states that need to be filled for conduction to happen have to be reduced in number. The only way this can be done is to reduce the thickness of the a-Si film, i.e. thin film transistors. Figure 95 shows the result when different gate biases are applied to a semiconductor with a thickness less than the screening length.

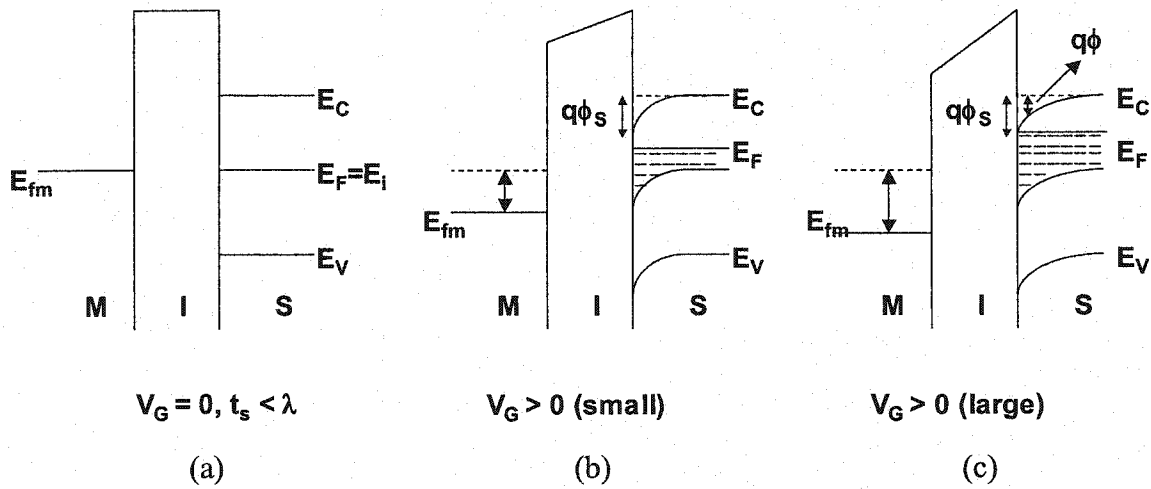


Figure 95. MIS device band diagram for thin films

Since the a-Si layer is thin, both band bending and an upward shift in the Fermi level occur in order to compensate increasing gate charge with increasing gate voltage. Initially, for a small gate voltage, the bands are flat at the back surface of the semiconductor. This is a consequence of the gate charge being balanced by the charge in the a-Si film (the net charge on the Gaussian surface from the metal to the back of the a-Si film is zero). Since the electric field in the metal is zero, so must the electric field at the bottom surface of the a-Si film be zero also. Increasing the gate voltage further, brings the Fermi level close to the conduction band causing a large increase in the free carriers and hence the TFT can be thought of as turning on.

Since both the bands bend and the Fermi level moves up, less gate charge is required to fill the traps in a thin a-Si layer before the number of electrons in the conduction band become appreciable. Therefore, it would be expected that using a thin layer for an a-Si film would lower the threshold voltage for a TFT. In addition, if the number of traps in the a-Si film is decreased, the threshold voltage would be further reduced. As a note, a highly defective material also serves to reduce the carrier mobility since there is increased scattering due to the defects [31].

A.6 Simplified I_{DS} calculation

Assuming a thin a-Si layer, an analysis similar to the MOS transistor Level 1 model [31] can be performed for a-Si TFT drain current where all drain current calculations are with reference to Figure 96 [32] below where V_d , V_s and V_g are voltages associated with the drain, source and gate terminals.

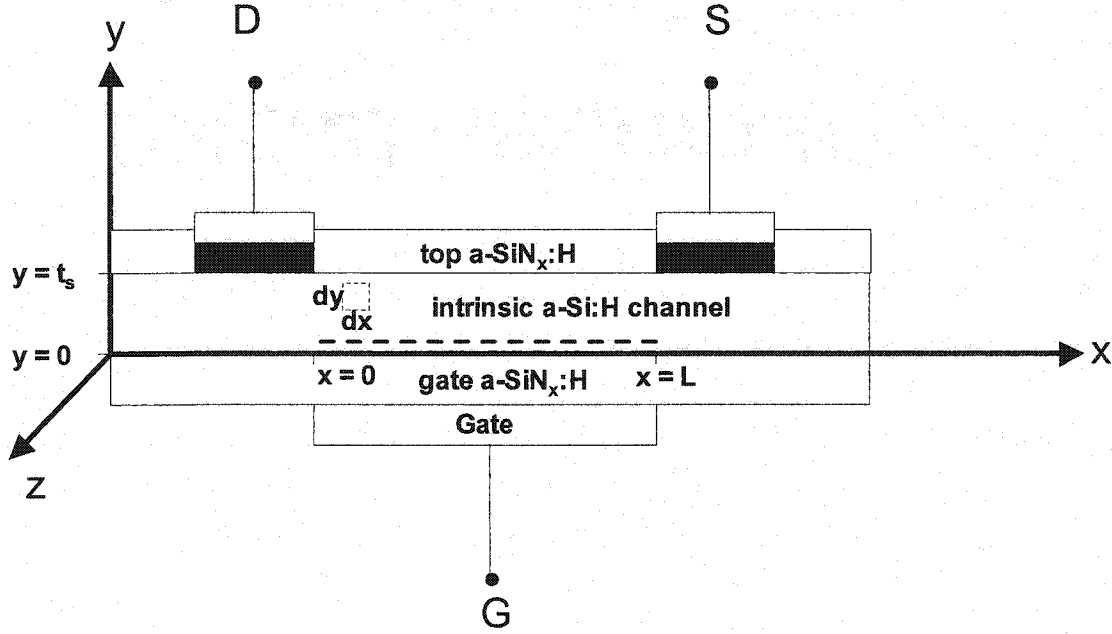


Figure 96. TFT reference points for drain current calculation

Assuming flat band conditions and noting that the trapped and free carrier charge in the a-Si layer must balance the charge due to the gate voltage on the metal,

$$Q_G = -Q_n - Q_T, \quad (10)$$

where Q_G is the charge on the gate metal, Q_n is the free charge in the conduction band and Q_T is the trapped charge in the acceptor states. For small gate voltages, Q_n is small and an increase in Q_G is seen by a corresponding increase in the trapped charge, Q_T . Assuming the a-Si film is very thin and much thinner than the screening length, λ , Q_T and Q_n can be approximated as,

$$Q_T \approx -qN_T t_s [E_F - E_i(y)], \quad (11)$$

$$Q_n \approx -qn_i t_s \exp[(E_F - E_i(y))/kT], \quad (12)$$

where t_s is the thickness of the a-Si semiconductor. Here the band bending is neglected due to the thin semiconductor as shown in Figure 95 where $E_i(y) = E_i$ since E_i is approximated as a constant with increasing y values. Also, the Fermi level moves up into the conduction band

with increasing gate voltage. The threshold voltage is arbitrarily defined as the value of gate voltage that gives an $[E_F - E_i(y)]$ that corresponds to $Q_T = Q_n$. Since Q_n increases exponentially and Q_T increases linearly with $[E_F - E_i(y)]$, a further increase in $[E_F - E_i(y)]$ beyond $Q_T = Q_n$ would raise the value of Q_n above Q_T . The threshold value, $[E_F - E_i]_{threshold}$ can be obtained by solving the following equation for $Q_T = Q_n$,

$$-qn_i t_s \exp[(E_F - E_i(y))/kT] = -qN_T t_s [E_F - E_i(y)] \quad (13)$$

$$kT \ln\left[\frac{N_T}{n_i} (E_F - E_i)_{threshold}\right] = (E_F - E_i)_{threshold} \quad (14)$$

Assuming a value of $[E_F - E_i]_{threshold}$ is obtained for a particular trap density N_T , Q_G as a function of position along the channel, x , can now be obtained.

$$Q_G(x) = C_{OX}[V_G - V(x)], \quad (15)$$

where we know Q_G from eqn. (10). Substituting gives,

$$Q_n = -C_{OX}[V_G - V(x)] - Q_T. \quad (16)$$

For values of Q_n above the defined threshold, $[E_F - E_i(y)]_{threshold}$, Q_n can be written as,

$$Q_n = -C_{OX}(V_G - V(x)) + qN_T t_s [E_F - E_i]_{threshold} \quad (17)$$

$$Q_n = -C_{OX}\left[V_G - \frac{qN_T t_s [E_F - E_i]_{threshold}}{C_i} - V(x)\right] \quad (18)$$

$$Q_n = -C_{OX}(V_G - V_T - V(x)) \quad (19)$$

where V_T is threshold voltage defined as,

$$V_T = \left[\frac{qN_T t_s [E_F - E_i]_{threshold}}{C_{ox}} \right] \quad (20)$$

Since the expression for Q_n above is very similar to that of a MOSFET, the remainder of the analysis can proceed in a similar fashion. Referring to Figure 96, the current at a point x in a MOSFET channel can be expressed as (assuming only drift current),

$$I_D \cdot dx = \mu_n Z Q_n(x) dV_x \quad (21)$$

$$\int_0^L I_D \cdot dx = -\mu_n Z C_{ox} \int_{V_D}^0 (V_G - V_T - V(x)) dV_x \quad (22)$$

$$I_D = \frac{\mu_n Z C_{ox}}{L} \left[(V_G - V_T) V_D - \frac{1}{2} V_D^2 \right] \quad \text{for } V_D < V_G - V_T \quad (23)$$

$$I_D = \frac{\mu_n Z C_{ox}}{2L} (V_G - V_T)^2 \quad \text{for } V_D \geq V_G - V_T \quad (24)$$

In practice, there are non-idealities including the quality of the insulator-semiconductor interface and the insulator itself. The non-idealities manifest themselves as changes to the threshold voltage. For example, issues such as fixed oxide charge, metal-semiconductor work function differences, surface states, donor or acceptor channel doping will affect the overall value of the threshold voltage. These will be thoroughly accounted for in the next section.

However, the importance of the above result is that simple MOS like equations can be used to approximate TFT forward characteristic operation by extracting V_T and an effective mobility from device measurements. In fact, the majority of preliminary circuit analysis carried out in this work is based on the simplified equations above. Of course, simulations (used for precise design) are based on detailed, complete equations for greater accuracy as defined in the next section.

While the above analysis considers TFT performance for above threshold, the below threshold region must also be examined since TFT threshold voltages can be quite high (around 2 V usually). Below threshold, i.e. below $[E_F - E_i]_{threshold}$, most of the charge induced by the gate voltage is approximated as being trapped charge. Therefore,

$$Q_G \approx -Q_T = qN_T t_s [E_F - E_i(y)] \quad (25)$$

and since $Q_G = C_{ox} V_G$ (all the voltage drops across the insulator, no drop over the thin semiconductor layer and $E_i(y) = E_i$),

$$\frac{C_{ox} V_G}{qN_T t_s} = [E_F - E_i] \quad (26)$$

Thus, the electron concentration near the grounded TFT source node can be estimated as,

$$n = n_i \exp\left[\frac{E_F - E_i}{kT}\right] = n_i \exp\left[\frac{C_{ox} V_G}{qN_T t_s kT}\right] \quad (27)$$

In the subthreshold regime, the main source of current flow is diffusion, which can be given as,

$$I_D = qD_{eff} Z t_s \frac{dn}{dx} = q\mu_n \left(\frac{kT}{q}\right) Z t_s \frac{dn}{dx} \quad (28)$$

$$\int_0^L I_D dx = q\mu_n \left(\frac{kT}{q}\right) Z t_s \int_{n_D}^{n_S} dn \quad (29)$$

From eqn. (27), the carrier concentration at the drain end, n_D is seen to be much smaller than at the grounded source node, $n_S = n$ for V_D exceeding a few kT/q volts. i.e. if $(V_D - V_S) > 3kT/q$, then,

$$n_S = n_i \exp\left[\frac{C_{ox} V_{GS}}{qN_T t_s kT}\right] \gg n_D = n_i \exp\left[\frac{C_{ox} V_{GD}}{qN_T t_s kT}\right] \quad (30)$$

where $V_{GS} = V_G - V_S$ and $V_{GD} = V_G - V_D$. Hence, I_D can be obtained in the subthreshold regime as,

$$I_D = q\mu_n \left(\frac{kT}{q} \right) \frac{Z}{L} n_i \exp \left[\frac{C_{ox} V_G}{qN_T t_s kT} \right] \quad (31)$$

The corresponding subthreshold slope, S , can be extracted as, $1/S = (d \log(I_D)/dV_G)$ where,

$$\log I_D = \log_{10} \left[q\mu_n \left(\frac{kT}{q} \right) \frac{Z}{L} n_i \right] + \left[\frac{C_{ox} V_G}{qN_T t_s kT} \right] \log_{10} e \quad (32)$$

Therefore, $1/S$ is simply given by,

$$\frac{1}{S} = \left[\frac{C_{ox}}{qN_T t_s kT} \right] \log_{10} e \quad (33)$$

Since V_T and S are directly proportional to N_T , both the threshold voltage, V_T , and subthreshold slope, S , are degraded if the trap density, N_T , is high. Note that in the above analysis, the transistor width (W) was represented as the more convenient Z since the width runs along the z axis in Figure 96.

A.7 Detailed I_{DS} calculation

A.7.1 Comparison with the previous simplified model

The previous analysis makes a number of assumptions that render it incomplete for modeling a-Si TFTs. Firstly, the DOS, N_T , was assumed to be constant which is an approximation. A number of authors have proposed different DOS distributions for a-Si devices as discussed in previous sections. Next, the previous approach simplified the problem considerably by assuming that the a-Si film thickness, $t_s \ll \lambda$, the screening length parameter. In general, this may not be true and the carrier concentration in the a-Si semiconductor as a function of band bending must be accounted for. The model in the previous section also defined the TFT threshold voltage V_T as the point where the free carrier concentration was equal to the electrons trapped in the acceptor-like states above the intrinsic

carrier energy level, E_i . Again, in practice, the magnitude of voltage required to bend the conduction band to reach the Fermi level would likely cause the device to breakdown [24]. i.e. the TFT spends most of its life operating with the Fermi level some kT/q less than the conduction band. Some authors [8][11] have claimed that the Fermi level gets pinned in the tail or deep states instead of cycling up to E_C as one would expect in the ideal thin a-Si film. Therefore, V_T needs to be redefined along with above and below threshold drain current. In addition, the effects of fixed oxide charge, surface states, metal-semiconductor work function differences also have to be accounted for in a practical model. The following discussion is based on the a-Si TFT model proposed by Leroux [21] and refined by Khakzar [22].

A.7.2 Density of localized states and free carrier concentration

The developed theory assumes that the localized DOS can be approximated by two exponential band-tail state (similar to Shur's DOS in Figure 93 but neglecting the deep states) distributions for the acceptor-like and donor-like tail states,

$$N_{acceptor}(E) = \frac{N_{tc}}{kT_C} \exp\left[\frac{E - E_C}{kT_C}\right], \quad N_{donor}(E) = \frac{N_{tv}}{kT_V} \exp\left[\frac{E_V - E}{kT_V}\right]. \quad (34)$$

The densities of induced mobile charge are given by the usual:

$$n = N_C \exp\left[\frac{E_{fn} - E_C}{kT}\right] \text{ and } p = N_V \exp\left[\frac{E_V - E_{fp}}{kT}\right]. \quad (35)$$

It should be noted that the density of induced mobile charge and any charge due to $N_{donor}(E)$ [21][22][24] is considered negligible with respect to the localized trapped charge in the acceptor-like states, $N_{acceptor}(E)$. So, using eqn. (34) and Fermi-Dirac statistics yields the following expression for charge as a function of band bending potential.

$$Q(\phi) = \int f(E)N(E)dE \approx -q \int_{-\infty}^{E_C} \frac{\frac{N_{tc}}{kT_C} \exp\left[\frac{E - E_C}{kT_C}\right]}{1 + (1/g) \exp\left(\frac{E - E_f}{kT}\right)} dE \quad (36)$$

where $f(E)$ is the Fermi-Dirac distribution function making use of g , a factor to account for degenerate states in the semiconductor (around $\frac{1}{2}$ for acceptor-like states) [21]. The above equation was exactly integrated by Leroux to yield a complex expression, which is unimportant to the understanding of drain current. What is more important is that the expression may be simplified [21] to give,

$$Q(\phi) = -qn_t \exp\left[\frac{q\phi}{kT_0}\right] \quad (37)$$

$$n_t = N_t \exp\left[\frac{-q\phi_f}{kT_0}\right] \quad (38)$$

where ϕ_f is defined in Figure 97 [22]. Figure 97 will be used as the reference band diagram from this point onwards. In the figure, V_a is the applied gate voltage and V_i is the voltage drop across the insulator. For completeness, N_t is a function of temperature, T given by,

$$N_t = N_{tc} g^{T/T_c} \left[\frac{\pi T/T_c}{\sin(\pi T/T_c)} \right], T_0 = T_c \text{ for } T < T_c \quad (39)$$

$$\text{and } N_t = N_{tc} g \left[\frac{T/T_c}{(T/T_c - 1)} \right], T_0 = T \text{ for } T > T_c. \quad (40)$$

Here, we define $\alpha = T/T_0$ for later use.

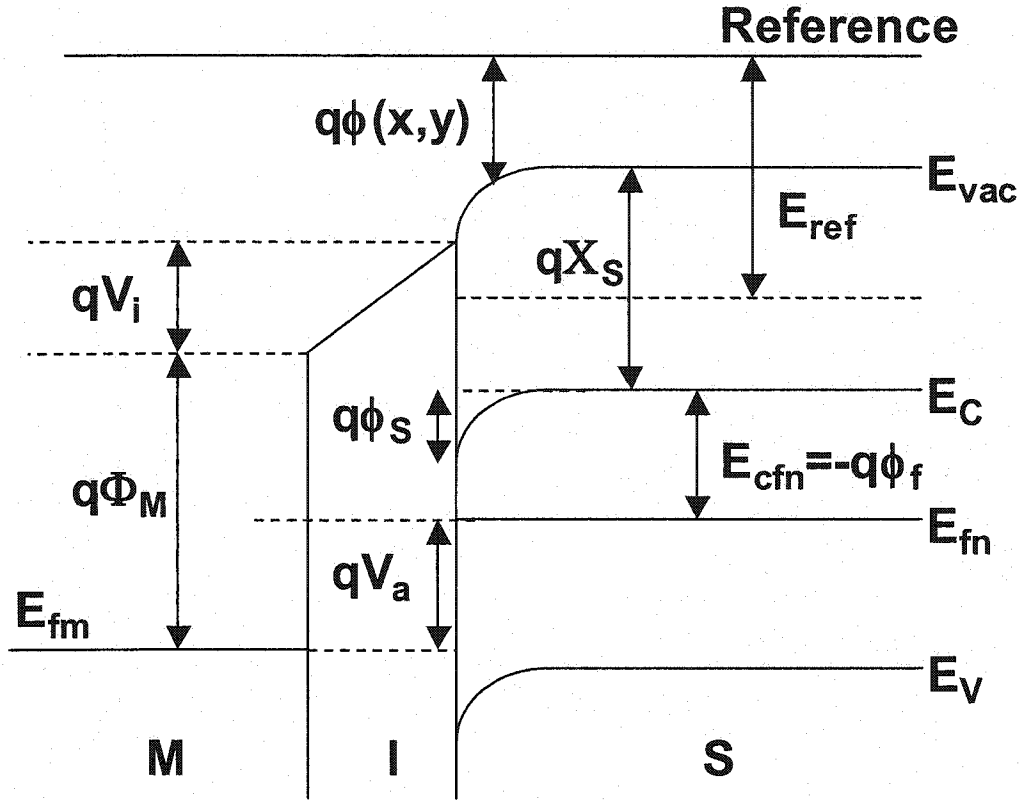


Figure 97. Band diagram for detailed drain current calculation (adapted from [22]).

A.7.3 Deriving the basic drain current equation

To obtain the TFT drain current equation, the following assumptions [21][22][23][33] are made with reference to Figure 96.

- $dI_D/dz = 0$ implying that the drain current modeling is only of interest in the x - y plane. The current is the same throughout the width of the TFT.
- $I_y = 0$ indicating no gate current which is expected in an MIS type structure. Therefore, the current equation must be solved only in the x – direction.
- $d^2\phi/dx^2 \ll d^2\phi/dy^2$ which is the gradual channel approximation and is needed to decouple the problem from the x - y plane in an x plane and a y plane problem, i.e.

Poisson's equation can be used to get the electric field distribution in the y direction without needing to consider the x electric field in the x direction.

Starting from the basic semiconductor current equation where drift and diffusion are considered [34],

$$J_n = q \left(n \mu_n E_u + D_n \frac{dn}{du} \right), \quad (41)$$

where,

$$n = N_C \exp \left(\frac{E_{fn} - E_C}{kT} \right), \quad (42)$$

where E_u is the electric field, and E_{fn} is the quasi Fermi level. Then,

$$\frac{dn}{du} = \frac{N_C}{kT} \exp \left(\frac{E_{fn} - E_C}{kT} \right) \cdot \left(\frac{dE_{fn}}{du} - \frac{dE_C}{du} \right) = \frac{n}{kT} \left(\frac{dE_{fn}}{du} - \frac{dE_C}{du} \right), \quad (43)$$

$$E_u = -\frac{dV}{du} = \frac{1}{q} \frac{dE_C}{du} = \frac{1}{q} \frac{dE_V}{du}, \quad (44)$$

Eqns. (41), (42) and (43) can be substituted into eqn. (44) to yield,

$$J_n = n \mu_n \frac{dE_{fn}}{du}, \quad (45)$$

Since $I_y = 0$, $dE_{fn}/dy = 0$ and eqn. (45) reduces to,

$$J_n = n(x, y) \mu_n \frac{dE_{fn}}{dx} = -qn(x, y) \mu_n \frac{dV_D(x)}{dx}, \quad (46)$$

where V_D is the voltage across the a-Si film from the drain to source terminal (assuming grounded source). Note that one of the factors determining the current is the slope of the quasi Fermi level in the x direction. Taking into account TFT width, Z and thickness, t_s ,

$$I_n = J_n \cdot \text{Area} = \int_0^{t_s} \int_0^Z \left(-qn(x, y) \mu_n \frac{dV_D(x)}{dx} \right) dz dy = -q \mu_n \frac{dV_D(x)}{dx} \int_0^{t_s} n(x, y) \int_0^Z dz \cdot dy, \quad (47)$$

$$I_n = -q\mu_n \frac{dV_D(x)}{dx} \int_0^{t_s} n(x, y) Z dy, \quad (48)$$

$$I_n = -q\mu_n Z \frac{dV_D(x)}{dx} \int_0^{t_s} n(x, y) dy = -q\mu_n Z \frac{dV_D(x)}{dx} n_c(x), \quad (49)$$

where $\int_0^{t_s} n(x, y) dy = n_c(x)$ takes into account the thickness of the semiconductor in the y direction. The above equation can be reduced to,

$$\int_0^L I_n dx = -q\mu_n Z \cdot \int_{V(x=0)}^{V(x=L)} n_c(x) dV_D(x) \Rightarrow I_n = -q\mu_n \frac{Z}{L} \cdot \int_{V(x=0)}^{V(x=L)} n_c(x) dV_D(x), \quad (50)$$

Here, μ_n is the band mobility of the free electrons and is assumed constant. So, from eqn. (50), the drain current problem is reduced to obtaining n_c as a function of the drain terminal voltage, V_D . Taking into account the thickness, t_s , the carrier concentration as a function of only the x direction is,

$$n_c(x) = \int_0^{t_s} n(x, y) dy = \int_0^{t_s} N_C \exp\left(\frac{-(E_C - E_{fn})}{kT}\right) dy, \quad (51)$$

From Figure 97, $(E_C - E_{fn})$ can be written as a function of the band bending as $(E_{ref} - q\phi(x, y))$ where E_{ref} is a constant reference level. In addition, after changing the variable from dy to $d\phi(x, y)$, $n_c(x)$ becomes,

$$n_c(\phi) = \int_{\phi_s}^{\phi_0} \left[\frac{N_C \exp\left(\frac{-(E_{ref} - q\phi(x, y))}{kT}\right)}{\frac{d\phi(x, y)}{dy}} \right] d\phi(x, y), \quad (52)$$

So again, the problem is further reduced to obtaining the electric field in the vertical direction, $d\phi(x, y)/dy$, the a-Si film surface potential ϕ_s at the gate insulator interface, and the a-Si film back channel potential ϕ_0 at the top interface towards the source/drain side. Once

that is done, ϕ needs to be evaluated in terms of the drain terminal voltage, V_D before eqn. (50) can be solved. Note that the drain voltage V_D , can be related to the applied voltage on the MIS structure, V_a in Figure 97 and the gate terminal voltage, V_G , (which is constant in the x-direction) via,

$$V_a(x) = V_G - V_D(x), \quad (53)$$

A.7.4 Charge and field distribution in the vertical M-I-S structure of the TFT

To obtain the electric field in the vertical direction as well as the potentials of the front and back a-Si channel, Poisson's equation needs to be solved. From the gradual channel approximation, Poisson's equation can be solved for the electric field in the y-direction neglecting the effect of the field in the x-direction. From section 2.4.2, since the charge trapped in the acceptor like states dominates, the free carrier concentration is neglected and using eqn. (37), Poisson's equation is:

$$\frac{d^2 \phi}{dy^2} = -\frac{Q(\phi)}{\epsilon_s} = \frac{qn_t}{\epsilon_s} \exp\left[\frac{q\phi(x, y)}{kT_0}\right] \quad (54)$$

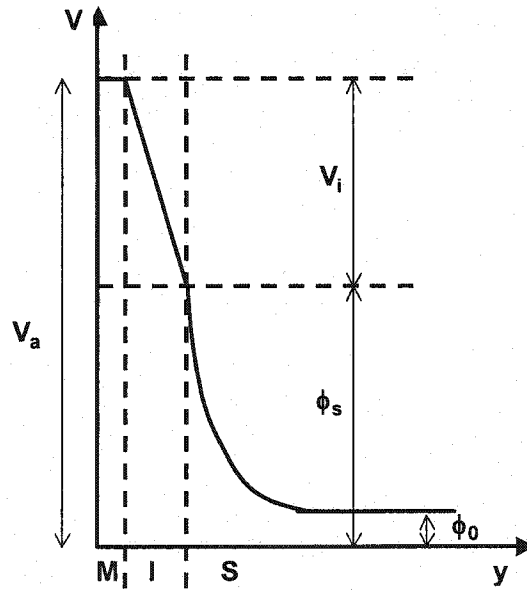


Figure 98. Potential drop in the MIS structure

Figure 98 illustrates the potential drop in the y direction in the MIS structure where V_i is the voltage drop across the insulator taking into account the contact potential, surface states and fixed oxide charges. The boundary conditions for eqn. (54) can then be written as,

$$y = t_s \text{ (back channel), } d\phi/dy = 0 \text{ (electric field is zero at back channel), } \phi = \phi_0 \quad (55)$$

$$y = 0 \text{ (front channel), } d\phi/dy = Q_C/\epsilon_s \text{ (electric field via Gauss' Law), } \phi = \phi_s \quad (56)$$

For the front channel, the electric field boundary condition can be obtained by using Gauss' Law,

$$Q_C = -\epsilon_s E(0) = -V_c C_{OX} \quad (57)$$

where $E(0)$ is the electric field at the a-Si front channel - gate insulator interface, V_c is the ideal voltage on the a-Si film across the insulator that induces the channel charge (without accounting for non-idealities like fixed oxide charge or surface states), and C_{OX} is the insulator capacitance. From Leroux [21], a first integration of eqn. (54) yields the electric field,

$$\frac{d\phi}{dy} = -\sqrt{\frac{2n_i kT_0}{\epsilon_s} \left(\exp \left[\frac{q(\phi - \phi_0)}{kT_0} \right] \right)}^{1/2} \quad (58)$$

Again, from Leroux [21], a second integration of eqn. (58) using an integrating factor yields the band bending as a function of the thickness, t_s of the a-Si film:

$$\phi = \phi_0 + \frac{kT_0}{q} \log \left[\tan \left(\frac{(t_s - y)}{2\delta} \right)^2 + 1 \right] \quad (59)$$

where,

$$\frac{1}{\delta} = q \sqrt{\frac{2n_i}{kT_0 \epsilon_s} \exp \left[\frac{q\phi_0}{2kT_0} \right]} \quad (60)$$

To obtain ϕ_s and ϕ_0 , eqn. (57) and eqn. (58) can be simplified using the boundary conditions for the front channel in eqns. (55) and (56) to yield the following pair of simultaneous equations.

$$\left. \frac{d\phi}{dy} \right|_{y=0} = E(0) = \frac{-V_c \cdot C_{ox}}{\epsilon_s} = -\sqrt{\frac{2n_i kT_0}{\epsilon_s}} \left(\exp \left[\frac{q(\phi_s - \phi_0)}{kT_0} \right] \right)^{1/2} \quad (61)$$

$$V_c \cdot C_{ox} = \sqrt{2n_i kT_0 \epsilon_s} \left(\exp \left[\frac{q(\phi_s - \phi_0)}{kT_0} \right] \right)^{1/2} \quad (62)$$

$$\frac{t_s}{2\delta} = \tan^{-1} \left(\left[\exp \left(\frac{q(\phi_s - \phi_0)}{kT_0} \right) - 1 \right]^{1/2} \right) \quad (63)$$

Leroux concluded that eqn. (62) and eqn. (63) are non-linear simultaneous equations that cannot be solved analytically. Instead, some insight can be gained from them if two cases are distinguished:

$\phi_s > \phi_0$ which implies there is band bending in the semiconductor film and,

$\phi_s \approx \phi_0$ which implies that the a-Si film thickness, $t_s \ll \lambda$, the screening length parameter indicating the previously analyzed case of a thin a-Si film in section 2.3.

For $\phi_s > \phi_0$, Leroux gave expressions for the front and back channel potentials,

$$\phi_s = \frac{kT_0}{q} \log \left[\frac{\pi^2 C_{ox}^2}{8n_i kT_0 \epsilon_s} \left[\frac{4V_c^2}{\pi^2} + \left(\frac{V_c V_0}{V_c + V_0} \right)^2 \right] \right] \quad (64)$$

$$\phi_0 = \frac{kT_0}{q} \log \left[\frac{\pi^2 C_{ox}^2}{8n_i kT_0 \epsilon_s} \left(\frac{V_c V_0}{V_c + V_0} \right)^2 \right] \quad (65)$$

where,

$$V_0 = \frac{2\varepsilon_s d \cdot kT_0}{\varepsilon_{ox} t_s q}, \text{ and } C_{ox} = \frac{\varepsilon_{ox}}{d} \quad (66)$$

In most TFTs, the first case of $\phi_s > \phi_0$ is true [21][25] and is more accurate. This case will be explored further in the next few sections. It should be noted that V_0 defines a limit between the above two cases of ϕ_s and ϕ_0 . In the first case, $\phi_s > \phi_0$, it can be noted by comparing eqn. (64) to eqn. (65) that $V_c \gg V_0$. Here, the conducting channel is near the insulator/a-Si interface while in the second case, $\phi_s \approx \phi_0$ ($V_c \ll V_0$), conduction takes place in the whole film's thickness.

A.7.5 Surface states, oxide charge and metal-semiconductor work function

Using the relation, $n_i = N_i \exp\left[\frac{-q\phi_f}{kT_0}\right]$ from eqn. (37), eqn. (64), and the case $\phi_s > \phi_0$, $V_c \gg V_0$,

$$\phi_s = \frac{kT_0}{q} \log \left[\frac{\pi^2 C_{ox}^2}{8n_i kT_0 \varepsilon_s} \left[\frac{4V_c^2}{\pi^2} + \left(\frac{V_c V_0}{V_c + V_0} \right)^2 \right] \right] \approx \frac{kT_0}{q} \log \left[\frac{\pi^2 C_{ox}^2}{8n_i kT_0 \varepsilon_s} \left[\frac{4V_c^2}{\pi^2} \right] \right] \quad (67)$$

$$\phi_s \approx \frac{kT_0}{q} \log \left[\frac{\pi^2 C_{ox}^2}{8n_i kT_0 \varepsilon_s} \left[\frac{4V_c^2}{\pi^2} \right] \right] = \frac{kT_0}{q} \log \left[\frac{V_c C_{ox}}{\sqrt{2n_i kT_0 \varepsilon_s}} \right]^2 \quad (68)$$

$$\phi_s = \frac{kT_0}{q} \log \left[\frac{V_c C_{ox}}{\sqrt{2N_i \exp\left[\frac{-q\phi_f}{kT_0}\right] kT_0 \varepsilon_s}} \right]^2 \quad (69)$$

$$\phi_s = \frac{2kT_0}{q} \log \left[\frac{V_c}{V_i} \right] + \phi_f \quad (70)$$

where,

$$V_i = \frac{\sqrt{2kT_0 N_t \epsilon_s}}{C_{ox}} \text{ and } \phi_f = -\frac{E_{fn}}{q}. \quad (71)$$

Note that V_i is the magnitude of the voltage across the insulator that, when $V_c = V_i$ in eqn. (70), will pull the Fermi level into the conduction band (see Figure 97), causing a large increase in TFT drain current. Also, V_i is directly proportional to square root of N_t implying an increase in N_t will cause a proportional increase in V_i , requiring a large V_c in turn to make the Fermi level reach the conduction band. So increasing the number of traps will degrade TFT characteristics as expected and typical values for N_t range from 10^{19} to 10^{20} states/cm³ [8][21]. Typical values for V_i range upwards of 35 V. The applied gate voltage required to supply a $V_c = V_i$ will be very high and possibly in the range where the gate insulator would be close to breaking down.

Using Figure 97 to relate V_a to the surface band bending ϕ_s , $(V_a - V_i)$ can be written as,

$$V_a - V_i = (\Phi_M - X_s - E_{fn}/q) - \phi_s \quad (72)$$

where the first term in brackets on the right hand side of eqn. (72) represents the metal-semiconductor work function difference and the second term, ϕ_s , is the surface band bending. The left hand side equals $V_a - V_i$, the difference between the applied voltage to the M-I-S structure and the actual drop across the insulator (including non-ideal effects like surface states and fixed oxide charge). To account for the effect of fixed oxide charges in the insulator, Q_f , surface states, N_{ss} and to relate the non-ideal insulator voltage drop, V_i to V_c , the electric field continuity can be used to obtain,

$$C_{ox}V_i + Q_f = C_{ox}V_c + q^2 N_{ss} \phi_s \quad (73)$$

where V_i is the actual voltage across the insulator that has to deal with fixed oxide charge, surface states and work function differences, and V_c is a subset of V_i as the ideal voltage across the insulator that induces the accumulation mode charge. Combining eqns. (70), (72)

and (73), the following transcendental equation relating the applied voltage, V_a and V_c can be written:

$$V_c - \frac{Q_f}{C_{ox}} + \frac{2kT_0}{q} \left(1 + \frac{q^2 N_{ss}}{C_{ox}} \right) \log \left[\frac{V_c}{V_1} \right] + \frac{q^2 N_{ss} \phi_f}{C_{ox}} + \phi_f = \phi_f + V_a - \Phi_m + X_s \quad (74)$$

$$V_a - \left(\Phi_m - X_s - \frac{Q_f}{C_{ox}} + \frac{q^2 N_{ss} \phi_f}{C_{ox}} \right) = V_c + \frac{2kT_0}{q} \left(1 + \frac{q^2 N_{ss}}{C_{ox}} \right) \log \left[\frac{V_c}{V_1} \right] \quad (75)$$

where,

$$V_{T0} = \left(\Phi_m - X_s - \frac{Q_f}{C_{ox}} + \frac{q^2 N_{ss} \phi_f}{C_{ox}} \right) \text{ and } V_2 = \frac{2kT_0}{q} \left(1 + \frac{q^2 N_{ss}}{C_{ox}} \right) \quad (76)$$

giving the summarized form of the transcendental function [22],

$$V_a - V_{T0} = V_c + V_2 \log \left[\frac{V_c}{V_1} \right] \quad (77)$$

Since, in practice, V_c never really reaches V_1 , eqn. (77) can be simplified for the case where $V_c < V_1$ making the log term negative for numbers less than one. Two cases arise: if $|V_2 \cdot \log[V_c/V_1]| < V_c$ or if $|V_2 \cdot \log[V_c/V_1]| > V_c$. For the former, $|V_2 \cdot \log[V_c/V_1]| < V_c$ makes $V_a - V_{T0} > 0$. Leroux [21] approximated this function relating V_c to V_a for $V_a - V_{T0} > 0$ by,

$$V_c \approx V_a - \left(V_{T0} + V_2 - V_2 \log \left[\frac{V_1}{V_2} \right] \right) \quad (78)$$

while Khakzar [22] fitted a curve of the form,

$$V_c = \frac{1}{1 + \frac{5}{2} \frac{V_1}{V_2}} V_a - \frac{1}{1 + \frac{5}{2} \frac{V_1}{V_2}} \left(V_{T0} - \frac{5}{2} V_2 \right) \quad (79)$$

For $|V_2 \cdot \log[V_c/V_1]| > V_c$, $V_a - V_{T0} < 0$ and it can only happen if V_c is made very small making $V_c/V_1 \ll 1$ which consequently makes $|V_2 \cdot \log[V_c/V_1]| \gg 1$. For $V_a - V_{T0} < 0$ and $V_2 < 1$, both Leroux and Khakzar approximated eqn. (77) for $V_a - V_{T0} < 0$ as,

$$V_a - V_{T0} \approx V_2 \log \left[\frac{V_c}{V_1} \right] \quad (80)$$

giving,

$$V_c \approx V_1 \exp \left[\frac{V_a - V_{T0}}{V_2} \right] \quad (81)$$

In a way, eqn. (78) and eqn. (81) define above threshold and sub-threshold operation for a TFT where the threshold voltage using eqn. (78) is defined as:

$$V_T = V_{T0} + V_2 - V_2 \log \left(\frac{V_1}{V_2} \right) \quad (82)$$

An examination of eqn. (77) reveals that the applied voltage V_a is split between V_c and a couple of other terms. V_{T0} accounts for the effect of metal semiconductor work function difference, effective fixed oxide charge and surface state density. $(V_2 \cdot \log[V_c/V_1])$ takes into account a surface state density but more importantly, it also accounts for the effect of traps in the a-Si semiconductor via the V_1 term. As discussed earlier, a larger number of traps increases V_1 , and since $V_c < V_1$ in general, the absolute value of the log term increases. This decreases the magnitude of the V_c term implying less band bending, and fewer carriers available for conduction and poor TFT performance, which is logical.

A.7.6 Static drain current for above and below threshold

In order to calculate the current/voltage characteristics, there is a requirement to know $n_c(\phi)$ given in eqn. (52). The original problem was to obtain the electric field in the vertical direction, $d\phi(x,y)/dy$, the a-Si film surface potential ϕ_s at the gate insulator interface, and the a-Si film back channel potential ϕ_0 at the top interface towards the source/drain side in order to solve eqn. (52) which was accomplished in section 2.4.4. In addition, it is necessary to relate the applied drain voltage V_D to the band bending potential ϕ across the a-Si film as well as accounting for the fixed oxide charges, surface states and metal-semiconductor work function differences. Thus, using eqn. (62) and the boundary condition in eqn. (56), eqn. (52) is solved in Leroux [21] to yield the following expression for $n_c(V_c)$ where V_c is a function of the surface band bending, ϕ_s :

$$n_c(V_c) = \frac{kT}{q} \frac{2N_c \epsilon_s}{(2 - \alpha_1)(2\epsilon_s kT_0 N_t)^{1-\alpha}} (C_{ox} V_c)^{\frac{2}{\alpha_1}-1} \quad (83)$$

Eqn. (83) along with equations (78) and (81) relate V_a to V_c (and hence $n_c(V_c)$ to $n_c(V_a)$) for above and below threshold regions of operation. Lastly, eqn. (53) relates V_a to V_D allowing computation of the drain current from eqn. (50). For $V_a < V_T$ or the subthreshold regime of operation, the drain current equation [21][22] becomes,

$$I_{subt} = I_0 \left[\exp \left(\frac{(2 - \alpha_1)(V - V_{T0})}{\alpha_1 V_2} \right) \right]_{V_{GD}}^{V_{GS}} \quad (84)$$

where,

$$I_0 = \mu_n \frac{Z}{L} \frac{2\alpha_1}{(2 - \alpha_1)^2} \frac{kTN_c \epsilon_s V_2}{C_{ox} V_1}, \quad \alpha_1 = \frac{T}{T_0} \quad (85)$$

and $T_0 = T_C$ for $T < T_C$, $T_0 = T$ for $T > T_C$.

For $V_a > V_T$ or the above threshold regime of operation, the drain current equation [21][22] becomes,

$$I_D = \mu_n \frac{Z}{L} \frac{\alpha_1}{2 - \alpha_1} \frac{kTN_c \epsilon_s}{C_{ox}} \left[\left(\frac{(V - V_T)}{V_1} \right)^\alpha \right]_{V_{GD}}^{V_{GS}} \quad (86)$$

$$I_D = \mu_n \frac{Z}{L} \frac{\alpha_1}{2 - \alpha_1} \frac{kTN_c \epsilon_s}{C_{ox}} \left[\left(\frac{(V_{GS} - V_T)}{V_1} \right)^\alpha - \left(\frac{(V_{GD} - V_T)}{V_1} \right)^\alpha \right] \quad (87)$$

where $\alpha = 2T_C/T$.

Note than eqn. (87) for above threshold, much like eqn. (84) for subthreshold are both implicitly defined for the linear region of operation, i.e $V_{DS} < V_{GS} - V_T$. As an example, to obtain saturation region operation for eqn. (86), set $V_{DS} = (V_{GS} - V_T)$ for $V_{DS} \geq (V_{GS} - V_T)$ to obtain [22],

$$I_D = \mu_n \frac{Z}{L} \frac{\alpha_1}{2 - \alpha_1} \frac{kTN_c \epsilon_s}{C_{ox}} \left(\frac{(V_{GS} - V_T)}{V_1} \right)^\alpha \quad (88)$$

A.8 Comparison with other a-Si TFT models in literature

The model derived by Khakzar [22] is very similar to that of Leroux [21] in theory. The main differences lie in the choice of the DOS where Khakzar used a double exponential (compared to the single exponential used by Leroux) which required numerical approximation and curve fitting terms i.e. a closed form solution to yield eqn. (32) was not possible. In addition, Khakzar approximated the transcendental eqn. (62) differently as mentioned in the previous section. The model presented by Khakzar, where the basic forward drain current theory is identical to that of Leroux, is meant for use in a circuit simulator (e.g Spice) and as such, it includes additional equations to ensure that the transition from subthreshold to threshold is a smooth one that avoids convergence issues.

In comparison, Shur [8][24] uses the concept of a gate voltage dependent field effect mobility, μ_{FET} , to model the TFT drain current. To recap a little, for an a-Si TFT, nearly all of the induced charge goes into deep localized states as well as into any gate insulator-semiconductor film surface states during the subthreshold regime of operation. With increasing positive voltage, more of the localized states in the upper half of the mobility gap are filled and the Fermi level at the a-Si insulator interface moves closer to the conduction band. This leads to an increase in the concentration of mobile electrons in the conduction band, which rises rapidly with gate voltage. The conduction band tail state density increases very rapidly with energy (see Figure 93) and at room temperature, when the Fermi level enters these states, most of the induced charge resides in states above the Fermi level. In this above threshold regime, the field-effect mobility is still much smaller than the band mobility, but it increases with increasing gate voltage as the Fermi level moves even closer to the conduction-band edge. At high gate fields it is possible, although unlikely, for the Fermi level to enter the conduction band (similar to Greve's model) giving rise to another operating regime (i.e. a MOS-like above threshold). The source-drain current I_D using Shur's method is computed differently as shown below. Starting with the common I_D equation,

$$I_D = q\mu_n n Z(dV/dx) \quad (89)$$

where n is the number of free carriers given by the ratio proposed by Shur [24],

$$N = (\mu_{FET}/\mu_n)n_{ind} \quad (90)$$

where n_{ind} is the total induced charge comprising of free and trapped electrons in the band tail states, μ_n is the band mobility and μ_{FET} is a field effect mobility. Then, substituting eqn. (90) into eqn. (89), the I_D integral can be written,

$$I_D = q \frac{Z}{L} \cdot \int_0^{V_{DS}} n_{ind} \mu_{FET}(n_{ind}) dV \quad (91)$$

where μ_{FET} needs to be evaluated as a function of induced charge. Compared to Leroux's integral in eqn. (50) where the number of carriers is evaluated as a function of applied voltage, Shur's integral requires computation of the induced charge as well as μ_{FET} . Shur's approach is an equally valid alternative to Leroux's approach except more numerical computation and non-physical parameters are required. In addition, Shur's model does not include any analytic expressions accounting for the temperature dependency of the current voltage characteristics unlike Leroux or Khakzar.

Appendix B – VHDL-AMS Model

An a-Si TFT model was implemented in VHDL-AMS by the author [47], based on the in-house a-Si TFT model developed by Servati [46] that included forward, reverse and dynamic current components. The dynamic part of the model is important since the parasitic overlap capacitances are accounted for to include second-order effects like charge feedthrough. A schematic of the implemented model is shown in Figure 99. The two opposing current sources account for TFT conduction in the forward regime as well as the front and back channel conduction components of the reverse regime leakage current [64]. Two voltage dependent parasitic capacitances, C_{GS} and C_{GD} , have also been included in this model in addition to the drain, source and channel resistances: R_D , R_S and R_{DS} respectively. All of the model code has been provided here. The a-Si TFT model was compared with actual measured values and is accurate to within 5%. For further details on the model including the physics of the TFT leakage current and transient performance, the reader is referred to [46].

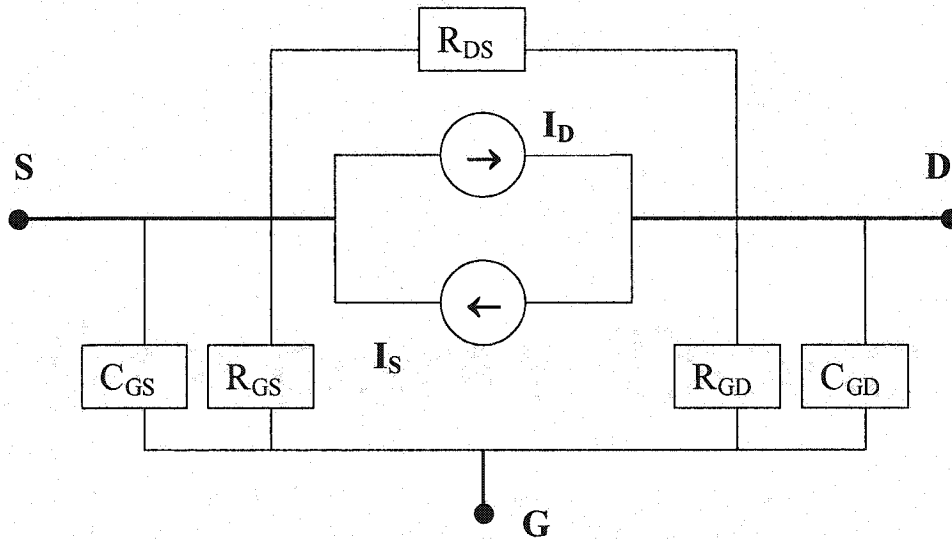


Figure 99. Static and Dynamic a-Si TFT model.

VHDL-AMS Model Code

1. 5 x 4 APS Array

```
library DISCIPLINES, IEEE, array_lib;
use disciplines.electromagnetic_system.all;
use IEEE.math_real.all;
```

```
entity APSarray is
  port (terminal read0, read1, read2, read3, read4:
    electrical;
        terminal rst0, rst1, rst2, rst3, rst4: electrical;
        terminal out0, out1, out2, out3: electrical;
        terminal Prail, SensorBias, LoadTFTBias :
    electrical);
end entity APSarray;
```

```
architecture FivebyFour of APSarray is
  constant LD_W: REAL:= 70.0e-6;
begin
```

```
  APS1x1: entity
    ARRAY_lib.APS(VOLTAGE_SENSING)
    generic map (I_PHOTO => 1.0E-12)
    port map (rst0, read0, out0, Prail, SensorBias);
```

```
  APS2x1: entity
    ARRAY_lib.APS(VOLTAGE_SENSING)
    generic map (I_PHOTO => 1.0E-11)
    port map (rst1, read1, out0, Prail, SensorBias);
```

```
  APS3x1: entity
    ARRAY_lib.APS(VOLTAGE_SENSING)
    generic map (I_PHOTO => 1.0E-10)
    port map (rst2, read2, out0, Prail, SensorBias);
```

```
  APS4x1: entity
    ARRAY_lib.APS(VOLTAGE_SENSING)
    generic map (I_PHOTO => 1.0E-12)
    port map (rst3, read3, out0, Prail, SensorBias);
```

```
  APS5x1: entity
    ARRAY_lib.APS(VOLTAGE_SENSING)
    generic map (I_PHOTO => 1.0E-11)
    port map (rst4, read4, out0, Prail, SensorBias);
```

```
  APS1x2: entity
    ARRAY_lib.APS(VOLTAGE_SENSING)
    generic map (I_PHOTO => 1.0E-10)
    port map (rst0, read0, out1, Prail, SensorBias);
```

```
  APS2x2: entity
    ARRAY_lib.APS(VOLTAGE_SENSING)
    generic map (I_PHOTO => 1.0E-12)
```

```
    port map (rst1, read1, out1, Prail, SensorBias);
```

```
  APS3x2: entity
    ARRAY_lib.APS(VOLTAGE_SENSING)
    generic map (I_PHOTO => 1.0E-11)
    port map (rst2, read2, out1, Prail, SensorBias);
```

```
  APS4x2: entity
    ARRAY_lib.APS(VOLTAGE_SENSING)
    generic map (I_PHOTO => 1.0E-10)
    port map (rst3, read3, out1, Prail, SensorBias);
```

```
  APS5x2: entity
    ARRAY_lib.APS(VOLTAGE_SENSING)
    generic map (I_PHOTO => 1.0E-12)
    port map (rst4, read4, out1, Prail, SensorBias);
```

```
  APS1x3: entity
    ARRAY_lib.APS(VOLTAGE_SENSING)
    generic map (I_PHOTO => 1.0E-11)
    port map (rst0, read0, out2, Prail, SensorBias);
```

```
  APS2x3: entity
    ARRAY_lib.APS(VOLTAGE_SENSING)
    generic map (I_PHOTO => 1.0E-10)
    port map (rst1, read1, out2, Prail, SensorBias);
```

```
  APS3x3: entity
    ARRAY_lib.APS(VOLTAGE_SENSING)
    generic map (I_PHOTO => 1.0E-12)
    port map (rst2, read2, out2, Prail, SensorBias);
```

```
  APS4x3: entity
    ARRAY_lib.APS(VOLTAGE_SENSING)
    generic map (I_PHOTO => 1.0E-11)
    port map (rst3, read3, out2, Prail, SensorBias);
```

```
  APS5x3: entity
    ARRAY_lib.APS(VOLTAGE_SENSING)
    generic map (I_PHOTO => 1.0E-10)
    port map (rst4, read4, out2, Prail, SensorBias);
```

```
  APS1x4: entity
    ARRAY_lib.APS(VOLTAGE_SENSING)
    generic map (I_PHOTO => 1.0E-12)
    port map (rst0, read0, out3, Prail, SensorBias);
```

```
  APS2x4: entity
    ARRAY_lib.APS(VOLTAGE_SENSING)
    generic map (I_PHOTO => 1.0E-11)
    port map (rst1, read1, out3, Prail, SensorBias);
```

```
  APS3x4: entity
    ARRAY_lib.APS(VOLTAGE_SENSING)
    generic map (I_PHOTO => 1.0E-10)
    port map (rst2, read2, out3, Prail, SensorBias);
```

```

APS4x4: entity
ARRAY_lib.APS(VOLTAGE_SENSING)
  generic map (I_PHOTO => 1.0E-12)
  port map (rst3, read3, out3, Prail, SensorBias);

APS5x4: entity
ARRAY_lib.APS(VOLTAGE_SENSING)
  generic map (I_PHOTO => 1.0E-11)
  port map (rst4, read4, out3, Prail, SensorBias);

LOAD1_TFT: entity ARRAY_lib.tft(bhv)
  generic map (W => LD_W)
  port map (out0, LoadTFTBias,
electrical_ground);

LOAD2_TFT: entity ARRAY_lib.tft(bhv)
  generic map (W => LD_W)
  port map (out1, LoadTFTBias,
electrical_ground);

LOAD3_TFT: entity ARRAY_lib.tft(bhv)
  generic map (W => LD_W)
  port map (out2, LoadTFTBias,
electrical_ground);

LOAD4_TFT: entity ARRAY_lib.tft(bhv)
  generic map (W => LD_W)
  port map (out3, LoadTFTBias,
electrical_ground);

end architecture FivebyFour;

```

2. APS Architecture

```

library DISCIPLINES, IEEE, array_lib;
use disciplines.electromagnetic_system.all;
use IEEE.math_real.all;

entity APS is
  generic ( RST_W: real:= 70.0e-6;
    RD_W : real:= 80.0e-6;
    SF_W: real:= 140.0e-6;
    C_DIODE: real:= 1.0e-12;
    R_DIODE: real:= 1.0e11;
    I_DARK: real:= 1.97e-12; -- for fluoro
    I_PHOTO: real:= 7.86e-12); -- for fluoro
  port (terminal reset, readout, output : electrical;
    terminal Prail, SensorBias : electrical);
end entity APS;

architecture voltage_sensing of APS is

```

```

  terminal A, B: electrical;

begin

RST_TFT: entity ARRAY_lib.tft(bhv)
  generic map (W => RST_W)
  port map (Prail, reset, A);

SF_TFT: entity ARRAY_lib.tft(bhv)
  generic map (W => SF_W)
  port map (Prail, A, B);

RD_TFT: entity ARRAY_lib.tft(bhv)
  generic map (W => RD_W)
  port map (B, readout, output);

DIODE_CAP: entity ARRAY_lib.capacitor(ideal)
  generic map (C => C_DIODE)
  port map (A, SensorBias);

DIODE_RES: entity ARRAY_lib.resistor(ideal)
  generic map (R => R_DIODE)
  port map (A, SensorBias);

PHOTOCURRENT: entity
ARRAY_lib.CurrentSource(ideal)
  generic map (J => I_PHOTO)
  port map (A, SensorBias);

DARKCURRENT: entity
ARRAY_lib.CurrentSource(ideal)
  generic map (J => I_DARK)
  port map (A, SensorBias);

end architecture voltage_sensing;

```

3. TFT Components

```

library DISCIPLINES, IEEE, array_lib;
use disciplines.electromagnetic_system.all;
use IEEE.math_real.all;

entity tft is
  generic (
    W: real:= 70.0e-6;
    L: real:= 20.0e-6;
    alpha: real:= 2.3;
    beta: real:= 0.0;
    gamma_n: real:= 1.0;
    gamma_p: real:= 1.0;
    Vt: real:= 3.5;
    Subt_slope: real:= 1.3; -- 5V/decade
    SC: real:= 1.0;
    lambda: real:= 0.0;

```

```

K:      real:= 0.0;
Koff:   real:= 0.0;
Roff:   real:= 20.0e6;
Rins:   real:= 20.0e6;
Overlap: real:= 2.0e-6;
C0:     real:= 1.0e-6;
Va:     real:= 1.0
);
port (terminal drain, gate, source : electrical);
end entity tft;

```

architecture bhv of tft is

begin

```

R_GD: entity ARRAY_lib.TFT_RES(insulator)
  generic map (W => W,
    Rins => Rins,
    Overlap => Overlap)
  port map (gate, drain);

```

```

R_GS: entity ARRAY_lib.TFT_RES(insulator)
  generic map (W => W,
    Rins => Rins,
    Overlap => Overlap)
  port map (gate, source);

```

```

R_DS: entity ARRAY_lib.TFT_RES(channel)
  generic map (W => W,
    L => L,
    Roff => Roff)
  port map (drain, source);

```

```

C_GD: entity ARRAY_lib.TFT_CAP(bhv)
  generic map (W => W)
  port map (drain, gate);

```

```

C_GS: entity ARRAY_lib.TFT_CAP(bhv)
  generic map (W => W)
  port map (source, gate);

```

```

I_D: entity ARRAY_lib.TFT_ISRC(bhv)
  generic map (W => W,
    L => L,
    alpha => alpha,
    beta  => beta,
    gamma_n => gamma_n,
    gamma_p => gamma_p,
    Vt     => Vt,
    Subt_slope => Subt_slope,
    SC      => SC,
    lambda  => lambda,
    K        => K,
    Koff     => Koff,
    Roff     => Roff,
    Va       => Va
  )

```

```

)
port map (drain, source, gate);
I_S: entity ARRAY_lib.TFT_ISRC(bhv)
  generic map (W => W,
    L => L,
    alpha  => alpha,
    beta   => beta,
    gamma_n => gamma_n,
    gamma_p => gamma_p,
    Vt      => Vt,
    Subt_slope => Subt_slope,
    SC       => SC,
    lambda   => lambda,
    K         => K,
    Koff      => Koff,
    Roff      => Roff,
    Va        => Va
  )
  port map (source, drain, gate);

```

end architecture bhv;

TFT RESISTANCES:

```

library DISCIPLINES, IEEE, array_lib;
use disciplines.electromagnetic_system.all;
use IEEE.math_real.all;

```

entity tft_res is

```

  generic (
    Roff: real:= 0.0;
    W:    real:= 70.0e-6;
    Overlap: real:= 2.0e-6;
    Rins:  real:= 0.0;
    L:     real:= 20.0e-6
  );
  port (terminal p, m : electrical);
end entity tft_res;

```

architecture channel of tft_res is

```

  quantity Vres across Ires through p to m;
  constant R_TFT: REAL:= 1.0E14;

```

begin

```

  Ires == Vres/R_TFT;

```

end architecture channel;

architecture insulator of tft_res is

```

  quantity Vres across Ires through p to m;
  constant R_TFT: REAL:= (Rins/(Overlap*W)) ;

```

```
begin
```

```
Ires == Vres/R_TFT;
```

```
end architecture insulator;
```

TFT CAPACITANCES:

```
library DISCIPLINES, IEEE, array_lib;
use disciplines.electromagnetic_system.all;
use IEEE.math_real.all;
```

```
entity tft_cap is
```

```
generic (
```

```
W:      real:= 70.0e-6;
```

```
L:      real:= 70.0e-6;
```

```
C0:     real:= 1.0e-12;
```

```
C0a:    real:= 1.0e-12;
```

```
Va:     real:= 1.0e-12;
```

```
Overlap: real:= 2.0e-6
```

```
);
```

```
port (terminal p, m : electrical);
```

```
end entity tft_cap;
```

```
architecture bhv of tft_cap is
```

```
constant Cox: real:= C0*W*L;
```

```
quantity volt across curr through p to m;
```

```
quantity C: real:= 0.0;
```

```
quantity V_C: real:= 0.0;
```

```
begin
```

```
V_C == C0a*exp(volt/Va);
```

```
C == C0*W*Overlap+V_C*Cox/(Cox+V_C);
```

```
curr == C * volt'dot;
```

```
end architecture bhv;
```

TFT CURRENT SOURCES:

```
library DISCIPLINES, IEEE, array_lib;
use disciplines.electromagnetic_system.all;
use IEEE.math_real.all;
```

```
entity tft_isrc is
```

```
generic (
```

```
W:      real:= 70.0e-6;
```

```
L:      real:= 20.0e-6;
```

```
alpha:  real:= 0.0;
```

```
beta:   real:= 0.0;
```

```
gamma_n: real:= 0.0;
```

```
gamma_p: real:= 0.0;
```

```
Vt:     real:= 3.5;
```

```
Subt_slope: real:= 0.7; -- 5V/decade
```

```
SC:     real:= 0.0;
```

```
lambda:  real:= 0.0;
```

```
K:      real:= 0.0;
```

```
Koff:   real:= 0.0;
```

```
Roff:   real:= 0.0;
```

```
Overlap: real:= 2.0e-6;
```

```
Va:     real:= 0.0
```

```
);
```

```
port (terminal p, m, n : electrical);
```

```
end entity tft_isrc;
```

```
architecture bhv of TFT_ISRC is
```

```
quantity Vgs across Igs through n to m;
```

```
quantity Vds across Ids through p to m;
```

```
quantity Vgd across Igd through n to p;
```

```
constant I0a: REAL:= 1.0E-7;
```

```
constant I0s: REAL:= I0a * 1.0E-5;
```

```
constant I0lf: REAL:= I0a * 1.0E-23;
```

```
constant Vtm: REAL:= 5.0;
```

```
begin
```

```
if (Vgs >= Vtm) use
```

```
Ids == (W/L)*I0a*(((Vgs/Vt) -
1.0)**alpha)*(1.0+lambda*Vds);
```

```
elsif ( (Vgs >= 0.0) and (Vgs < Vtm) ) use
```

```
Ids == (W/L)*I0s*
exp((2.3)*Vgs/Subt_slope)*(1.0+lambda*Vds);
```

```
elsif ( (Vgs < 0.0) and (Vds > (-Vgs/10.0)) ) use
```

```
Ids ==
(W/L)*I0s*exp((2.3)*Vgs/gamma_n)*(1.0+lambda
*Vds)+
(W*Overlap)*I0lf*exp((-
Vgd/SC)+(gamma_p*Vds));
```

```
else -- if ( (Vgs < 0.0) and not (Vds > (-
Vgs/10.0)) ) use
```

```
Ids == (W/L)*I0s*
exp((2.3)*Vgs/gamma_n)*(1.0+lambda*Vds);
end use;
```

```
Igs == 0.0;
```

```
Igd == 0.0;
```

```
break on Vgs'above(Vtm), Vgs'above(0.0),
Vds'above(-Vgs/10.0);
```

```
end architecture bhv;
```

4. DEMUX Architecture

```
library DISCIPLINES, IEEE,array_lib;
use disciplines.electromagnetic_system.all;
```

```

use IEEE.math_real.all;

entity decoder is
  generic ( Ron : real:= 1.0e1;
           Roff: real:= 1.0e12);
  port   (terminal tin : electrical;
          terminal tout0, tout1, tout2, tout3, tout4:
            electrical;
          signal ctrl: in bit_vector(2 downto 0);
          signal enable: in bit);
end entity decoder;

```

architecture bhv of decoder is

```

  quantity vin across iin through tin to
  electrical_ground;
  quantity vsw0 across isw0 through tin to tout0;
  quantity vsw1 across isw1 through tin to tout1;
  quantity vsw2 across isw2 through tin to tout2;
  quantity vsw3 across isw3 through tin to tout3;
  quantity vsw4 across isw4 through tin to tout4;

```

begin

```

  if (enable = '1' and ctrl = "000") use
    isw0 == vsw0/Ron;
  else
    isw0 == vsw0/Roff;
  end use;

```

```

  if (enable = '1' and ctrl = "001") use
    isw1 == vsw1/Ron;
  else
    isw1 == vsw1/Roff;
  end use;

```

```

  if (enable = '1' and ctrl = "010") use
    isw2 == vsw2/Ron;
  else
    isw2 == vsw2/Roff;
  end use;

```

```

  if (enable = '1' and ctrl = "011") use
    isw3 == (vsw3)/Ron;
  else
    isw3 == (vsw3)/Roff;
  end use;

```

```

  if (enable = '1' and ctrl = "100") use
    isw4 == vsw4/Ron;
  else
    isw4 == vsw4/Roff;
  end use;

```

break on enable, ctrl;

```

iin == 0.0;

```

end architecture bhv;

5. MUX Architecture

```

library DISCIPLINES, IEEE,array_lib;
use disciplines.electromagnetic_system.all;
use IEEE.math_real.all;

```

entity mux is

```

  generic ( Ron : real:= 1.0e1;
           Roff: real:= 1.0e12);
  port   (terminal tout : electrical;
          terminal tin0, tin1, tin2, tin3, tin4:
            electrical;
          signal ctrl: in bit_vector(2 downto 0);
          signal enable: in bit);
end entity mux;

```

architecture bhv of mux is

```

  quantity vout across iout through tout to
  electrical_ground;
  quantity vsw0 across isw0 through tin0 to tout;
  quantity vsw1 across isw1 through tin1 to tout;
  quantity vsw2 across isw2 through tin2 to tout;
  quantity vsw3 across isw3 through tin3 to tout;
  quantity vsw4 across isw4 through tin4 to tout;

```

begin

```

  if (enable = '1' and ctrl = "000") use
    isw0 == vsw0/Ron;
  else
    isw0 == vsw0/Roff;
  end use;

```

```

  if (enable = '1' and ctrl = "001") use
    isw1 == vsw1/Ron;
  else
    isw1 == vsw1/Roff;
  end use;

```

```

  if (enable = '1' and ctrl = "010") use
    isw2 == vsw2/Ron;
  else
    isw2 == vsw2/Roff;
  end use;

```

```

  if (enable = '1' and ctrl = "011") use
    isw3 == (vsw3)/Ron;
  else
    isw3 == (vsw3)/Roff;

```

```

end use;

if (enable = '1' and ctrl = "100") use
    isw4 == vsw4/Ron;
else
    isw4 == vsw4/Roff;
end use;
break on enable, ctrl;
iout == 0.0;
end architecture bhv;

```

6. A/D Architecture

```

LIBRARY disciplines;
USE disciplines.electromagnetic_system.all;

```

```

entity adc is
    generic (vmin      : REAL;
             vmax      : REAL;
             bus_width : NATURAL := 8;
             delay      : TIME := 0 ns);

    PORT ( start : IN bit;
           clock : IN bit;
           eoc   : OUT bit;
           d     : OUT bit_vector((bus_width-1)
                                   downto 0);
           TERMINAL input, ref: electrical
           );
end entity adc;

```

```

architecture sa of adc is

```

```

    quantity vin across iin through input to ref;

```

```

begin

```

```

    iin == 0.0;
    entity_adc: assert (vmax > vmin)
        REPORT " vmax is less than vmin "
        SEVERITY ERROR;

```

```

    clock_proc: PROCESS

```

```

        VARIABLE d_drv      : bit_vector((bus_width-
1) downto 0);
        VARIABLE delta_v    : REAL := 0.0;
        VARIABLE input_hold : REAL := 0.0;
        VARIABLE counter    : INTEGER :=
d_drv'HIGH;
        VARIABLE conv_flag  : BOOLEAN :=
FALSE;
        begin

```

```

            wait on start, clock;
            if start'EVENT and start = '1' then
                delta_v := vmax - vmin;
                input_hold := vin - vmin;
                counter := d'HIGH;
                conv_flag := TRUE;
                eoc <= '0';
            end if;

```

```

            if clock'EVENT AND clock = '1' AND
conv_flag then
                delta_v := delta_v/2.0;

```

```

                if input_hold >= delta_v then
                    d_drv(counter) := '1';
                    input_hold := input_hold - delta_v;
                else
                    d_drv(counter) := '0';
                end if;

```

```

                if counter = 0 then
                    eoc <= '1';
                    for i in d_drv'HIGH downto d_drv'LOW
LOOP
                        d(i) <= d_drv(i) after delay;
                    end loop;
                    conv_flag := FALSE;
                else
                    counter := counter - 1;
                end if;

```

```

            end if;
        end process;
    end architecture sa;

```

Appendix C – TFT Parameter Extraction

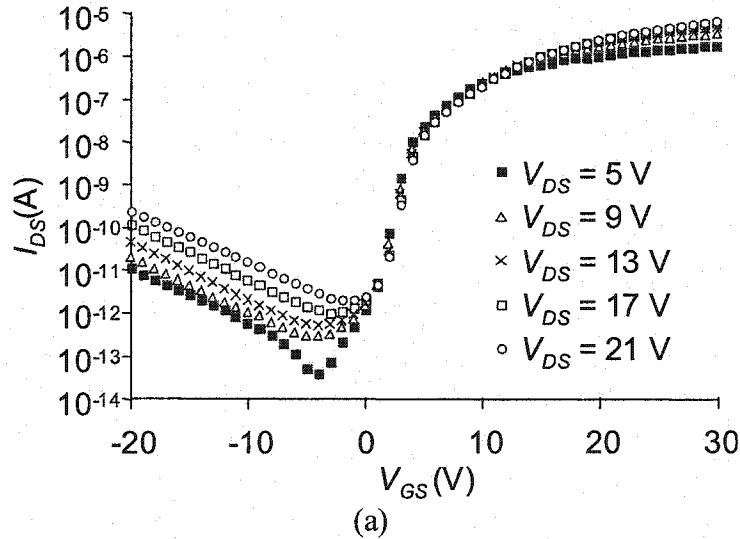
The TFT parameters can be extracted from the TFT saturation mode via the approach in outlined in [36]. Here, using eqn. (88) for a TFT in saturation, the following simplified expression can be written,

$$I_D = \mu_n \frac{Z}{L} \frac{\alpha_1}{2 - \alpha_1} \frac{kTN_c \epsilon_s}{C_{ox}} \left(\frac{(V_{GS} - V_T)}{V_1} \right)^\alpha = K(V_{GS} - V_T)^\alpha \quad (92)$$

where extracting values for K , V_T and α require measurements of above-threshold gate voltages at saturated drain currents over a range of drain voltages and temperatures (since α is a function of temperature). At each fixed temperature, K , V_T and α can be obtained via,

$$\sqrt[\alpha]{\frac{I_d}{K}} = (V_{gs} - V_t) \quad (93)$$

A computer program (such as Excel) can be used to graph and iterate until a self-consistent result is obtained from a straight line fit of an $(I_D/K)^\alpha$ versus V_G curve to the measured data. Once α is obtained from the curve fitting, the y-intercept yields V_T . Common values for α range from 2.2 to 2.5 [10]. Some characteristic curves for in-house fabricated TFTs are displayed below in Figure 100.



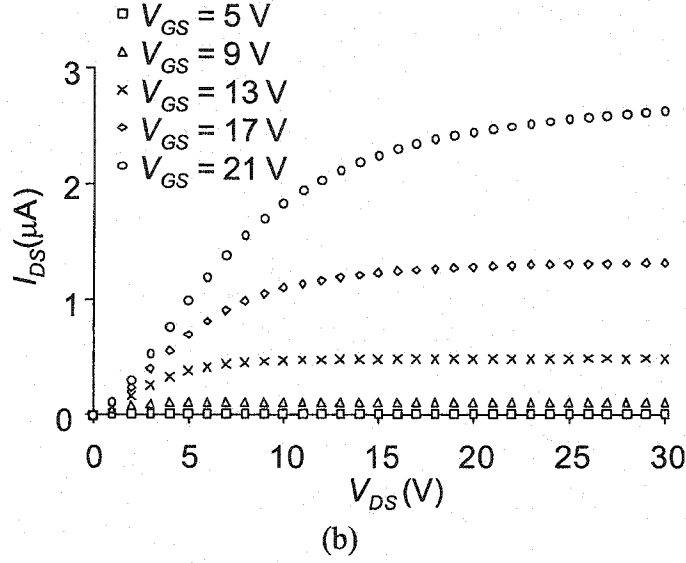


Figure 100. TFT (a) transfer and (b) I-V characteristics

While the above method gives accurate values for V_T , K and α , it is sometimes desirable to extract V_T from the linear mode data of a TFT. The linear mode method for V_T extraction is preferable to the saturation region primarily because of extraction simplicity. As seen in previous sections, the a-Si TFT drain current is not a perfect quadratic function of V_G , but it is proportional to $(V_G - V_T)^\alpha$, where α is around 2.38 for the in-house TFTs at Waterloo.

The validity of the linear mode V_T extraction procedure outlined below is based on [35] where we begin by rewriting eqn. (87) as,

$$I_D = M_0 \frac{1}{\alpha} [(V_{GS} - V_T)^\alpha - (V_{GD} - V_T)^\alpha] \quad (94)$$

Here, $\alpha = 2(T_c/T)$, $M_0 = \mu_{EFF} C_{OX}(Z/L)$ and μ_{EFF} is an effective mobility accounting for the various coefficients detailed in eqn. (2.71). Noting that $[(V_{GS} - V_T)^2 - (V_{GD} - V_T)^2]$ can be reduced to $[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$, eqn (94) can be simplified as,

$$I_D = \frac{M_0}{2} (V_{GS} - V_T)^{\alpha-2} [2(V_{GS} - V_T)V_{DS} - mV_{DS}^2] \quad (95)$$

where it is implicitly assumed that the TFT is operating in linear mode with small V_{DS} and the variable m is used to account for the series expansion used in eqn. (94) [35]. Neglecting the V_{DS}^2 term for the linear mode of operation,

$$I_D \approx M_0 (V_{GS} - V_T)^{\alpha-1} V_{DS} \quad (96)$$

Here, since $(\alpha - 1)$ can be approximated as near unity (~ 1.38), the above equation is simplified as,

$$I_D \approx M_0 (V_{GS} - V_T) V_{DS} \quad (97)$$

Eqn (97) is linear and can be used to extract V_T in the linear region of operation of the TFT. If the TFT's I_D - V_G transfer characteristics are measured in the linear regime and plotted on a linear scale, V_T is given as the intercept of the line extrapolated on the V_G axis as shown in Figure 101. Here, note that the $I_D - V_G$ characteristics are linear at low gate biases but increase sub-linearly (due to series resistance discussed in Chapter 3) as the gate bias increases.

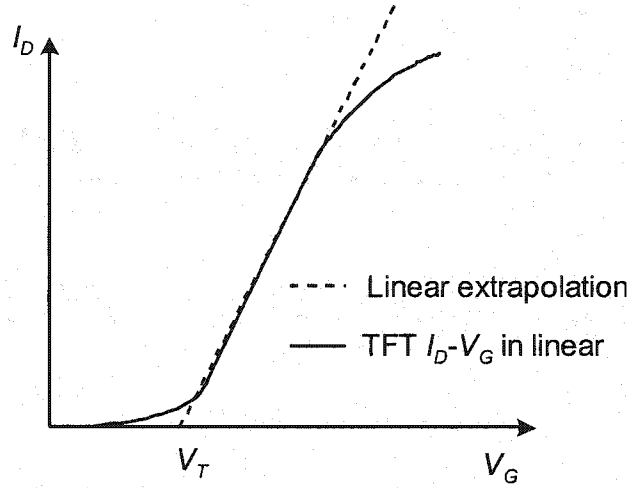


Figure 101. Method for extracting the V_T of a TFT operating in the linear regime.

Appendix D – Mask Layouts

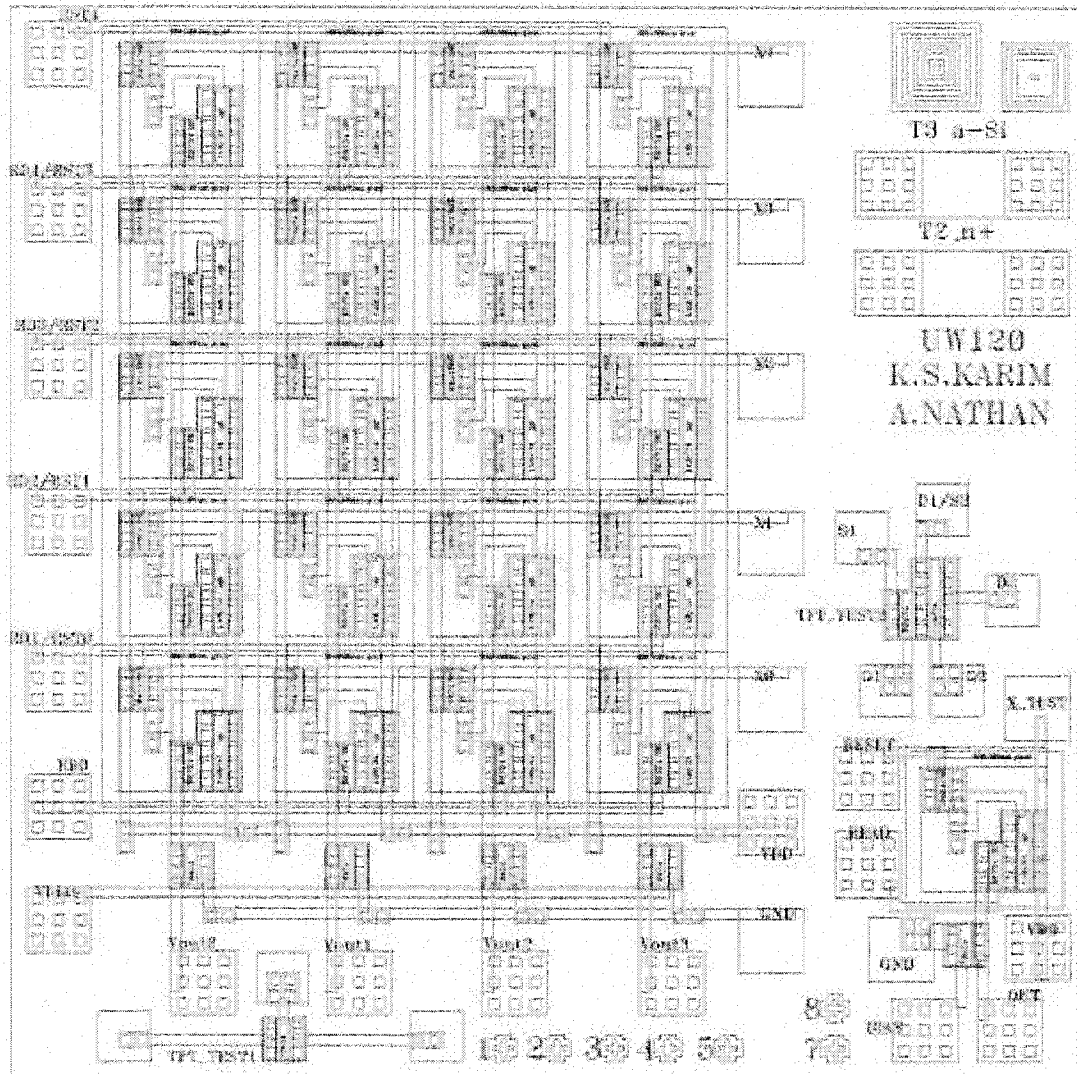


Figure 102. UW 120 - 5 x 4 V-APS array and associated test pixels

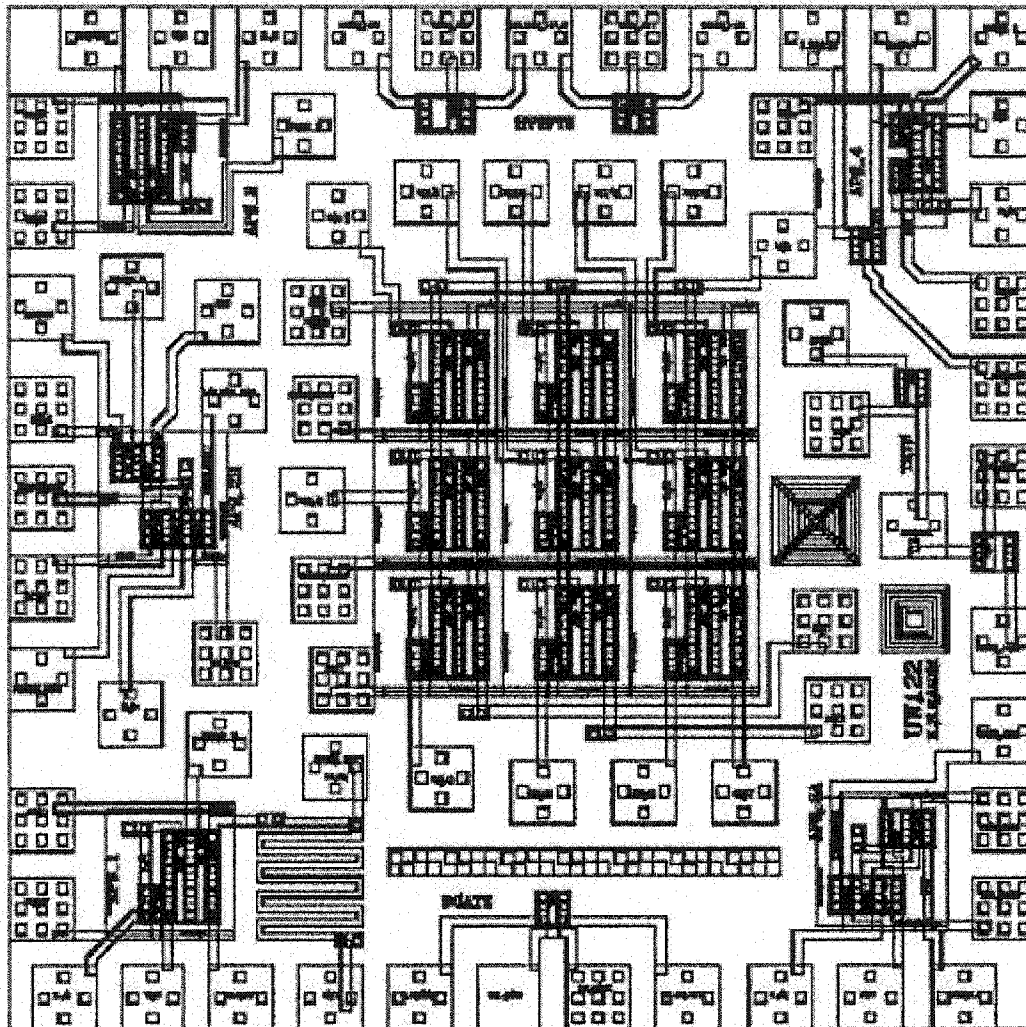


Figure 103. UW 122 - 3 x 3 C-APS Array and various test pixels

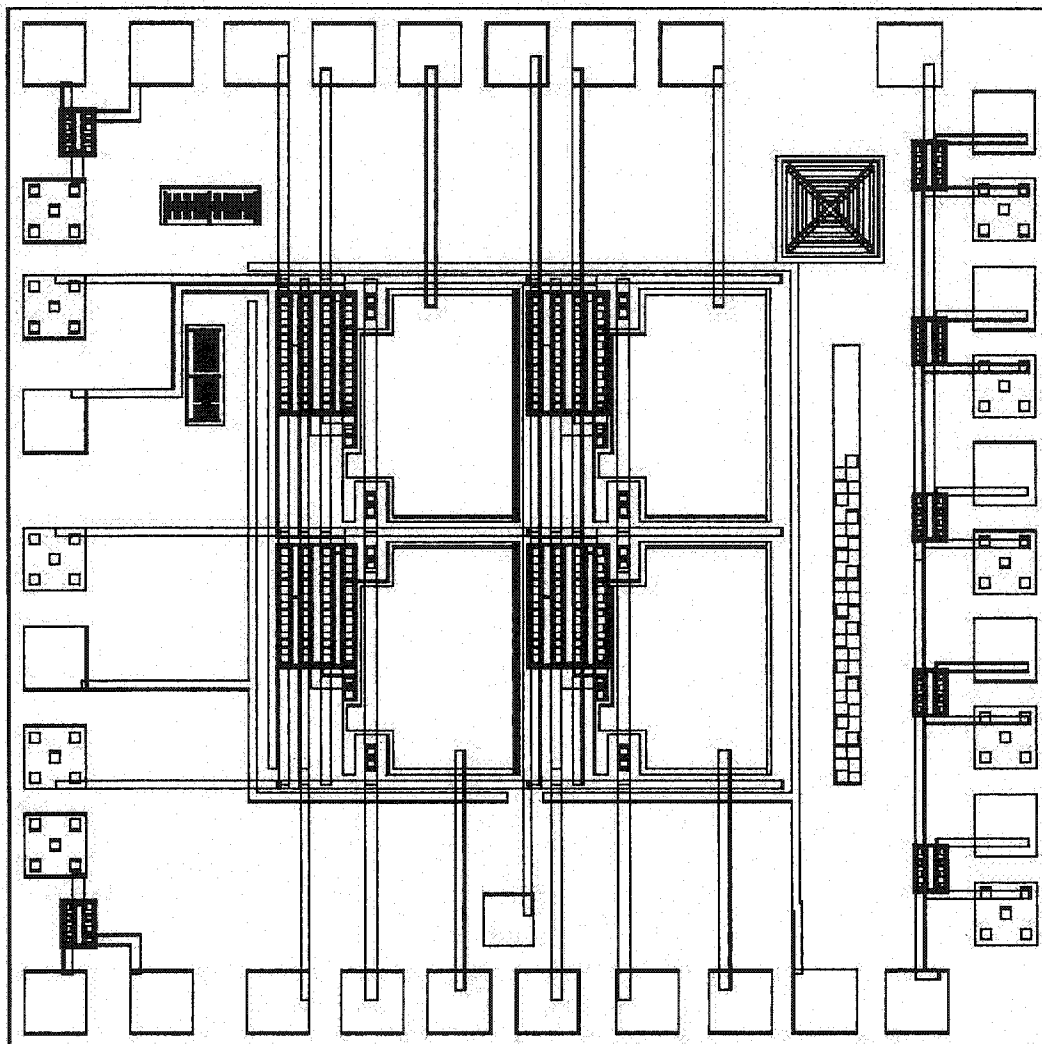


Figure 104. UW 126 - 2 x 2 C-APS Array for integration with a-Se photoconductor and test devices

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